CMOS Data Acquisition Products

A/D Converters
Operational Amplifiers
Display Drivers/Counters
Power Supply Circuits
General Purpose Analog Circuits

The Maxim Advantage

Maxim Integrated Products is an international supplier of analog products for data acquisition and control systems that require real world signal processing.

The demand for quality products to serve this market is accelerating rapidly — fueled in part by the availability of inexpensive microprocessors. Industries new and old are calling for improved quality, higher levels of reliability in the field, effective customer service, and innovative products at no increase in cost.

We at Maxim have accepted this challenge.

In order to fulfill the promise of better products, Maxim has a rigorous system of quality control and reliability testing. This begins with product design and continues through wafer inspection to the final Quality Assurance acceptance prior to shipment. We've made a company-wide commitment to supply the highest quality and best characterized products available to you, the customer.

In addition, Maxim has both national and international sales and distribution capabilities offering immediate world-wide service and support.

Maxim has also taken an innovative approach to Customer Service, assuring on-time deliveries and accurate customer order status. Our Customer Service organization is chartered with predicting and avoiding potential schedule misses and delivery problems, not providing excuses after the fact. Service to the customer, together with an unparalleled Quality Assurance Program, is of the highest priority at our company.

In summary, what Maxim offers the industry is a stable and consistent source of higher quality, consistently reliable products for a fair price — in other words, good value. Moreover, because service comes first at Maxim, the end user at last receives the customer support he requires and has a right to expect. In this way, Maxim can help you be a better supplier to your customer.

We would appreciate the opportunity to serve you.

Jack Gifford
President and Chief Excecutive Officer

Guide to Using This Catalog

The Maxim ADVANTAGE™

The "Maxim Advantage"™ signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters, and device enhancements, when needed, that result in improved preformance without changing the functionality. Furthermore all pins on Maxim's devices are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (test circuit per MilStd883, Method 3015.1).

These Maxim Advantages are listed on the "Maxim Advantage™" page (usually the third page of the data sheet) and are highlighted (shaded) in the Electrical Characteristics table. For reference purposes, the original manufacturer's Electrical Characteristics are reproduced on the page facing the "Maxim Advantage™" page.

In addition to these advantages, Maxim provides enhanced Product Conditioning and Qualification at no additional cost, as described in the "Packaged Unit Process Flow" section (Page A-1).

Data Sheet Identifiers

IDENTIFIER	PRODUCT STATUS	COMMENTS
None	Full Production	Data Sheet finalized.
Advance Information	Initial Production	Data Sheet based on design goals.

Numeric Index

Part number index arranged first by alpha sequence, then by numeric sequence. All suffixes — package/temperature/number of pins are ignored.

Alpha Numeric Index

Part number index arranged by numeric sequence. All alpha prefixes and suffixes are ignored. The complete part number is shown, with the base number bold faced.

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MAXIM

CMOS Data Acquisition Catalog 1985

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*Additional devices listed under "New Products".

General Purpose Analog Circuits*

New Products

Appendix

*Additional devices listed under "New Products".

Alpha Numeric Index

Numeric Index

A/D Converters

MAXIM
3½ Digit A/D Converter

General Description

The Maxim ICL7106 and ICL7107 are monolithic analog to digital converters. They have very high input impedances and require no external display drive circuitry. On-board active components include polarity and digit drivers, segment decoders, voltage reference and a clock circuit. The ICL7106 will directly drive a non-multiplexed liquid crystal display (LCD) whereas the ICL7107 will directly drive a common anode light emitting diode (LED) display.

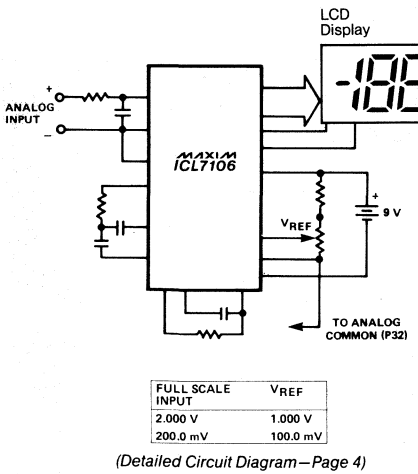
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7106 and ICL7107, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Page 4)

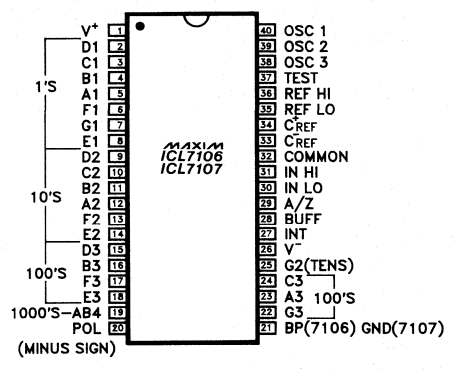
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
  LCD-ICL7106
  LED-ICL7107
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **True Differential Reference and Input**
- **True Polarity Indication for Precision Null Applications**
- **Monolithic CMOS design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7106CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7106CJL	0°C to +70°C	40 Lead CERDIP
ICL7106CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7106C/D	0°C to +70°C	Dice
ICL7107CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7107CJL	0°C to +70°C	40 Lead CERDIP
ICL7107CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7107C/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V+ to V− 15V
- ICL7107, V+ to GND ..... +6V
- ICL7107, V− to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input
- ICL7106 ..... TEST to V+
- ICL7107 ..... GND to V+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Cerdip Package 800mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	-1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- supply current 7107 only			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment voltage = 3V	5 10	8.0 16		mA mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

3½ Digit A/D Converter

- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 7)**
- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Negligible Hysteresis**
- **Maxim Quality and Reliability**
- **Increased Maximum Rating for Input Current (Note 8)**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS:

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1; unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 6)	−000.0	±000.0	+000.0	Digital
	0° ≤ T_A ≤ 70°C (Note 10)	**−000.0**	**±000.0**	**+000.0**	Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 6)	999	999/1000	1000	Digital
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV				
	T_A = 25°C (Note 6)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ 70°C (Note 10)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 6)		1	10	pA
	0° ≤ T_A ≤ 70°C		**20**	**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0				
	T_A = 25°C		0.6	1.8	mA
	0° ≤ T_A ≤ 70°C			**2**	
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	25kΩ between Common & Pos. Supply		75		ppm/°C
7106 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7107 Only—Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment Voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
7106 Only—Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	**V**
Overload Recovery Time (Note 9)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	**Measurement Cycles**

Note 6: Test condition is V_{IN} applied between pins IH-HI and IN-LO. i.e., 1MΩ resistor in Figures 1 and 2.

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 9: Number of measurement cycles for display to give accurate reading.

Note 10: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter

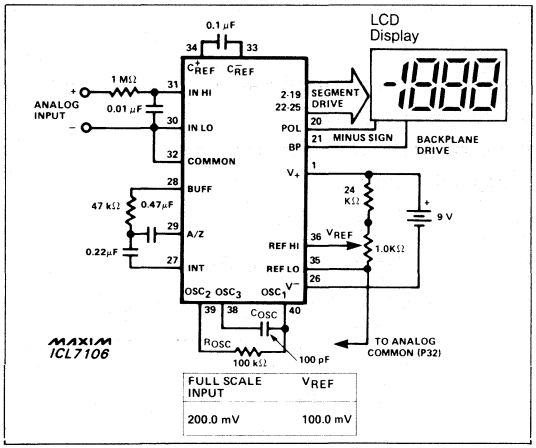


Figure 1. Maxim ICL7106 Typical Operating Circuit

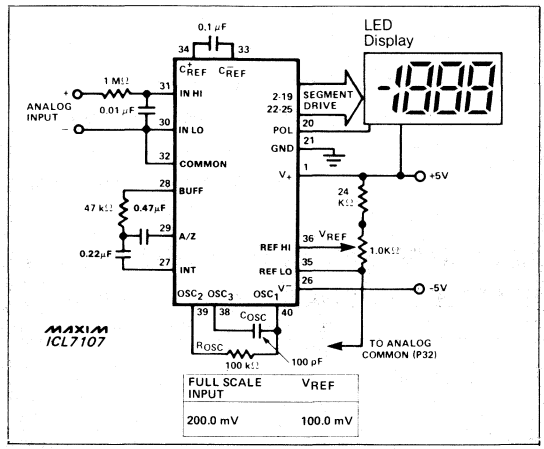


Figure 2. Maxim ICL7107 Typical Operating Circuit

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" overrange conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a rollover voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This happens during de-integration of a positive signal. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

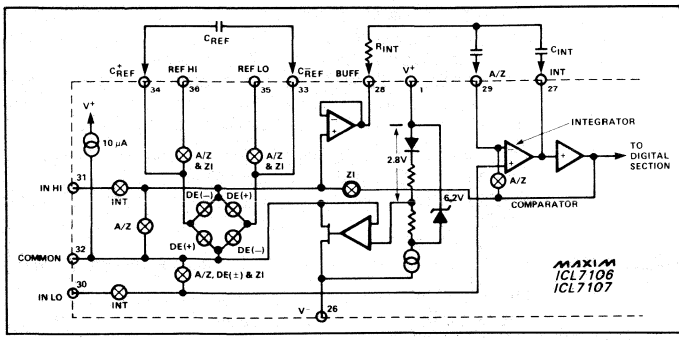


Figure 3. Analog Section of ICL7106/ICL7107

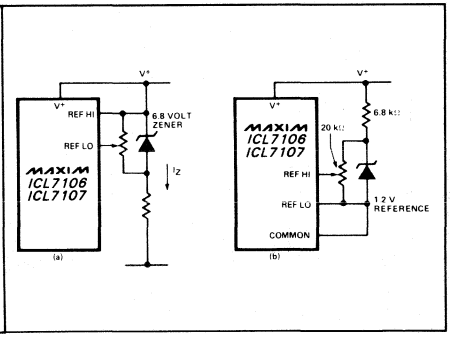


Figure 4. Using an External Reference

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful when using the ICL7106, or for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The analog common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80ppm/°C, and a low voltage coefficient (.001%).

The internal heating of the ICL7107 by the LED display drivers degrades the stability of Analog Common. The power dissipated by the LED display drivers changes with the displayed count, thereby changing the temperature of the die, which in turn results in a small change in the Analog Common voltage. This combination of variable power dissipation, thermal resistance, and temperature coefficient causes a 25–80µV increase in noise near full scale. Another effect of LED display driver power dissipation can be seen at the transition between a full scale reading and an overload condition. Overload is a low power dissipation condition since the three least significant digits are blanked in overload. On the other hand, a near full scale reading such as 1999 has many segments turned on and is a high power dissipation condition. The difference in power dissipation between overload and full scale may cause a ICL7107 with a negative temperature coefficient reference to cycle between overload and a near full scale display as the die alternately heats and cools. An ICL7107 with a positive TC reference will exhibit hysteresis under these conditions: once put into overload by a voltage just barely more than full scale, the voltage must be reduced by several counts before the ICL7107 will come out of overload.

None of the above problems are encountered when using an external reference. The ICL7106, with its low power dissipation, has none of these problems with either an external reference or when using Analog Common as a reference.

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from analog-common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible analog common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, REF-LO should be connected to analog common. This will remove the common-mode voltage from the reference system.

Analog Common is internally tied to an N-channel FET that can sink 30mA or more of current. This will hold the Analog Common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 10µA of source current, however, so COMMON may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD if left in this mode for several minutes.

3½ Digit A/D Converter

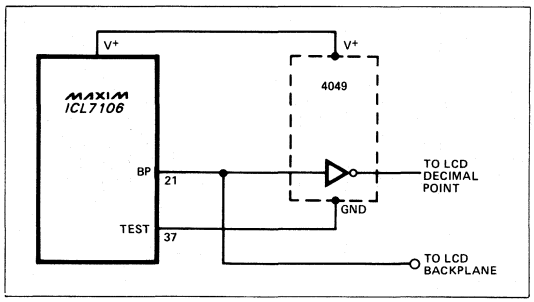


Figure 5A. Fixed Decimal Point Drivers

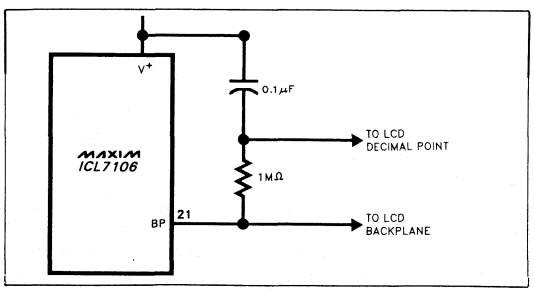


Figure 5B. Fixed Decimal Point Drivers

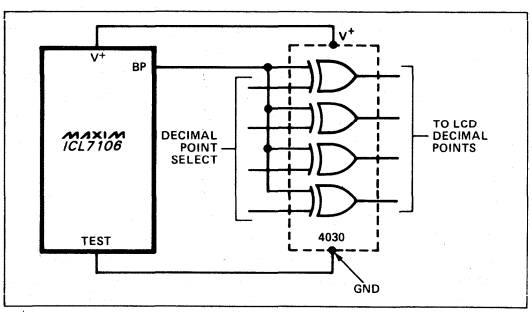


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Digital Section

The digital section for the ICL7106 and ICL7107 is illustrated in Figures 8 and 9. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P-channel source follower. This supply is made stiff to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the segment is ON and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The ICL7107 is identical to the ICL7106 except that the backplane and drivers have been replaced by N-channel segment drivers. The ICL7107 is designed to drive common anode LED's with a typical segment current of 8mA. Pin 19 (thousands digit output) sinks current from two LED segments, and has a 16mA drive capability.

The polarity indication is "on" for negative analog inputs, for both the ICL7106 and ICL7107. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7106 and ICL7107 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 48kHz would be used to obtain three readings per second.

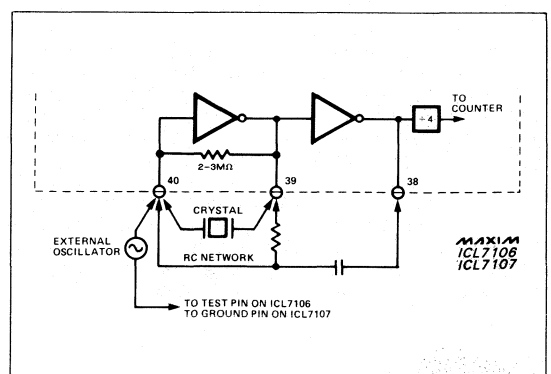


Figure 7. Clock Circuits

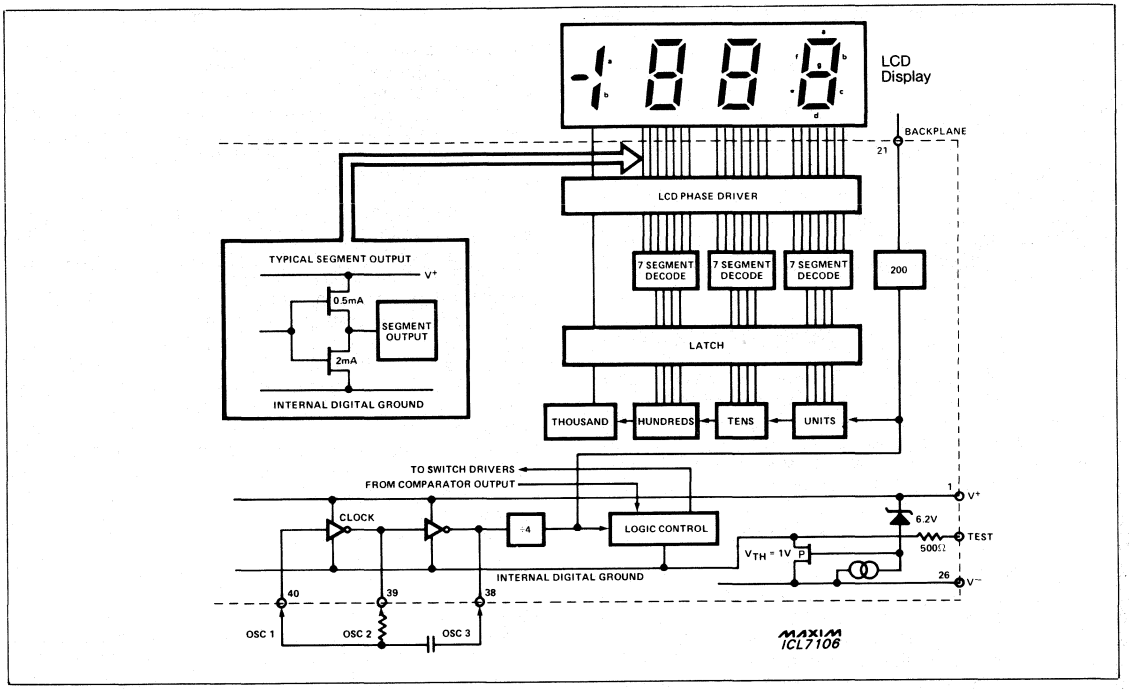


Figure 8. ICL7106 Digital Section

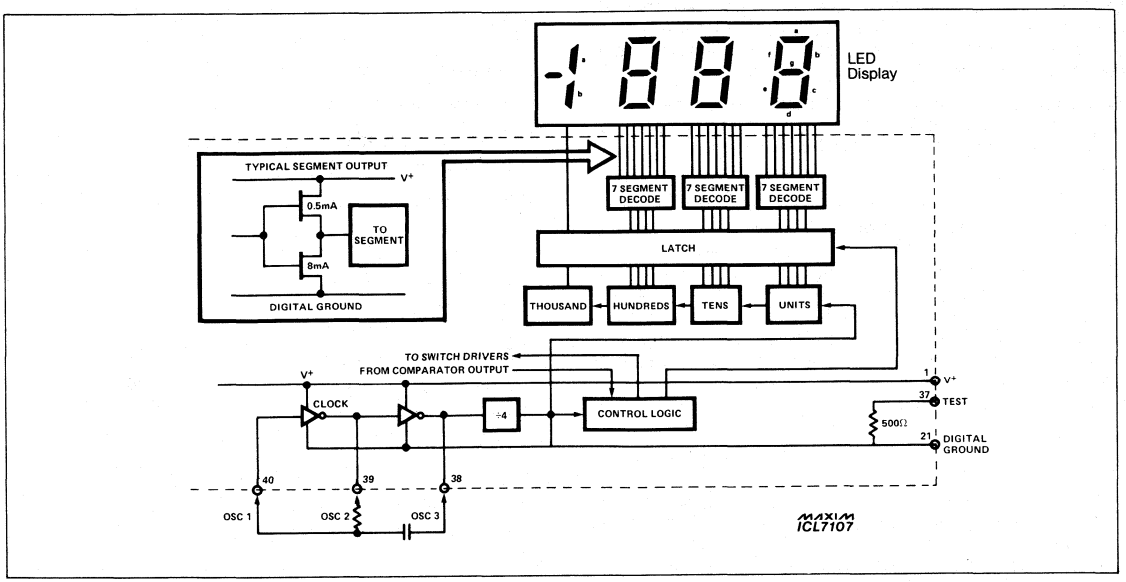


Figure 9. ICL7107 Digital Section

3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For the 2V scale, a 0.047μF capacitor is adequate. A capacitor size of 0.47μF is recommended for 200mV full scale where low noise operation is very important. Due to the ZI phase of Maxim's ICL7106/7, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems seen in other manufacturers' ICL7106/7 which do not have the ZI phase.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent rollover error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (at approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable for the ICL7106 or ICL7107 when the analog common is used as a reference. A nominal ±3.5 to 4 volt swing is acceptable for the ICL7107 with a ±5V supply and analog common tied to supply ground. The nominal values for C_{INT} are 0.22μF and 0.10μF for three readings per second. (48kHz clock). These values should be changed in inverse proportion to maintain the same output swing if different oscillator frequencies are used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 100μA of quiescent current. 20μA of drive current can be supplied with negligible non-linearity. This resistor should be large enough to maintain the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 47KΩ resistor is recommended; (2V scale/470KΩ).

Oscillator Components

A 100KΩ resistor is recommended for all ranges of frequency. By using the equation f = 0.45/RC, the capacitor value can be calculated. For 48kHz clock, (3 readings/second), the oscillator capacitor plus stray capacitance should equal 100pF.

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. Suitable values of the capacitor and integrating resistor would be 0.22μF and 120KΩ. This provides for a slightly quieter system and also avoids a divider network on the input. The ICL7107 can accept input signals up to ±4V with ±5V supplies. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset reading can be conveniently generated.

ICL7107 Power Supplies

The ICL7107 is designed to operate from ±5V supplies. However, when a negative supply is not available it can be generated from a clock output with two diodes, two capacitors, and an inexpensive IC. Refer to Figure 10. Alternatively a −5V supply can be generated using Maxim's ICL7660 and two capacitors.

A negative supply is not required in selected applications. The conditions to use a single +5V supply are:

- An external reference is used.
- The signal is less than ±1.5V.
- The input signal can be referenced to the center of the common-mode range of the converter.

See Figure 18.

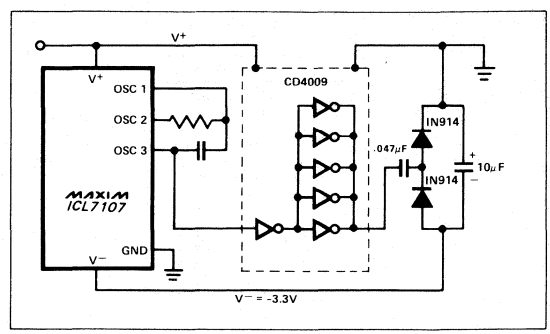


Figure 10. Generating Negative Supply from +5V

Applications Information

Heat is generated within the ICL7107 IC package due to the sinking of LED display current. Fluctuating chip temperature can cause a display to change reading if the internal voltage reference is used. By reducing the power being dissipated such variations can be reduced. The ICL7107 power dissipation is reduced by reducing the LED common anode voltage. The curve tracer illustration showing the relationship between the output current and the output voltage for typical ICL7107 is seen in Figure 11. Note that the typical ICL7107 output is 3.2V (point A), since the typical LED has 1.8V across it (8mA drive current) and its common anode is connected to +5V. Maximum power dissipation is:

$$8.1mA \times 3.2V \times 24 \text{ segments} = 622mW$$

Once the ICL7107 output voltage is above 2V, the LED current is essentially constant as output voltage increases. Point B illustrates that reducing the output voltage by 0.7V results in 7.7mA of LED current, (only 5% reduction). The maximum power dissipation is a reduction of 26% as calculated by:

$$7.7mA \times 2.5V \times 24 \text{ segments} = 462mW$$

As illustrated in Figure 12, reduced power dissipation is easy to obtain. This can be accomplished by placing either a 5.1Ω resistor or a 1 amp diode in series with the display (but not in series with the ICL7107). Point C of Figure 18 illustrates that a resistor will reduce the ICL7107 output voltage when all 24 segments are "On". The output voltage will increase when segments are turned "Off". On the other hand, the diode will result in a relatively steady output voltage, around Point B. The resistor not only reduces the change in power dissipation as the display changes, but also limits the maximum power dissipation. This is due to the fact that as fewer segments are "On", each "On" output drops more voltage and current. The resistor circuit will change about 230mW when changing from the best case of six segments, a "111" display, to worst-case of a "1888" display. If the resistor is removed, the power dissipation change will be 470mW. The resistor, therefore, will reduce the effect of display dissipation on reference voltage drift by about 50%.

As more segments are turned off, the change in LED brightness caused by the resistor is almost unnoticeable. A diode may be used instead of the resistor if it is important to maintain a steady level of display brightness.

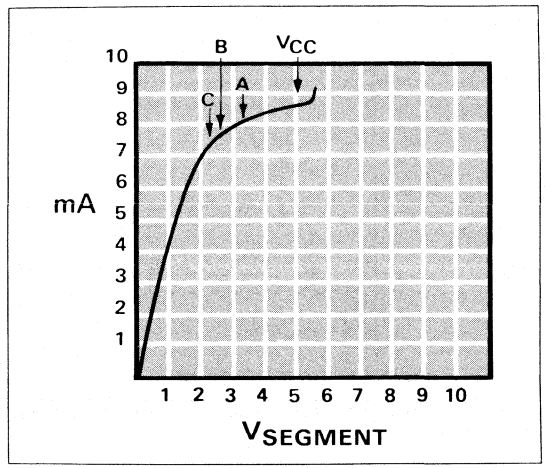


Figure 11. ICL7107 Output Current vs. Output Voltage

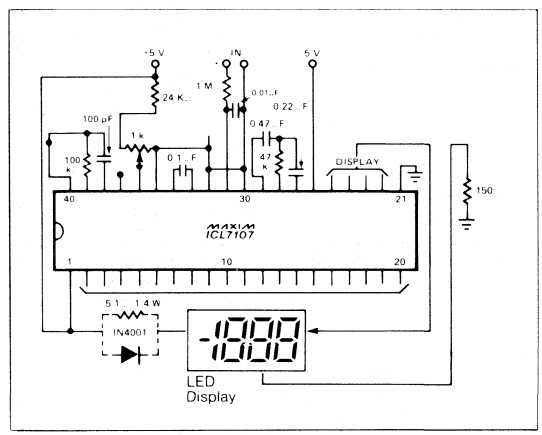


Figure 12. Diode or Resistor Limits Package Power Dissipation

3½ Digit A/D Converter

Typical Applications

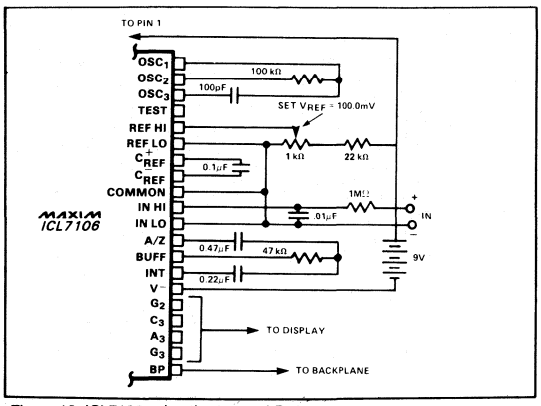


Figure 13. ICL7106 using the Internal Reference. 200mV Full Scale; 3 Readings per Second.

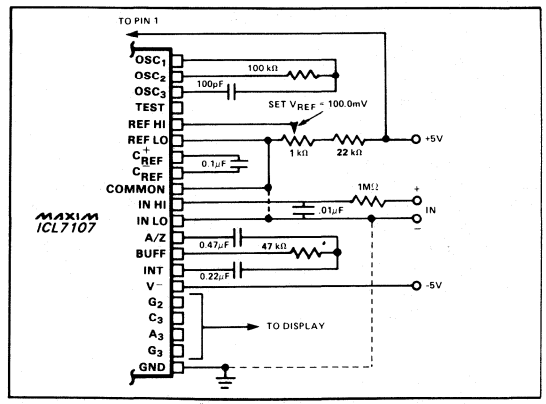


Figure 14. ICL7107 Internal Reference. 200mV Full Scale; 3 Readings per Second, V_{IN} Tied to GND for Single Ended Inputs. (See discussion under "Analog Common".)

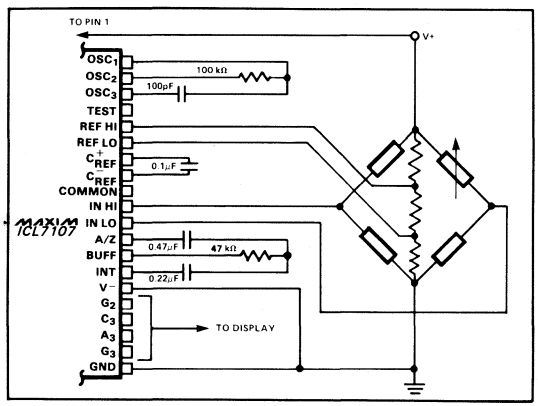


Figure 15. ICL7107 Measuring Ratiometric Values of a Load Cell. Desired Sensitivity is Determined by Resistor Values Within the Bridge.

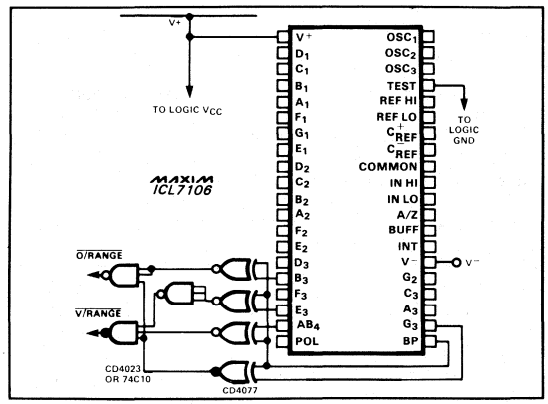


Figure 16. Circuit for Developing Under Range and Over Range Signals from ICL7106 Outputs.

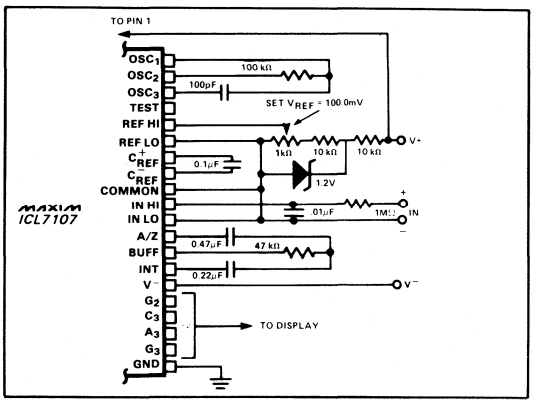


Figure 17. ICL7107 with a 1.2V External Band-Gap Reference V_{IN} tied to common.

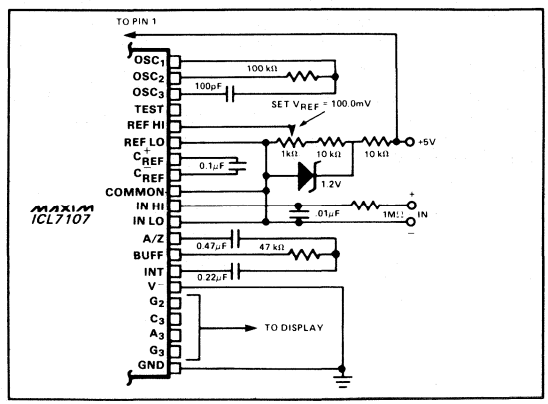


Figure 18. ICL7107 Operated from Single +5V Supply. An external Reference must be used in this application.

Typical Applications

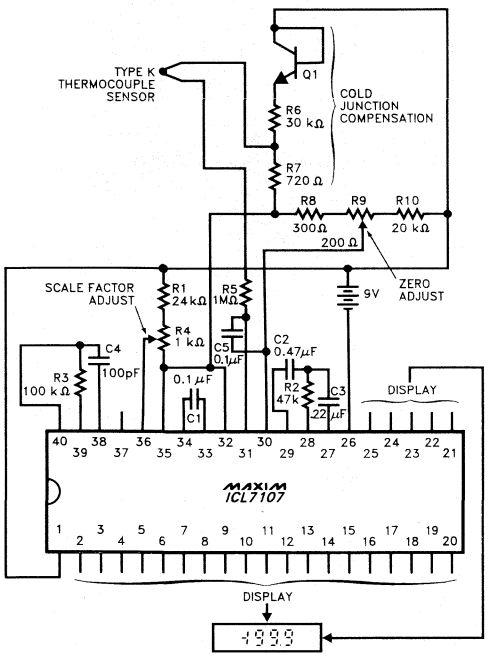


Figure 19. Thermocouple Thermometer. This circuit operates with approximately 50mV reference, so the 50.4mV/°C output of a Type K thermocouple results in 1 count/°C.

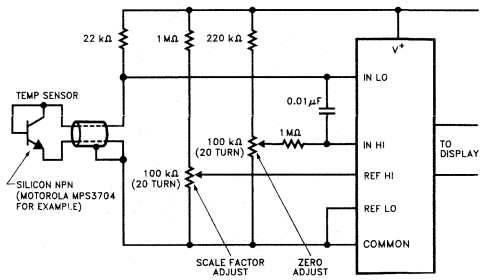


Figure 20. Digital Thermometer

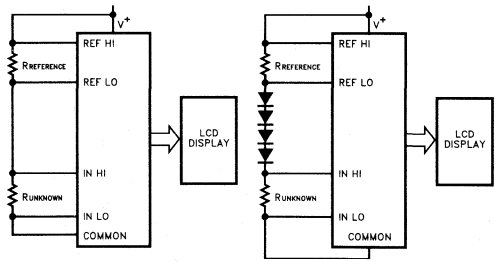
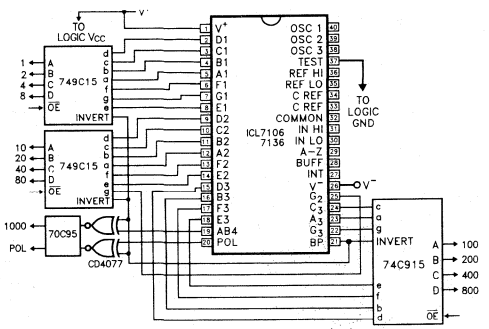
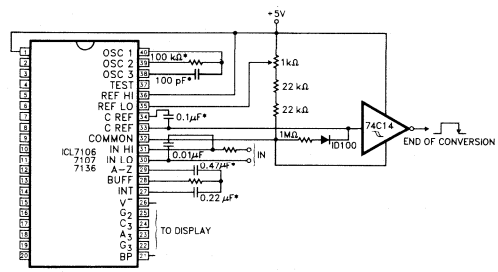


Figure 22. Ratiometric Ohms Measurement



* For ICL7107, tie "INVERT" high, and omit EX-NOR gates.

Figure 21. BCD Output from 7-Segment Drivers

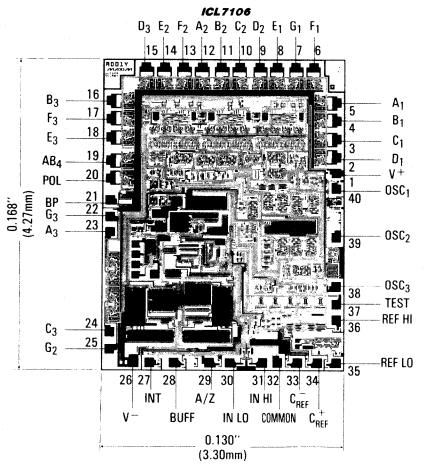


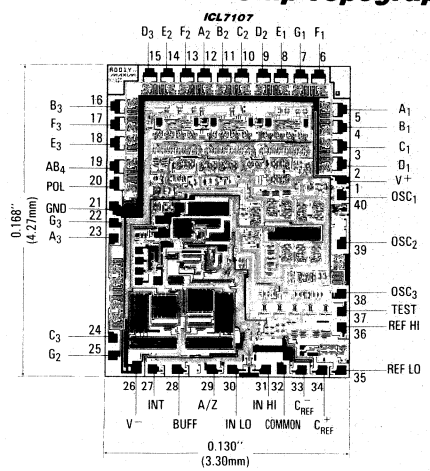
* ICL7106/7 only. See data sheet for values for other parts.

Figure 23. Simple End-of-Conversion Detector

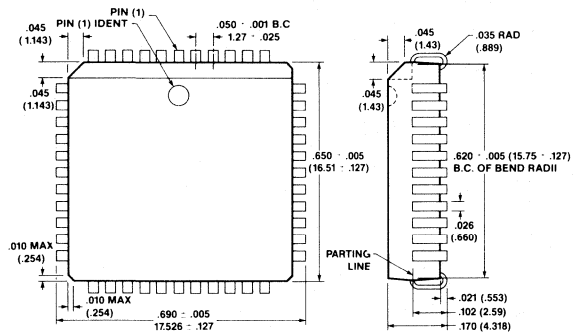
3½ Digit A/D Converter

Chip Topographies

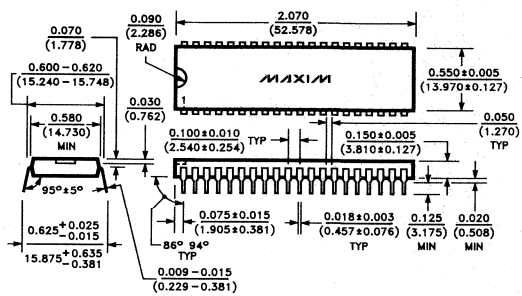




Package Information

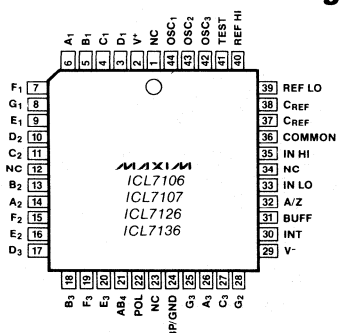


44 Lead Plastic Chip Carrier (Quad Pack) (Q)

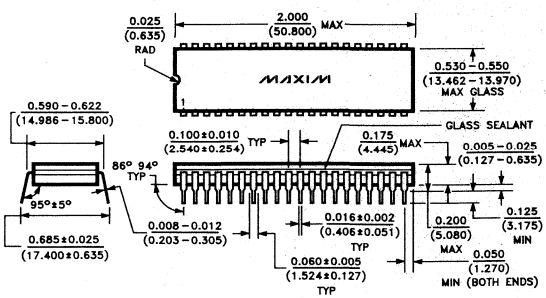


40 Lead Plastic (PL)
θ_{JA} = 100°C/W, θ_{JC} = 45°C/W

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)



40 Lead Cerdip (JL)
θ_{JA} = 45°C/W

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7126 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7126 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7126 a superior device, especially for portable systems.

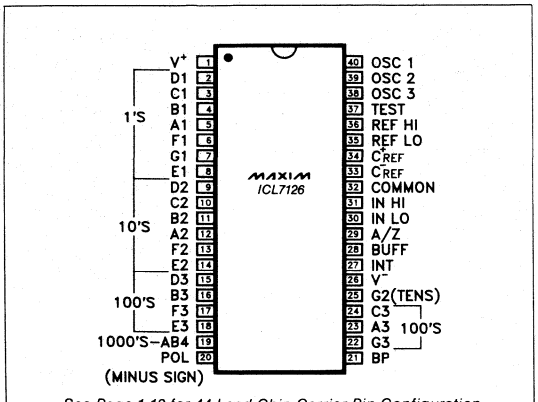
Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7126 eliminates overrange hangover and hysteresis effects. The Zero Integrator phase also allows the use of larger auto zero capacitors reducing noise further. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration



See Page 1-12 for 44 Lead Chip Carrier Pin Configuration

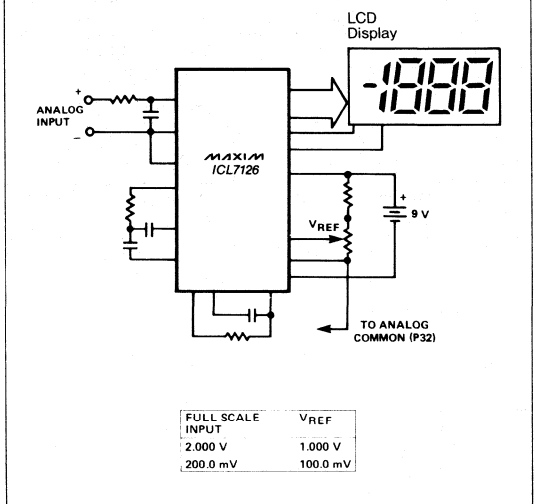
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guaranteed less than 1mW-9V battery life 8000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7126CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7126CJL	0°C to +70°C	40 Lead CERDIP
ICL7126CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7126C/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram—Figure 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 8)	999	999/1000	1000	Digital
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ 200.0mV				
	T_A = 25°C (Note 8)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 12)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0				
	T_A = 25°C		60	100	µA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	**V_{IN} changing from ± 10V to 0V**		**0**	**1**	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO. i.e., 1MΩ resistor in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

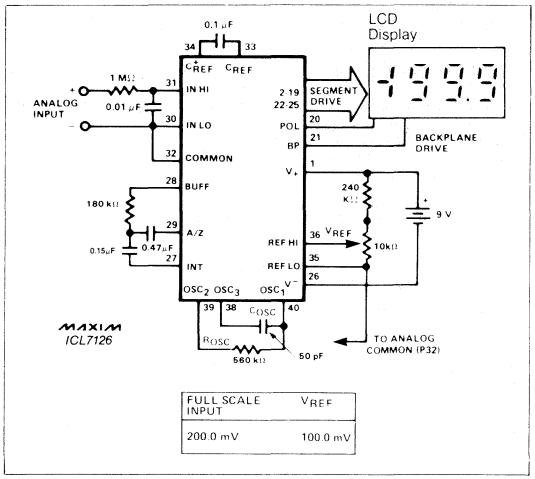


Figure 1. Maxim ICL7126 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

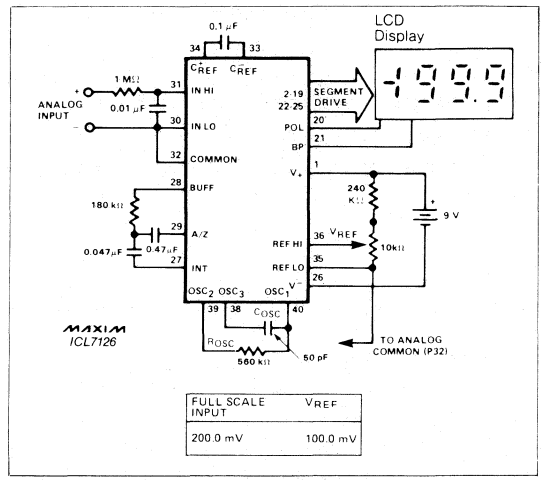


Figure 2. Maxim ICL7126 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

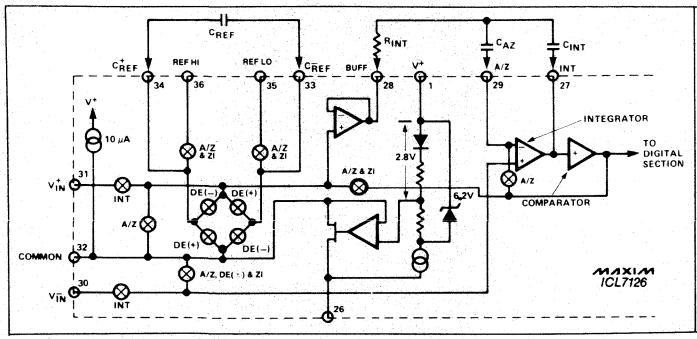


Figure 3. Analog Section ICL7126

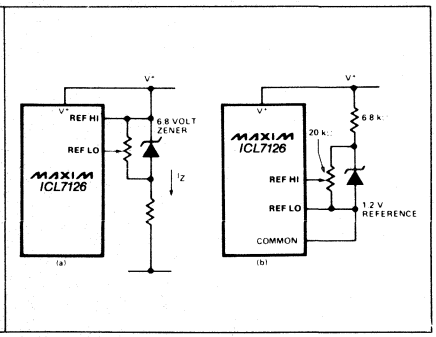


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7126. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

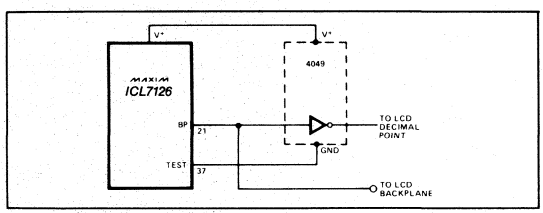


Figure 5. Simple Inverter for Fixed Decimal Point

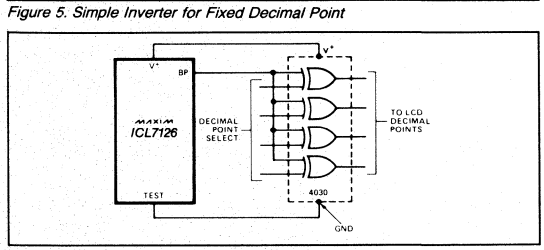


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

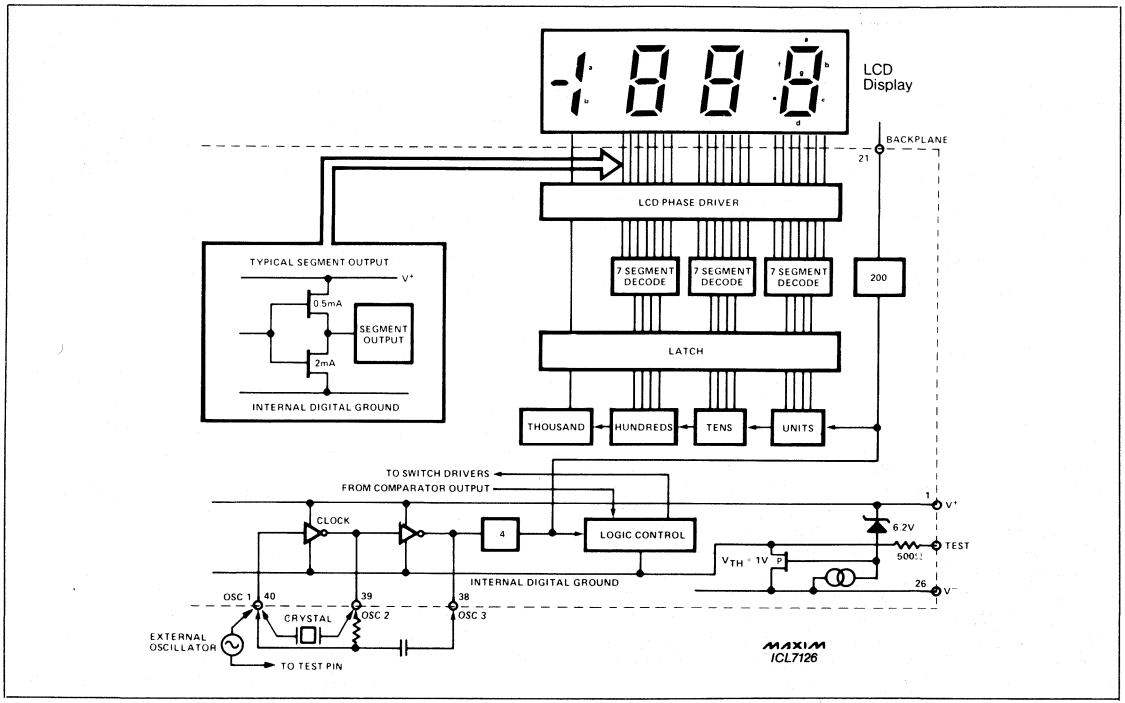


Figure 7. ICL7126 Digital Section

Digital Section

The digital section for the ICL7126 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7126. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7126 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80khZ, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000) clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. While the Maxim ICL7126 will operate with a 0.33μF capacitor, a 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held to half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

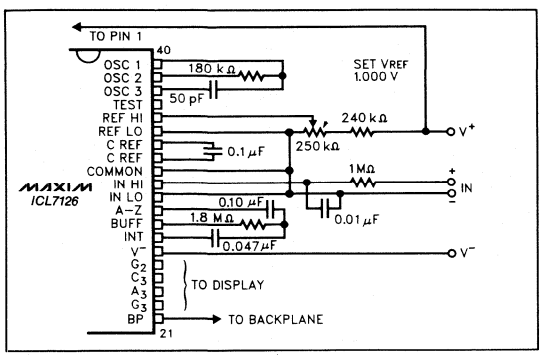


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

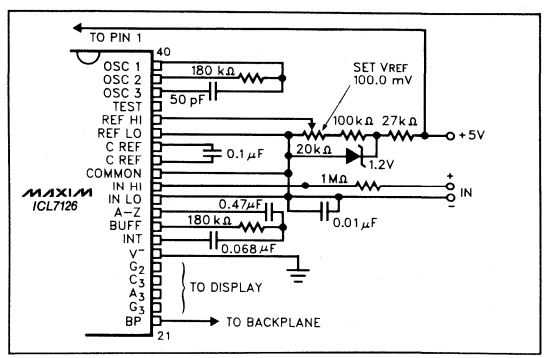


Figure 9. 7126 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

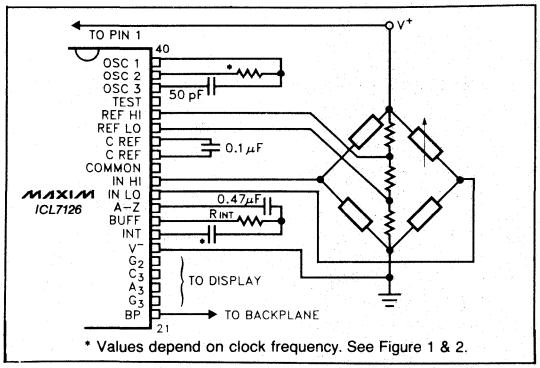


Figure 10. 7126 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

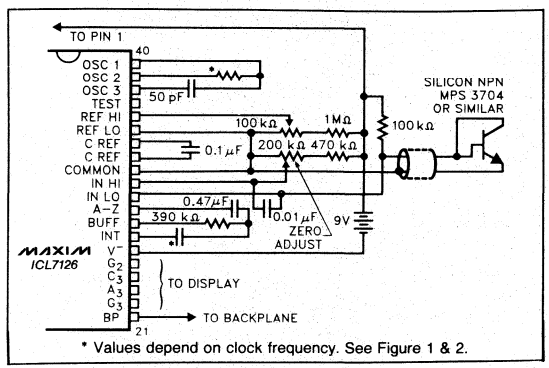
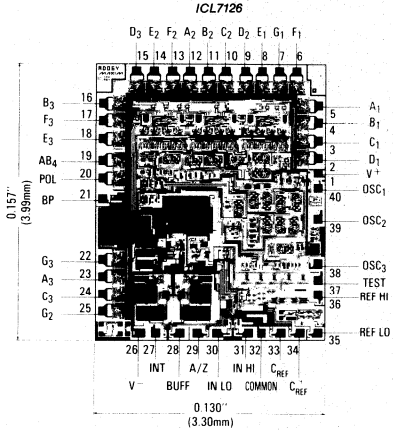
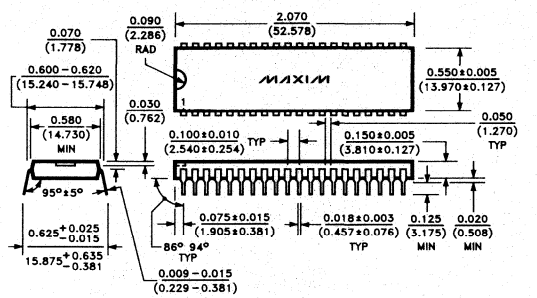


Figure 11. 7126 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/° C/. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

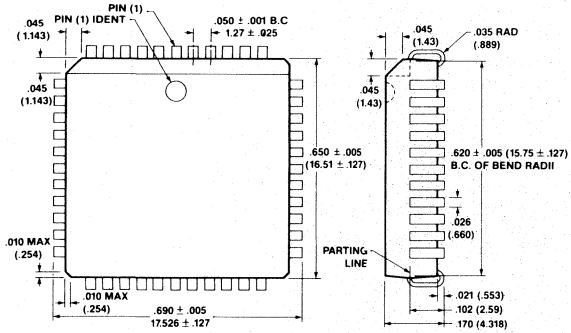
Chip Topography



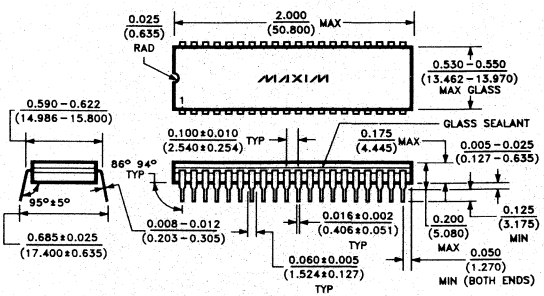
Package Information



40 Lead Plastic (PL)
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W



44 Lead Plastic Chip Carrier (Quad Pack) (Q)



40 Lead Cerdip (JL)
θ_{JA} = 45°C/W

MAXIM

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7136 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7136 a superior device, especially for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7136 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

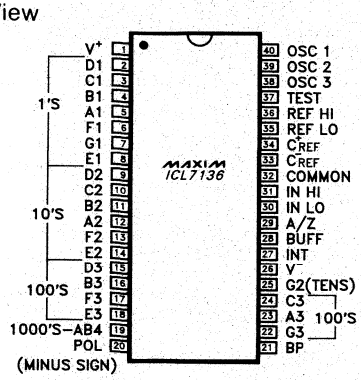
Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Pin Configuration

Top View



See Page 1-12 for 44 Lead Chip Carrier Pin Configuration

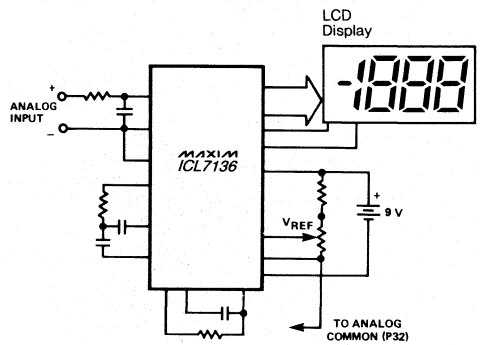
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Power dissipation guaranteed less than 1mW-9V battery life 8000 hours typical**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LCD Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

Part	Temp. Range	Package
ICL7136CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7136CJL	0°C to +70°C	40 Lead CERDIP
ICL7136CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7136C/D	0°C to +70°C	Dice

Typical Operating Circuit



FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Figure 1 & 2)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \simeq$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0V (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A = 25°C, f_{CLOCK} = 16kHz and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed over Temperature**
- **Guaranteed Overload Recovery Time**
- **Significantly Improved ESD Protection (Note 9)**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 10)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 8)	−000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**−000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 8)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ +70°C (Note 12)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−V_{IN} = +V_{IN} 200.0mV				
	T_A = 25°C (Note 8)	−1	±.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 12)		±.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0				
	T_A = 25°C (Note 8)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0				
	T_A = 25°C		60	100	µA
	0° ≤ T_A ≤ +70°C			**120**	
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
Test Pin Voltage	**With respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ±10V to 0V		0	1	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO. i.e., 1MΩ resistor in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.

Low Power, 3½ Digit A/D Converter

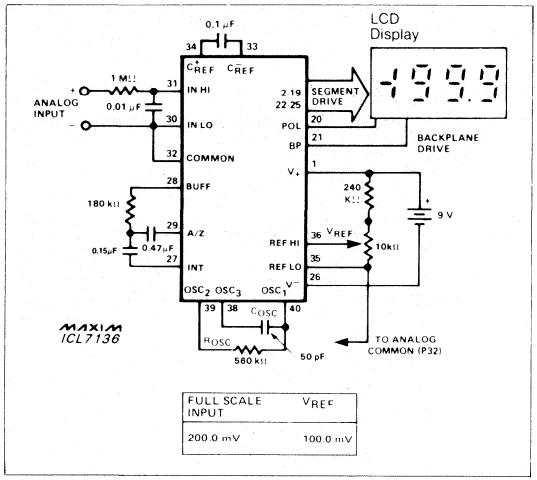


Figure 1. Maxim ICL7136 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)

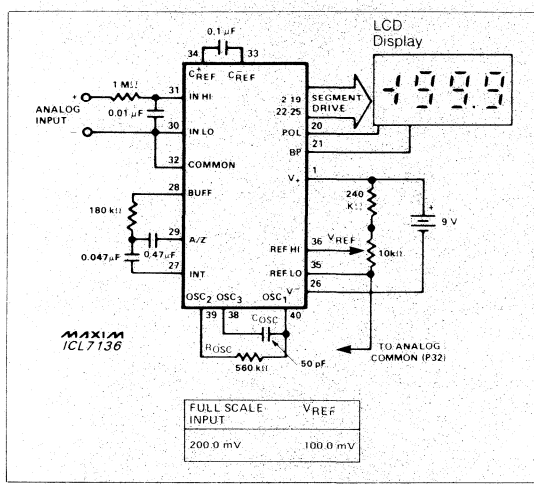


Figure 2. Maxim ICL7136 Typical Operating Circuit Clock Frequency 48kHz (3 readings/sec)

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)

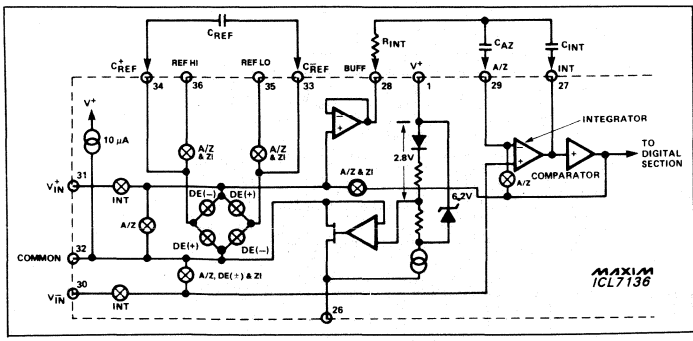


Figure 3. Analog Section of 7136

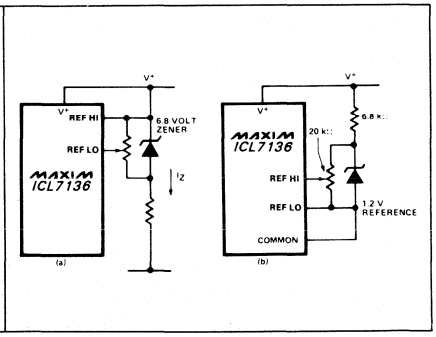


Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7136. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.

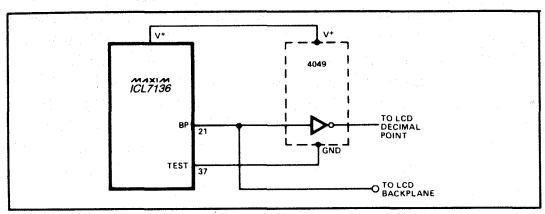


Figure 5. Simple Inverter for Fixed Decimal Point

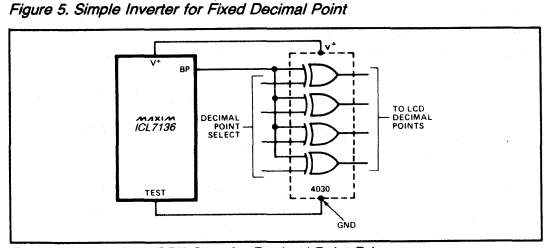


Figure 6. Exclusive "OR" Gate for Decimal Point Drive

Low Power, 3½ Digit A/D Converter

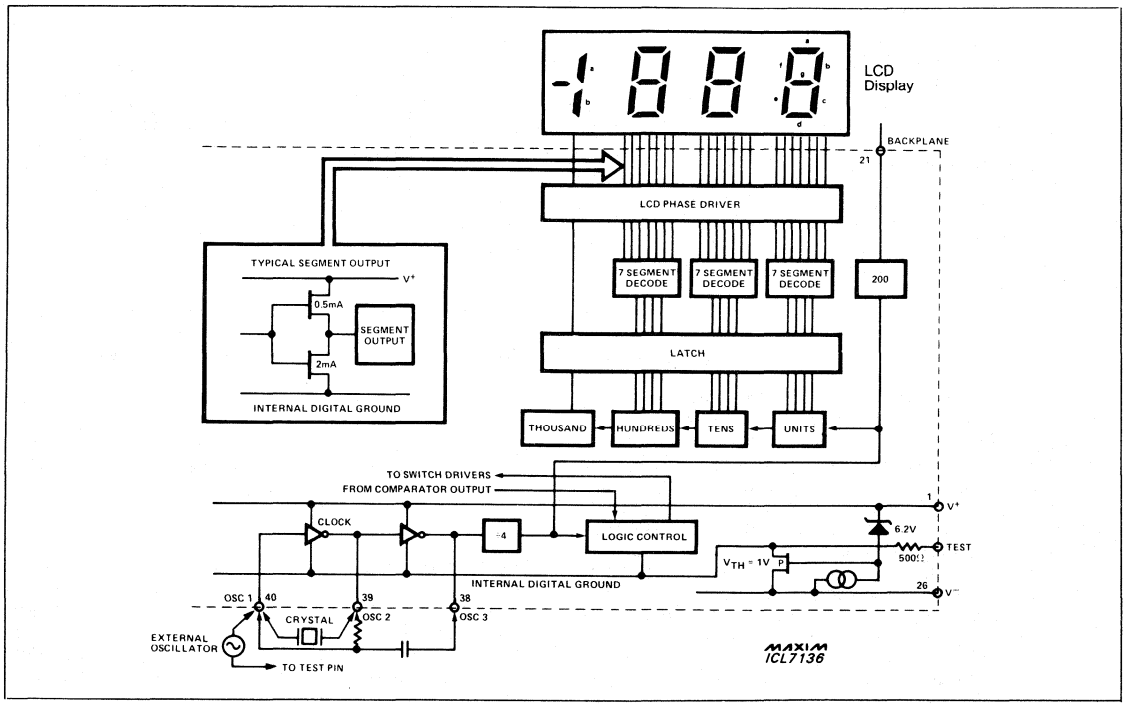


Figure 7. ICL7136 Digital Section

Digital Section

The digital section for the ICL7136 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currrents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7136. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7136 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.
2. An external oscillator connected to pin 40.
3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000 clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a 0.1μF capacitor is adequate. A 0.47μF capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a 0.1μF capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held half a count by using a 1.0μF capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is 0.15μF at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with 6μA of quiescent current and can supply 1μA of drive current with negligible non-linearity.

The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a 180kΩ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 200mV. A suitable value of the integrating resistor would be 330kΩ. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), R = 180kΩ, for 16kHz, R = 560kΩ.

Typical Applications

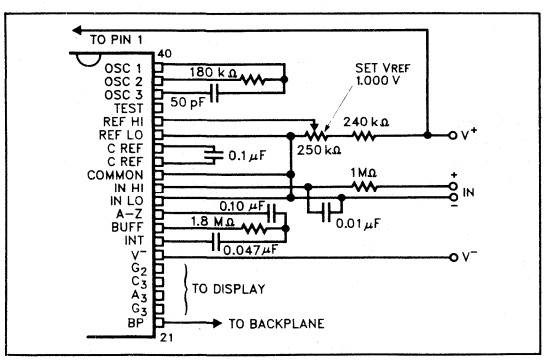


Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.

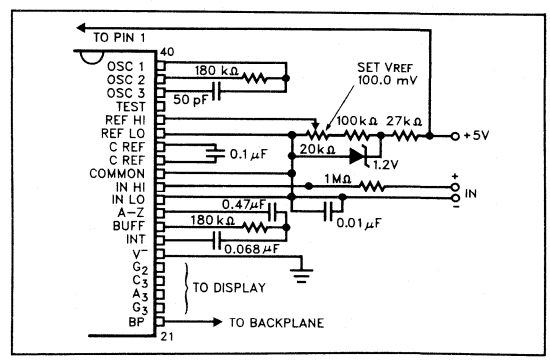


Figure 9. 7136 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

Low Power, 3½ Digit A/D Converter

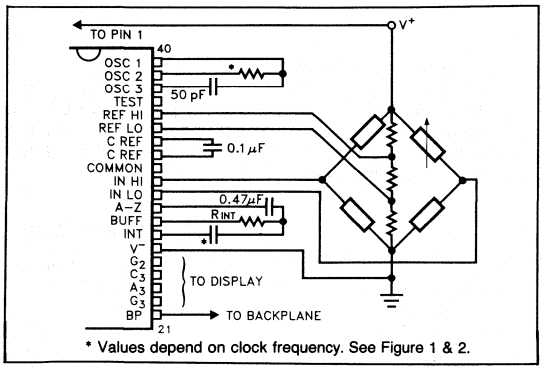


Figure 10. 7136 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

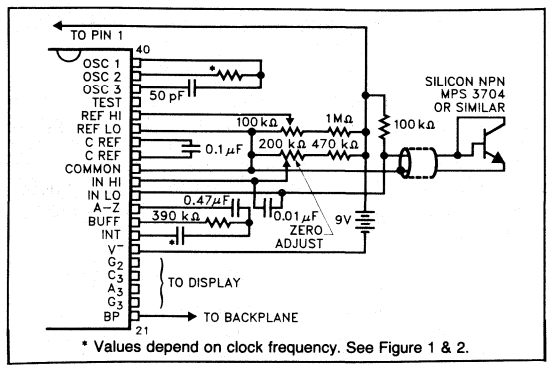
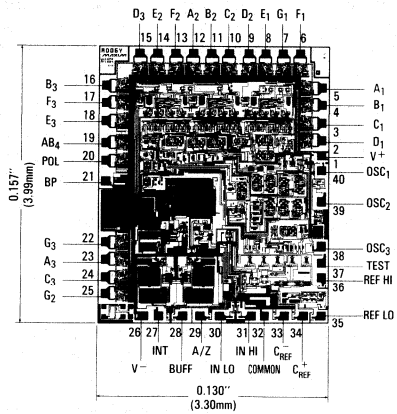
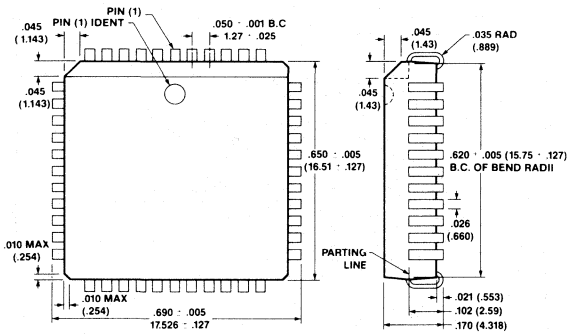


Figure 11. 7136 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography

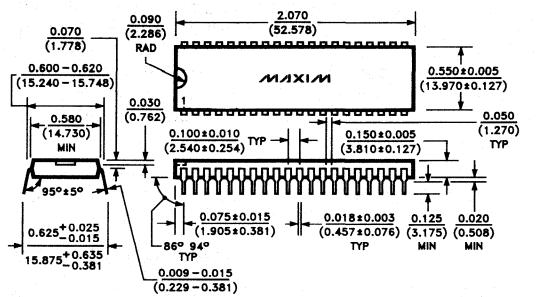
ICL7136



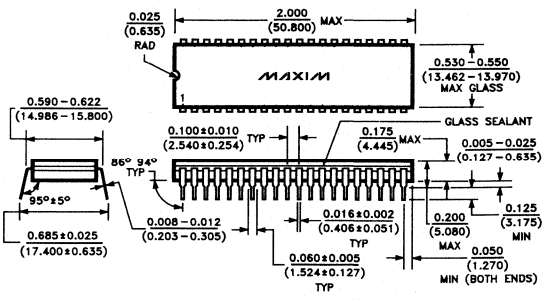


44 Lead Plastic Chip Carrier (Quad Pack) (Q)

Package Information



40 Lead Plastic (PL)
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W



40 Lead Cerdip (JL)
θ_{JA} = 45°C/W

MAXIM

12 Bit A/D Converter With 3-State Binary Outputs

General Description

The ICL7109 is a monolithic 12 bit A/D converter designed for easy interface with microprocessors and UARTs. The 12 bit binary plus polarity and over-range outputs can be directly interfaced to a microprocessor bus. In this mode the ICL7109 is controlled by the microprocessor through the chip select and two byte enable inputs. For remote data logging applications the ICL7109 outputs are easily converted to a UART handshake mode, working with industry standard UARTs to provide serial data transmission.

This device offers high accuracy by lowering rollover error to less than 1 count and zero reading drift to less than 1 μV/°C. In many data acquisition systems the ICL7109 is an attractive, low cost, one-per-channel alternative to analog multiplexing due to its low power consumption and input bias current.

Maxim has added a zero-integrator phase to the ICL7109, eliminating overrange hangover, "crosstalk" and hysteresis effects. Maxim has also increased the current sourcing capabilities of the ICL7109, enabling it to rapidly drive the large capacitances often found on microprocessor busses.

Applications

This device is used in a wide range of data acquisition and control applications. Most applications involve the measurement of analog data:

Pressure	Speed	Voltage
Resistance	Flow	Weight
Temperature	Power	Current

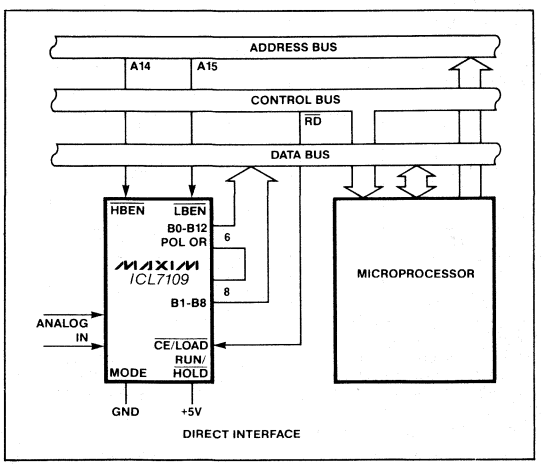
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Zero Integrator Phase for Fast Overload Recovery**
- **Hysteresis and "Crosstalk" Eliminated**
- **Enhanced Bus Driving Capability**
- **Byte Organized Three-state Outputs**
- **UART Handshake Mode for Serial Interfacing**
- **True Differential Input and Reference**
- **Up to 30 Conversions per Second**
- **Significantly Improved ESD Protection**
- **Monolithic, Low Power CMOS Design**

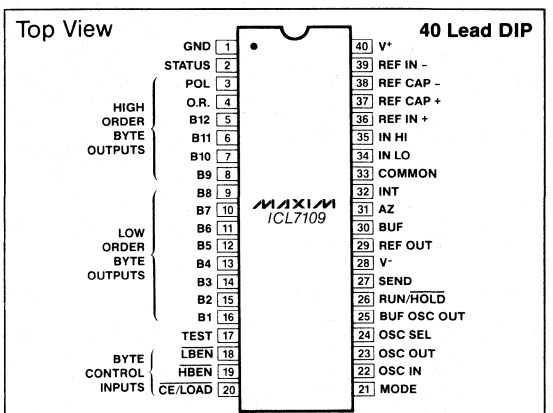
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7109MJL	-55°C to +125°C	40 Lead CERDIP
ICL7109IJL	-20°C to +85°C	40 Lead CERDIP
ICL7109CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7109CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7109C/D	0°C to +70°C	Dice

Typical Operating Circuit



Pin Configuration



See Last Page for 44 Lead Chip Carrier Pin Configuration.

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

12 Bit A/D Converter With 3-State Binary Outputs

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... -9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) .. V^+ to V^-
Digital Input Voltage
(Pins 2-27) (Note 2) .... GND - 0.3V ≤ V_{IN} ≤ V^+ + 0.3V
Power Dissipation (Note 3)
Cerdip Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Plastic Chip Carrier (Quad) ..... 400mW @ +70°C

Operating Temperature
Cerdip Package (MJL) ..... -55°C ≤ T_A ≤ +125°C
Cerdip Package (CJL) ..... -20°C ≤ T_A ≤ +85°C
Plastic Package (CPL) ..... 0°C ≤ T_A ≤ +70°C
Plastic Chip Carrier
(Quad) Package (Q) ..... 0°C ≤ T_A ≤ 70°C
Storage Temperature ..... -65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 4.096V Over full operating temperature range.	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	VCMR	Input Hi, Input Low, Common	V^- +1.5		V^+ -1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage current at Input	I_{ILK}	V_{IN} = 0 All devices 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C ICL7109IDC -25°C ≤ T_A ≤ +85°C ICL7109MDL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV = > 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C
Input Common Mode Range	V_{CM}	IN HI, IN LO, COMMON	V^- +1.5	V^+ -0.5 to V^- +1.0	V^+ -1.0	V

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100 μA.

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

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12 Bit A/D Converter With 3-State Binary Outputs

- ♦ Zero Integrator Phase ensures fast overload recovery
- ♦ "Crosstalk" and Hysteresis Eliminated
- ♦ Bus Driving Capability Enhanced
- ♦ Maxim Quality and Reliability
- ♦ Significantly Improved ESD Protection (Note 4)

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Recovery Time				**0**	**1**	**Measurement Cycles**
Zero Input Reading		V_{IN} = 0.0V Full Scale = 409.6mV	-0000_8	$\pm0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 5)	-1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)		Full Scale = 409.6mV to 2.048V Over full operating temperature range (Note 5)	-1	±.2	+1	Counts
Common Mode Rejection Ratio	CMRR	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Input Common Mode Range	V_{CMR}	Input Hi, Input Low, Common	V^- +1.5		V^+ -1.0	V
Noise (p-p value not exceeded 95% of time)	e_n	V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input	I_{ILK}	V_{IN} = 0V All devices, T_A = 25°C ICL7109CPL CQ 0°C ≤ T_A ≤ +70°C ICL7109IJL -20°C ≤ T_A ≤ +85°C ICL7109MJL -55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} ≈ 408.9mV ≈ 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I^+	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29 open		700	1500	μA
Supply Current V^+ to V^-	I_{SUPP}			700	1500	μA
Ref Out Voltage	V_{REF}	Referred to V^+, 25kΩ between V^+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C

Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (test circuit per Mil Std 883, Method 3015.1).

Note 5: A 4.096V full scale voltage exceeds the Common Mode Voltage Range of the device. The full scale voltage has therefore been changed to 2.048V.

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

(All parameters with V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current		Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current		Pins 18, 19, 20 V_{OUT} = V^+ -3V MODE input at GND		5		μA
Control I/O Loading		HBEN Pin 19 LBEN Pin 18			50	pF
Input High Voltage	V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage	V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current		Pins 26, 27 V_{OUT} = V^+ -3V		5		μV
Input Pull-up Current		Pins 17, 24 V_{OUT} = V^+ -3V		25		μA
Input Pull-down Current		Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High O_{OH}	V_{OUT} = 2.5V		1		mA
	Low O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width	tw		50			ns

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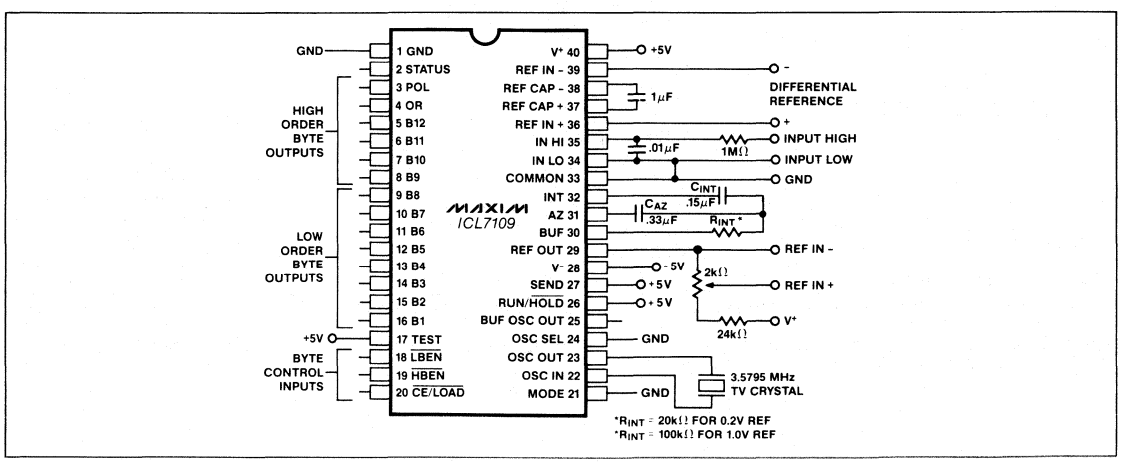

Figure 1. ICL7109 Test Circuit

12 Bit A/D Converter With 3-State Binary Outputs

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, GND = 0V, T_A = 25°C, unless noted.)

DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		**V_{OH}**	**Pins 2-16, 18-20. I_{OUT} = 1mA** **I_{OUT} = 100µA**	**3.5** **4.0**	**4.3** **4.5**		**V** **V**
Output Low Voltage		V_{OL}	I_{OUT} = -1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	µA
Control I/O Pullup Current			**Pins 18, 19, 20 V_{OUT} = V^+ -3V** **MODE input at GND**	**2**	**5**	**20**	**µA**
Control I/O Loading			HBEN Pin 19, LBEN Pin 18			50	pF
Input High Voltage		V_{IH}	Pins18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			**Pins 26, 27 V_{OUT} = V^+ -3V**	**2**	**5**	**20**	**µA**
Input Pull-up Current			**Pins 17, 24 V_{OUT} = V^+ -3V**	**5**	**25**	**100**	**µA**
Input Pull-down Current			**Pin 21 V_{OUT} = GND +3V**	**2**	**5**	**20**	**µA**
Oscillator Output Current	**High**	**O_{OH}**	**V_{OUT} = 2.5V**	**1**	**2**		**mA**
	Low	**O_{OL}**	**V_{OUT} = 2.5V**	**1.5**	**3**		**mA**
Buffered Oscillator Output Current	**High**	**BO_{OH}**	**V_{OUT} = 2.5V**	**2**	**4**		**mA**
	Low	**BO_{OL}**	**V_{OUT} = 2.5V**	**5**	**10**		**mA**
MODE Input Pulse Width		t_W	(Note 6)	50			ns
Byte Enable Width		t_{BEA}	(Note 6)	350	100		ns
Data Access Time from Byte Enable		t_{DAB}	(Note 6)		150	350	ns
Data Hold Time from Byte Enable		t_{DHB}	(Note 6)		100	300	ns
Chip Enable Width		t_{CEA}	(Note 6)	400	120		ns
Data Access Time from Chip Enable		t_{DAC}	(Note 6)		175	400	ns
Data Hold Time from Chip Enable		t_{DHC}	(Note 6)		150	400	ns

Note 6: Guaranteed by design; sample tested only.

12 Bit A/D Converter With 3-State Binary Outputs

Table 1. PIN FUNCTIONS

PIN	FUNCTION	TYPE	DESCRIPTION
1	GND		Ground return for digital logic, 0V
2	STATUS	Output	HI = Converter in integrate phase, or deintegrate phase until data is latched LO = Converter in zero-integrator phase, auto-zero phase, or deintegrate phase after data is latched.
3	POL	Three state data output bits	Polarity — HI = Positive input.
4	OR		Overrange — HI = Overranged
5	B12		Bit 12 = Most significant bit
6	B11		Bit 11
7	B10		Bit 10
8	B9		Bit 9
9	B8		Bit 8
10	B7		Bit 7
11	B6		Bit 6
12	B5		Bit 5
13	B4		Bit 4
14	B3		Bit 3
15	B2		Bit 2
16	B1		Bit 1 = Least significant bit.
17	TEST	Input	HI = Normal operation LO = All output bits high. MID = Counter output latches enabled. Connect to +5V if not used.
18	$\overline{\text{LBEN}}$	Input Output	Low Byte Enable. When MODE is low and $\overline{\text{CE/LOAD}}$ is low, taking Low Byte Enable low activates low order byte outputs B1-B8. In handshake mode (when MODE is HI) this pin becomes a low byte flag output.
19	$\overline{\text{HBEN}}$	Input Output	High Byte Enable. When MODE is low and $\overline{\text{CE/LOAD}}$ is low, taking High Byte Enable low activates high order byte outputs B9-B12, POL & OR. In handshake mode (when MODE is HI) this pin becomes a high byte flag output.
20	$\overline{\text{CE/LOAD}}$	Input Output	When MODE is low, taking Chip Enable/Load high disables B1-B12, POL & OR. Taking it low enables B1-B12, POL & OR if $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ are low. In handshake mode (when MODE is HI) this pin becomes a load strobe output.

PIN	FUNCTION	TYPE	DESCRIPTION
21	MODE	Input	LO = Converter in direct output mode. Makes $\overline{\text{LBEN}}$, $\overline{\text{HBEN}}$ & $\overline{\text{CE/LOAD}}$ act as inputs controlling byte outputs directly. HI = Converter in handshake mode. Makes $\overline{\text{LBEN}}$, $\overline{\text{HBEN}}$ & $\overline{\text{CE/LOAD}}$ act as outputs.
22	OSC IN	Input	Oscillator input.
23	OSC OUT	Output	Oscillator output.
24	OSC SEL	Input	Taking Oscillator Select high or leaving it open configures OSC IN, OSC OUT & BUF OSC OUT as an RC oscillator. Clock frequency = BUF OSC OUT frequency. Taking it low configures OSC IN & OSC OUT for crystal oscillators. Clock frequency = BUF OSC OUT frequency ÷ 58.
25	BUF OSC OUT	Output	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input	HI = Continuous conversions every 8192 clock pulses. LO = Converter stops in auto-zero after completing the conversion in progress.
27	SEND	Input	Indicates ability of external device to accept data when converter is in handshake mode. Connect to +5V if not used.
28	V^-		Negative supply. Nominally -5V from GND.
29	REF OUT	Output	Reference voltage output. Nominally 2.8V below V^+.
30	BUFFER	Output	Buffer Amplifier Output.
31	AUTO-ZERO		Inside foil of C_{AZ} connects here.
32	INTEGRATOR	Output	Outside foil of C_{INT} connects here.
33	COMMON		Analog Common.
34	INPUT LO		Low side of differential input.
35	INPUT HI		High side of differential input.
36	REF IN$^+$		Positive input of differential reference.
37	REF CAP$^+$		Positive side of reference capacitor.
38	REF CAP$^-$		Negative side of reference capacitor.
39	REF IN$^-$		Negative input of differential reference.
40	V^+	Input	Positive supply. Nominally +5V from GND.

Note: All digital levels are positive true.

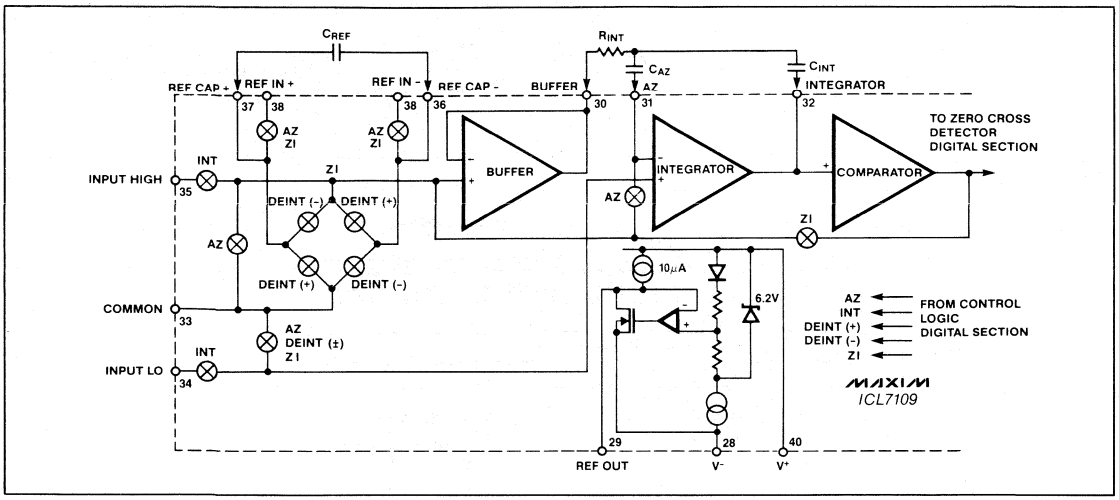

Figure 2. Analog Section

Detailed Description

Analog Section

The equivalent circuit of the Analog Section of the ICL7109 is shown in Figure 2. The circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle) when the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+. Each measurement cycle is divided into four phases as shown in Figure 3. They are:

1. Auto-Zero (AZ)
2. Signal Integrate (INT)
3. De-integrate (DE)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during Auto-zero. The inputs, In-Hi and In-Lo, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. Lastly, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy. In any event, the offset referred to the input is less than 10 μV.

Signal Integrate Phase

The internal input high (In-Hi) and input low (In-Lo) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between In-Hi and In-Lo for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. The polarity of the integrated signal is determined at the end of this phase.

De-integrate Phase

The third phase is De-integrate, also known as reference integrate. Input high is internally connected across the previously charged reference capacitor and input low is internally connected to analog Common. The polarity detection circuit connects the reference capacitor with the polarity such that the integrator output returns with a fixed slope to the zero level established in the Auto-Zero phase. The time required for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

Zero Integrator Phase

Input low is shorted to analog Common and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return rapidly to zero (See Figure 3). This phase normally lasts between 16 and 32 clock pulses but is extended to 1552 clock pulses after an overrange conversion.

This phase will remove any residual charge left on the integrator capacitor after an overload reading. This Zero Integrator phase virtually eliminates the problem of interaction or "crosstalk" between the various channels of a Maxim ICL7109 based multiple channel data acquisition system. Without the zero integrator phase, an overload on one channel would leave charge on the integrator capacitor, which would then be transferred to the autozero capacitor during the autozero cycle, resulting in an erroneous reading for the next channel that is measured after the channel with the overload.

12 Bit A/D Converter With 3-State Binary Outputs

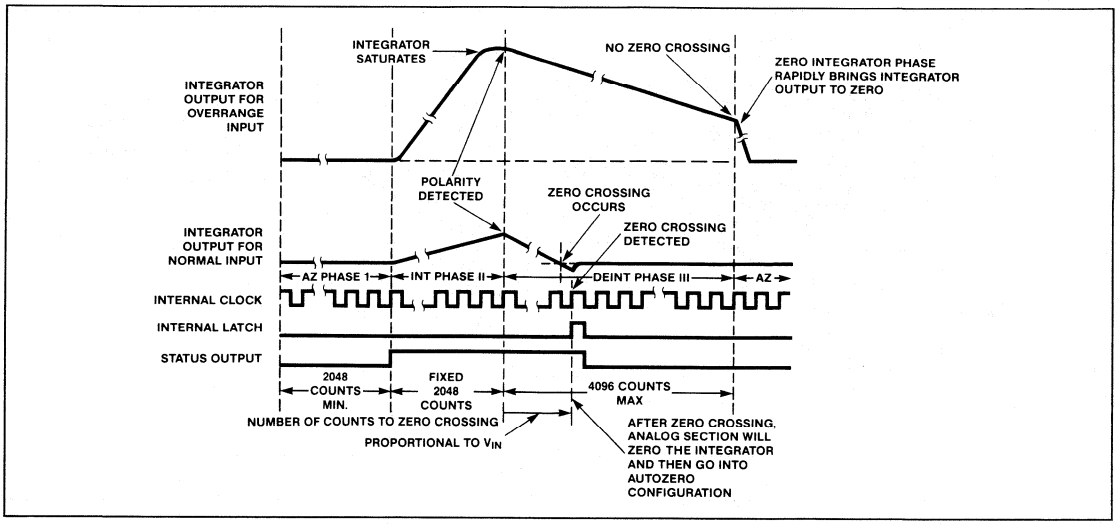

Figure 3. Conversion Timing (RUN/$\overline{HOLD}$ Pin High)

Differential Input

Differential input voltages anywhere within the common-mode range of the input amplifier can be accepted (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB typical in this range. For optimum performance the input voltage at In-Lo and In-Hi should not come within 2 volts of either the positive or negative supply. Care must be exercised to ensure that the integrator output does not saturate, since the integrator also swings with the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator positive. The integrator output swing can be reduced to less than the recommended 4V full-scale swing with little loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

The ICL7109 has been optimized for operation with analog common near digital ground. This allows for a 4V full scale integrator swing positive or negative which maximizes performance of the analog section with ±5V power supplies.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Roll over error defines this difference in reference for positive or negative input voltages. This error can be held to less than one half count for worst-case condition by using an optimum reference capacitor. (See component value selection.)

By having the reference common mode voltage near or at analog COMMON, the roll-over error from these sources is minimized.

Component Value Selection

Care must be exercised in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate for optimum performance of the analog section. The optimum values must be selected for each application.

Integrating Resistor

Both the integrator and buffer amplifier have a class A output stage with a quiescent current of 100 μA, which can supply 20 μA with negligible non-linearity. The integrating resistor should be small enough that undue leakage requirements are not placed on the PC board, but large enough to keep the output current less than 40 μA. For 2.048 volt full scale, 100kΩ is optimum and similarly a 20kΩ is optimum for a 409.6mV scale. For other full scale voltages, R_{INT} should be selected by the relation

$$R_{INT} = \frac{\text{full scale voltage (mV)}}{20\ \mu A}\ k\Omega$$

Integrating Capacitor

C_{INT} (the integrating capacitor) should be selected for maximum integrator output voltage swing without saturation of the integrator (at 0.3 volt from either supply). A ±3.5 to ±4 volt integrator output swing is ideal for the ICL7109 with a ±5 volt supplies and analog common connected to GND. Nominal values for C_{INT} and C_{AZ} are 0.15 μF and 0.33 μF, respectively, for 7½ conversions per second (61.44kHz clock frequency). These values should be changed to maintain the integrator output voltage swing, if different clock frequencies are used. The value of C_{INT} is generally given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\ \mu A)}{\text{Integrator output voltage swing (V)}}\ \mu F$$

To prevent roll-over and linearity errors a low dielectric absorption capacitor is required. Polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. Teflon™ capacitors are recommended for the military temperature range. Polypropylene and Teflon™ capacitors should give less than 0.5 count of error due to dielectric absorption even though their absorption characteristics vary somewhat from unit to unit.

Auto-Zero Capacitor

The Maxim ICL7109 has a zero integrator phase which ensures that any charge left on the integrator after an overrange reading is removed before the autozero phase is started. This zero integrator phase allows the use of larger values of autozero capacitors than allowed with other manufacturer's ICL7109s. Normally, the optimum value of the autozero capacitor is between 2 and 4 times the value of the integrator capacitor. The typical value of the autozero capacitor is 0.33 μF. Lower values of C_{AZ} increase the noise in the autozero loop; very large values will take a longer time to charge to the proper value after power-up.

The outer foil of C_{AZ} should be connected to the R_{INT}, C_{INT} summing junction and the inner foil to pin 31 for optimal rejection of stray pickup. Similarly, the inner foil of C_{INT} should be connected to the RC summing junction, and the outer foil of C_{INT} should be connected to pin 32. Above 85°C, Teflon™, or equivalent capacitors are recommended for their low leakage characteristics.

Reference Capacitor

Good results can be achieved in most applications with a 1 μF capacitor. A larger value is required to prevent roll-over error where a 409.6mV scale is used and a large common mode voltage exists (i.e., the reference low is not at analog common). The roll-over error can generally be held to one half count by 10 μF in this case. Above 85°C, Teflon™, or equivalent capacitors are again recommended for their low leakage characteristics.

Reference Voltage

An analog input of $V_{IN} = 2 \times V_{REF}$ generates a full scale output of 4096 counts. For a normalized scale, a reference of 204.8mV should be used for a 409.6mV full scale (100 μV per LSB), and 1.024V reference should be used for a 2.048V full scale (500 μV per LSB). There will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output in many applications where the A/D is sensing the output of a transducer. In a weighing system, for example, the designer could possibly want a full scale reading when the voltage from the transducer is 0.682V. The input voltage should be measured directly and a reference voltage of 0.341V should be used instead of dividing the input down to 409.6mV. 34kΩ and 0.15 μF are suitable values for the integrating resistor and capacitor. A divider on the input is thus avoided. When a zero reading is desired for non-zero input, another advantage of this system is realized. Examples might include temperature and weight measurements with an offset or tare. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. It may be more efficient, however, to perform this type of scaling or tare subtraction digitally using software in processor-based systems using the ICL7109.

Reference Sources

A major factor in the overall absolute accuracy of the converter is the stability of the reference voltage. The resolution of the ICL7109 at 12 bits is 244 ppm or one part in 4096. Therefore, a temperature difference of 3°C will introduce a one-bit error if the reference has a temperature coefficient of 80 ppm/°C (like the onboard reference). Where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made, an external high quality reference should be used.

To generate a suitable reference voltage, the ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider. This output will sink up to about 20mA without a significant output variation. A pullup bias device which sources about 10 μA is also provided. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80 ppm/°C typical. REF^+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+, and REF OUT (Pin 29) should be connected to REF^- (pin 39) when using the onboard reference. Shown in the test circuit is the circuit for a 204.8mV reference. The fixed resistor should be removed for a 1V reference, and a 25kΩ precision

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potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink sufficient current to destroy the device. By placing a 1kΩ resistor in series with pin 39, this can be avoided.

Detailed Description

Digital Section

The digital section (Figure 4) includes: 1) the clock oscillator and divider circuit; 2) a 12-bit binary counter with output latches and TTL-compatible three-state output drivers; 3) control logic; and 4) UART handshake logic.

Note: The term "clock cycles" as used in the following discussion relates to the internal clock, which is the oscillator output ÷ 58 when OSC SEL is low.

Three-State Outputs

The ICL7109 has 14 three-state outputs: 12 data bits, 1 polarity bit, and 1 overrange bit. These bits are enabled either by the CE/LOAD, LBEN and HBEN control signals (see Table 2), or by entering the Handshake mode.

CE/LOAD, LBEN, and HBEN

These three control pins can function as either inputs or outputs. In the Direct interface mode (see "Interfacing" below), these three pins are Chip Enable and Byte Enable inputs. In the Handshake mode these three pins become outputs that load data into the UART. These pins will be outputs while a handshake transfer is in progress or at any time that the Mode input is high.

Run/Hold Input

When the Run/Hold input is tied high, the ICL7109 continuously performs A/D conversions with a fixed length of 8192 clock cycles per conversion. When Run/Hold is taken low, the ICL7109 will complete the conversion in progress, then wait in the autozero phase. After the minimum autozero time has been completed, a high-going pulse on Run/Hold of at least 200 nanoseconds is required to start a new conversion; but any pulses during a conversion or up to 2048 clock cycles after Status goes low will be ignored. If the ICL7109 is holding at the end of the autozero phase, a new conversion will start and Status will go high within 7 clock cycles after Run/Hold goes high.

In addition to starting and stopping conversions, the Run/Hold pin can also be used to minimize conversion time. If Run/Hold is high, each conversion takes a full 8192 clock cycles, with the De-integrate phase taking 4096 clock cycles independent of input voltage. On the other hand, if Run/Hold is low at any time after Status goes low, the ICL7109 immediately jumps to the Auto-Zero phase rather than taking a full 4096 clock cycles for De-integrate. A simple way to ensure minimum conversion time is to drive the Run/Hold input with the Buffered Oscillator Output. When this is done, the conversion time is dependent on the input voltage: 4096 clock cycles for a zero voltage input, rising to 8192 clock cycles for full scale or overrange inputs.

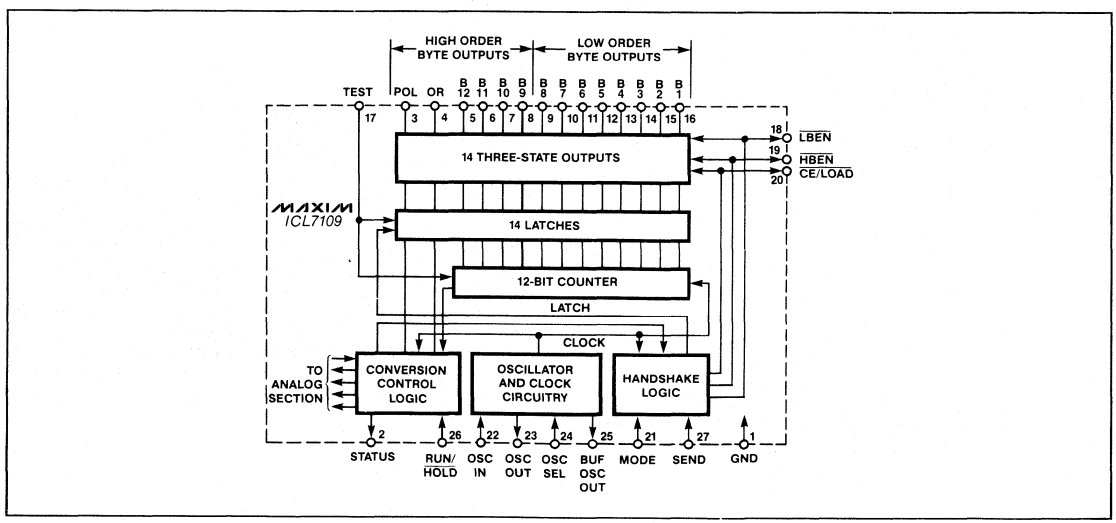


Figure 4. Digital Section

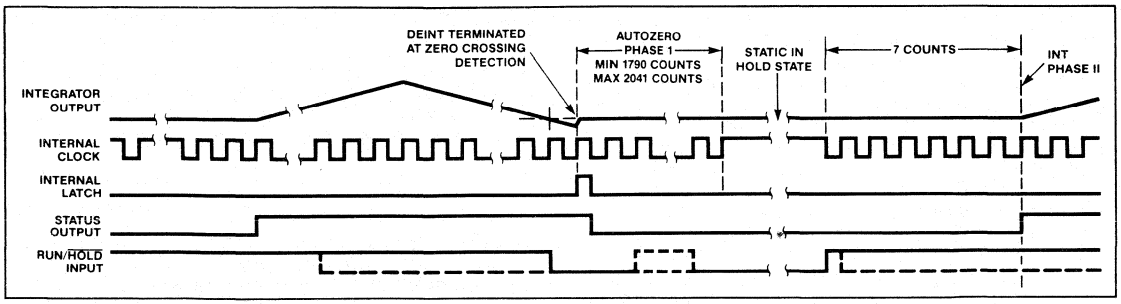


Figure 5. RUN/$\overline{HOLD}$ Operation

Mode Input

The Mode input is used to control the converter output mode. The converter is in its Direct output mode, where the output data is directly accessible under the control of the chip and byte enable inputs when the Mode pin is low or left open. (To ensure a low level when the pin is left open, this input is provided with an internal pulldown resistor.) When the Mode input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "Direct" mode. The converter will output data in the handshake mode at the end of every conversion cycle when the Mode input remains high. (See "Handshake Mode" section for more details.)

Send Input

The Send Input is a handshake control input used during handshake transfers. The use of Send to control a handshake interface is discussed in the "Interfacing" section, below.

The Maxim ICL7109 contains an improved power-up reset circuit that ensures that the ICL7109 powers up in the Direct mode if the Mode input is low, but other manufacturer's ICL7109s may power up in the Handshake mode even if the Mode input is held low. Although the Send input on the Maxim ICL7109 can be tied either high or low if only the Direct mode is used, other manufacturer's ICL7109s require that the Send input be tied high so that the ICL7109 will return to the Direct mode in 7 clock cycles if the Handshake mode is inadvertently entered on power-up.

Oscillator

The ICL7109 has a versatile three terminal oscillator that may be operated as a crystal or RC oscillator. It also may be overdriven by an external clock source. To optimize it for crystal or RC operation, the Oscillator Select input changes the internal configuration of the oscillator. The oscillator is configured for RC operation when the Oscillator Select input is high or left open (the input is provided with an internal pullup resistor), and the internal clock will be of the same phase and frequency as the signal at the Buffered Oscillator Output. (See Figure 6 for the resistor and capacitor connections.) Oscillation will occur in the circuit at a frequency given by f = 0.45/RC. The oscillator resistor should be 100kΩ. The capacitor value should be chosen such that 2048 clock periods are close to an integral multiple of the 60Hz period for optimum 60Hz line rejection, but the capacitor value should not be less than 50pF.

A feedback device and input and output capacitors are added to the oscillator when the Oscillator Select input is low. With no external components, the oscillator will function with most crystals in the 1 to 5MHz range. (See Figure 7.) A fixed ÷ 58 circuit is inserted between the Buffered Oscillator Output and the internal clock by taking the Oscillator Select input low. This division ratio provides 33.18ms integration time, by using a 3.58MHz TV crystal.

$$T = (2048 \text{ clock periods}) \times \frac{58}{3.58\text{MHz}} = 33.18\text{ms}$$

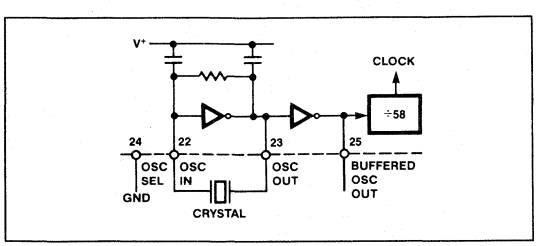


Figure 6. RC Oscillator

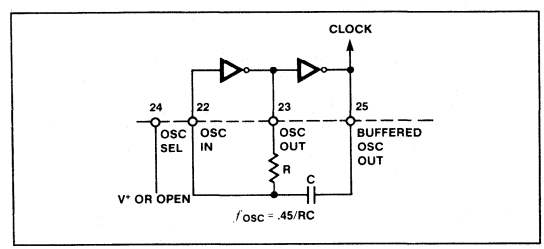


Figure 7. Crystal Oscillator

12 Bit A/D Converter With 3-State Binary Outputs

This time is quite close to 33.33ms or two 60Hz periods. The error is lower than one percent, which will yield better than 40dB of 60Hz rejection. If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the Oscillator Input, and the Oscillator Output should be left open. When Oscillator Select is left open, the internal clock will be of the same duty cycle, frequency and phase as the input signal. The clock will be the input frequency divided by 58 when Oscillator Select is at Ground. The divide by 58 circuit will operate reliably up to about 5MHz (Oscillator Select low), while the converter itself will operate at clock rates up to 2 MHz (Oscillator Select high). This implies a conversion rate of 244 conversions/sec. To operate the converter at these rates the auto-zero and integrating capacitors must be scaled using the guidelines in the Component Selection section. As the conversion rate increases, the accuracy of the converter is compromised, primarily due to noise and the delay of the comparator. If the clock period is less than the comparator delay (typically 1-3 μsec.), the low order bits become meaningless. At 2 MHz, typical readings with the inputs shorted may be 4-10 counts, rendering the 4 LSBs meaningless.

Note: At 15 conversions per second, the integration time of 2048 clock pulses equals one complete period of 60 Hz. This is therefore the maximum conversion rate that will provide 60 Hz noise rejection.

Status Output

At the end of a conversion cycle the Status output goes low, one-half clock period after new data from the conversion has been stored in the output latches. Status goes high at the beginning of Signal Integrate (Phase II). Figure 3 shows the timing details. This signal may be utilized as a flag indicating "data valid" for monitoring the status of the converter or to drive interrupts since data never changes while Status is low.

Test Input

The counter output latches are enabled when the Test input is taken to a level halfway between V^+ and Ground, allowing the counter contents to be examined. When the Test input is grounded, the internal clock is disabled and the counter outputs are all forced into the high state. The counter outputs will be clocked to the low state when the input returns to the 1/2 (V^+ -Ground) voltage (or to V^+) and one clock is applied. This facilitates testing of the counter and the output drivers.

Although the Test pin has an internal pullup, it should be tied high if not used. This ensures that high speed transitions on adjacent pins (particularly LBEN) do not inadvertently activate the test mode.

Table 2. DIRECT MODE TRUTH TABLE

$\overline{CE/LOAD}$	$\overline{LBEN}$	$\overline{HBEN}$	B1-B8	B9-B12, POL,OR
1	X	X	Hi-Z	Hi-Z
0	1	1	Hi-Z	Hi-Z
0	0	1	Data Out	Hi-Z
0	1	0	Hi-Z	Data Out
0	0	0	Data Out	Data Out

Interfacing

Direct Mode

The ICL7109 is in the Direct mode when the Mode pin is low. In this mode the output interface is a simple parallel interface with a Chip Enable ($\overline{CE/Load}$) and two byte enables ($\overline{HBEN}$ and $\overline{LBEN}$). As shown in the truth table of Table 2, the least significant 8 bits of data are enabled when both $\overline{CE/Load}$ and $\overline{LBEN}$ are low. The upper 4 bits of data, polarity, and overrange are enabled whenever $\overline{CE/Load}$ and $\overline{HBEN}$ are low. The Maxim version of the ICL7109 has significantly enhanced current sourcing capability, which enables it to rapidly drive the large capacitances often found on microcomputer busses.

In Figure 12, an approach to interfacing several ICL7109s to a bus is shown. This is achieved by using the $\overline{CE/Load}$ inputs (decoded from an address possibly) to select the desired converter, and tying the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together.

The ICL7109 can also be controlled through I/O peripheral ports, as shown in Figures 14, 15 and 16. Figures 13 through 16 are some practical circuits utilizing the parallel three-state output capabilities of the ICL7109. Shown in Figure 16 is a straightforward interface to the Intel MCS-48, -80 and -85 systems via an 8255 PPI, where the ICL7109 data outputs are active at all times. The 8155 I/O ports may be utilized in the same way. Although a read performed while the data latches are undergoing updates will lead to scrambled data, this interface can be used in a read-

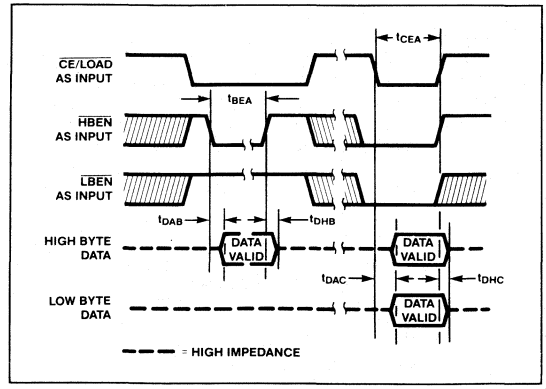


Figure 8. Direct Mode Output Timing

anytime mode. One way of solving this problem is to read the Status output as well. If it is high, read the data a second time after a delay of more than 1/2 converter clock period. If Status is still high, the first reading is correct. If Status is now low, the second reading is correct. On the other hand, the problem of timing is completely avoided by using a read-after-update sequence. (See Figure 14.) Data can be accessed by the high to low transition of the Status output driving an interrupt to the microprocessor. Figure 14 also demonstrates the Run/Hold input being used to initiate conversions under software control.

Figure 15 shows a similar interface to 650X or 680X systems. The transition of the Status output from high to low generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the Run/Hold pin through Control Register B. This application permits software-controlled initiation of conversions.

Direct interfacing to most microprocessor busses is allowed by the three-state output capability of the ICL7109. (See Figure 13 and the typical operating circuit on the first page.) It is important that the requirements for setup and hold times, and minimum pulse widths are met. There are also drive limitations on long busses that should be noted. In general, this type of interface is favored only if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can mandate several extra components. The use of interfacing devices will simplify the system in many cases.

Handshake Mode

Handshake Mode permits the interface with a number of external devices. For example, byte enables may be used as load enables or as byte identification flags, and external latches may be clocked by the rising edge of $\overline{CE}$/Load.

The handshake mode is specifically designed to directly interface the ICL7109 to industry standard UARTs, with no external logic required. The ICL7109 is in the handshake mode whenever the Mode input is high. In the handshake mode the $\overline{CE}$/Load, $\overline{LBEN}$ and $\overline{HBEN}$ pins are outputs and Send is an input. A typical UART to ICL7109 interface is shown in Figure 18, with the interface timing shown in Figures 9 through 11.

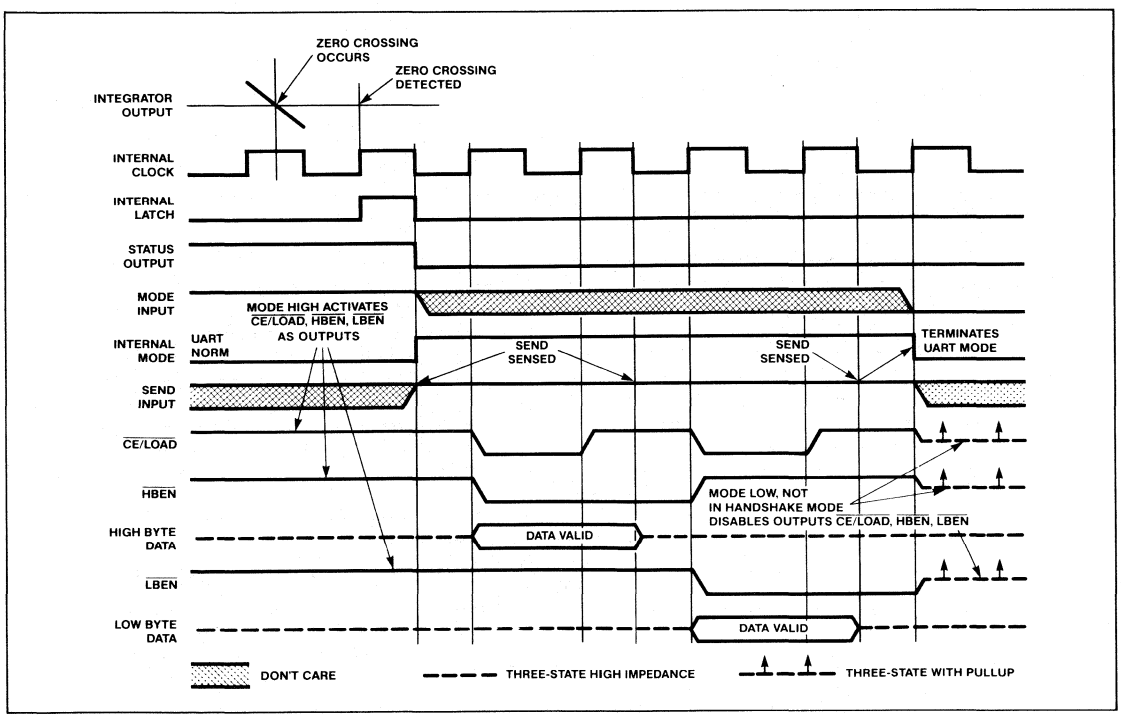


Figure 9. Handshake With Send Held Positive

12 Bit A/D Converter With 3-State Binary Outputs

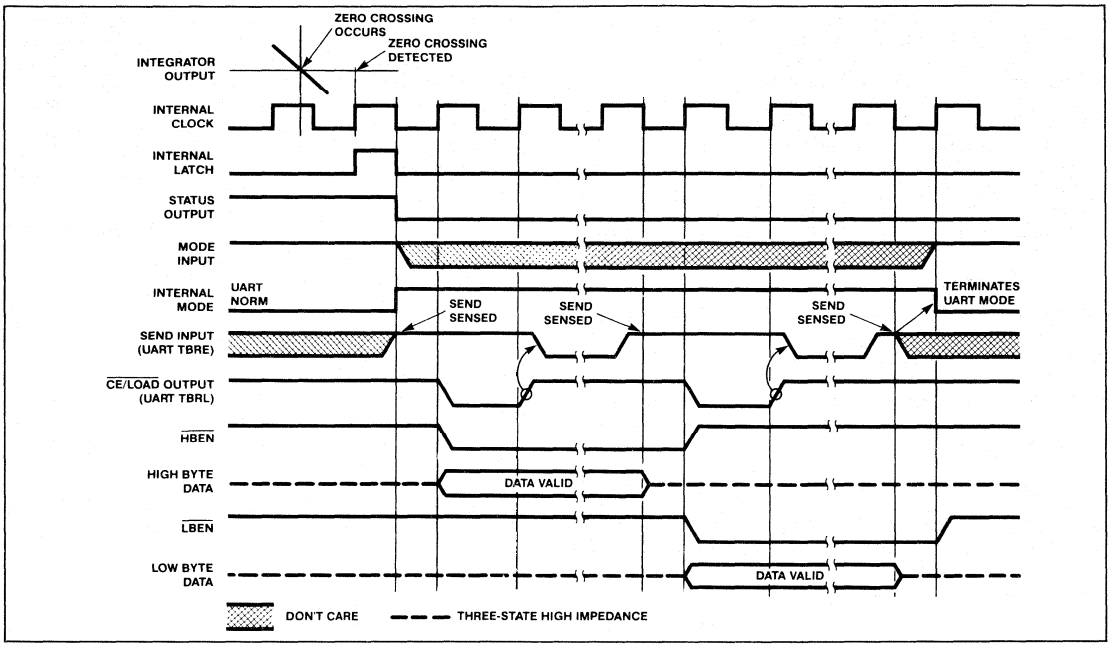


Figure 10. Handshake - Typical UART Interface Timing

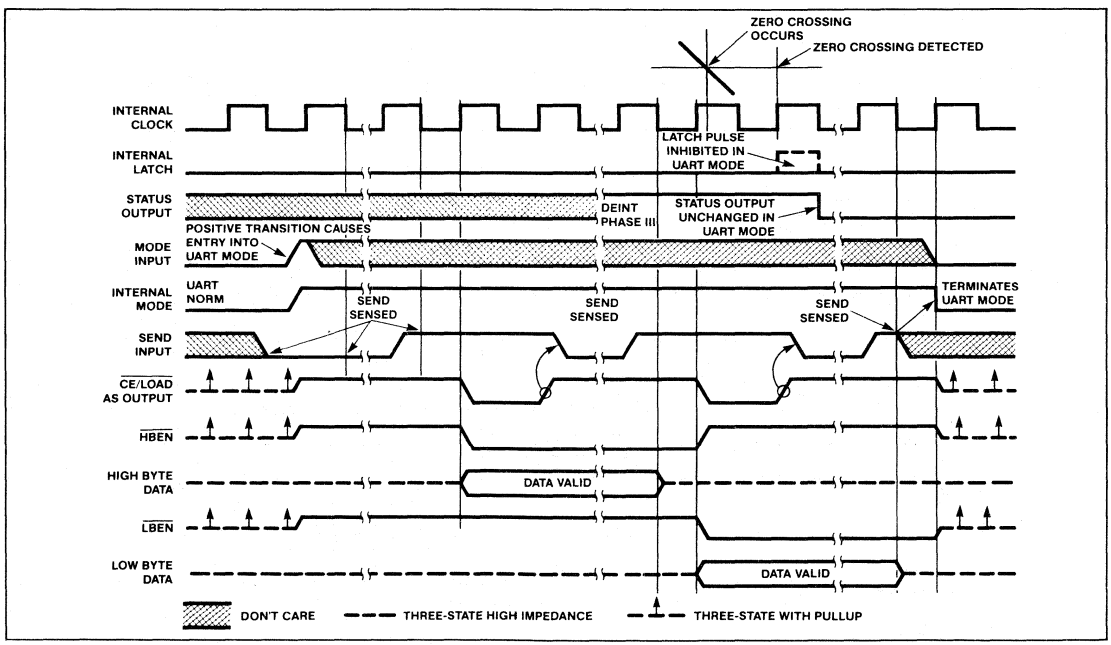


Figure 11. Handshake Triggered By Mode

When Mode is continuously held high, a new UART transmission will be started when Status goes low, provided Send is high at that time. As shown in Figure 10 the high byte of data will be written into the UART by the first pulse of $\overline{CE}$/Load. The $\overline{TBRE}$ signal of the UART will momentarily go low upon receiving the data. After the UART transfers the data to the transmitter register, the UART's $\overline{TBRE}$ output drives the ICL7109's Send input high. The ICL7109 senses the high level on the Send input and loads the low byte of data into the UART with a second pulse of $\overline{CE}$/Load. The ICL7109 continues its conversion cycles while this handshake takes place, and if the UART's $\overline{TBRE}$ has driven the ICL7109 Send input high by the end of the next conversion, the data transfer sequence will repeat. If the UARTs $\overline{TBRE}$ (and therefore the ICL7109's Send input) is low when the ICL7109 completes the next conversion, the internal latch pulse is inhibited and the data from that conversion is lost.

A handshake transfer can be initiated by a high-going pulse on the Mode pin. Upon receiving a high going pulse, the ICL7109 sets an internal Mode latch and will start a handshake transmission when Status goes low at the end of the next conversion. An alternate method of controlling the ICL7109 is to leave Mode high and initiate conversions via the Run/$\overline{Hold}$ input. With this method the ICL7109 will first make a conversion then transmit the data. Another method of initiating a transmission is shown in Figure 11. Here Mode is pulsed high while Send is low. A UART transmission is started when Send is taken high (at least 2 negative clock edges later).

The UART mode is also useful in interfacing the ICL7109 to I/O ports such as the 8255 and 6520. Figure 17 is an example of such an interface. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the Send input to the ICL7109, and using the $\overline{CE}$/Load to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1. The next conversion's result will be strobed into the port if the 8255 IBF flag is low and the ICL7109 is in handshake mode. The strobe will cause IBF to go high (Send goes low) which will prevent the ICL7109 from loading the second byte of data. The PPI will generate an interrupt. When executed, the result is that the data is read. The IBF will be reset low when the byte is read which causes the ICL7109 to sequence into the next byte. Figure 17 shows the PC7 line of the PPI connected to the Mode input of the ICL7109. If this input is tied high or left high, the data from every conversion will be sequenced into the system (provided the data access takes less time than a conversion). The output sequence can be obtained on demand by using the PC7 output to drive the Mode input. Note that the 8255 can service another peripheral device since only one port is used. The 8155 can utilize the same arrangement.

The ICL7109 is not limited to the applications described here. These examples show some of the many interfaces and uses of the ICL7109 and merely provide a point of departure for users to develop appropriate systems. Many of the suggestions made here may be combined. More specifically, the uses of the Mode, Status, and Run/$\overline{Hold}$ signals may be mixed.

Typical Applications

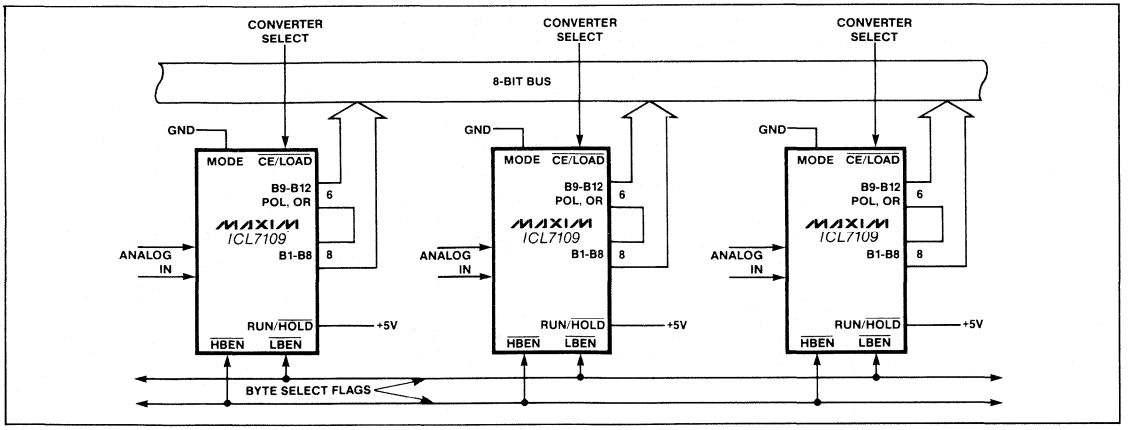


Figure 12. Three-stating several 7109's to a Bus

12 Bit A/D Converter With 3-State Binary Outputs

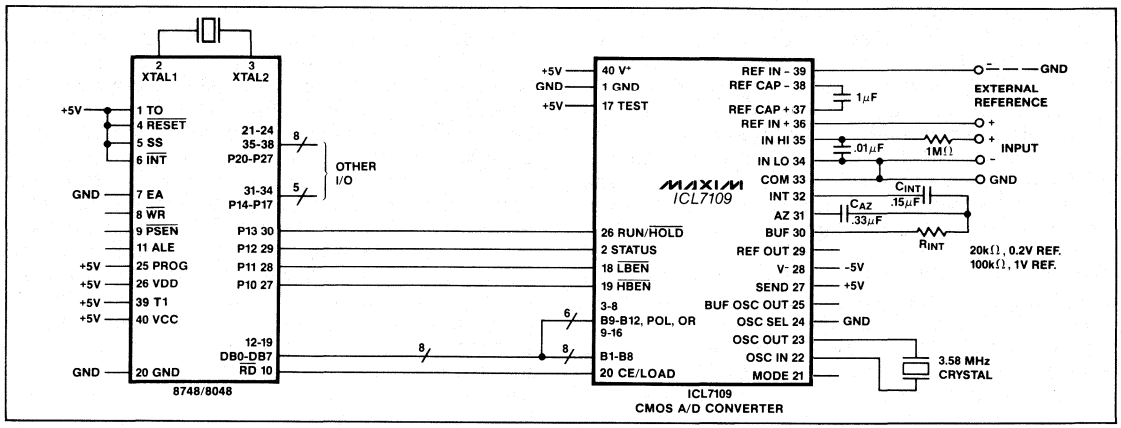


Figure 13. Typical Connection Diagram Parallel Interface with MCS-48 Microcomputer

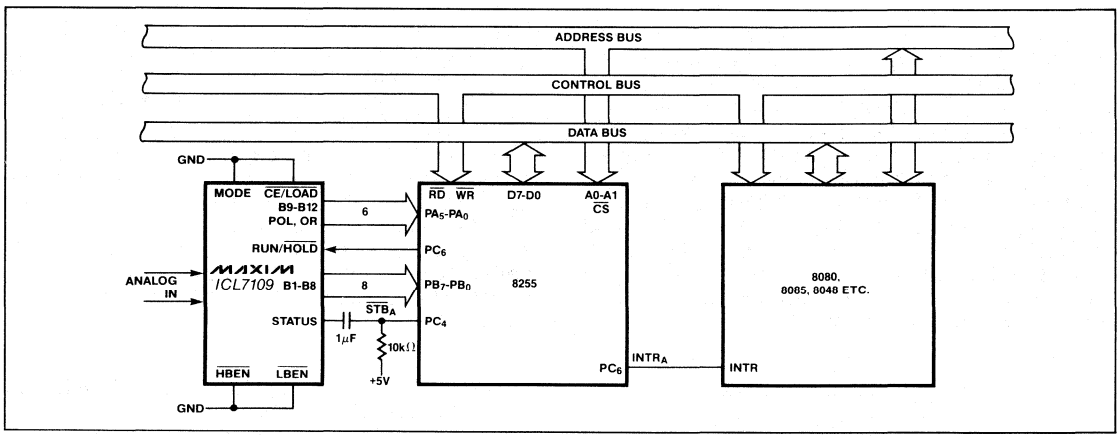


Figure 14. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputers with Interrupt

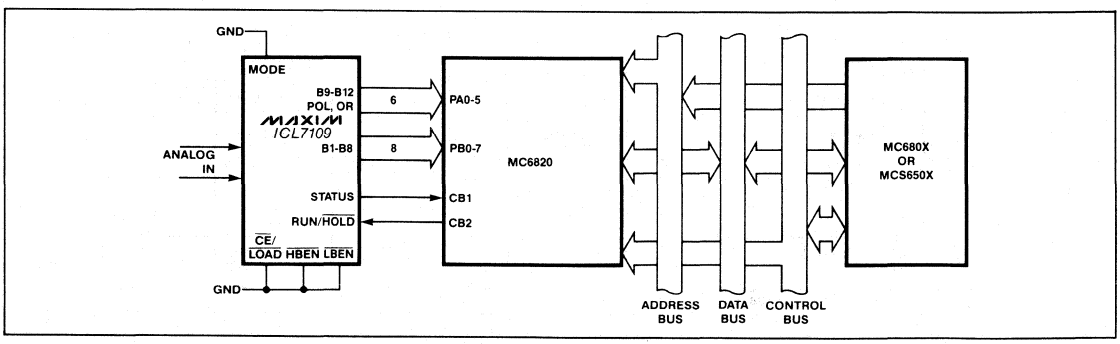


Figure 15. Full-time Parallel Interface to MS680X or MCS650X Microprocessors

12 Bit A/D Converter With 3-State Binary Outputs

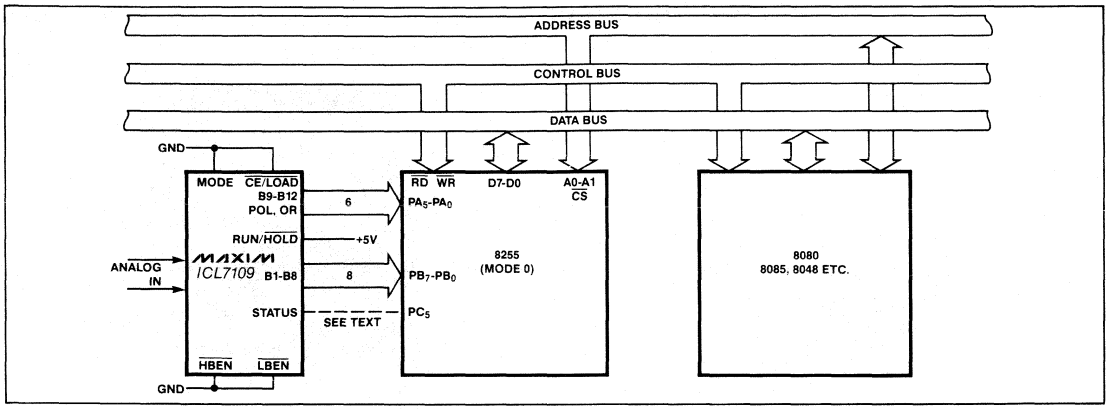


Figure 16. Full-time Parallel Interface to MCS-48, -80, -85 Microcomputer Systems

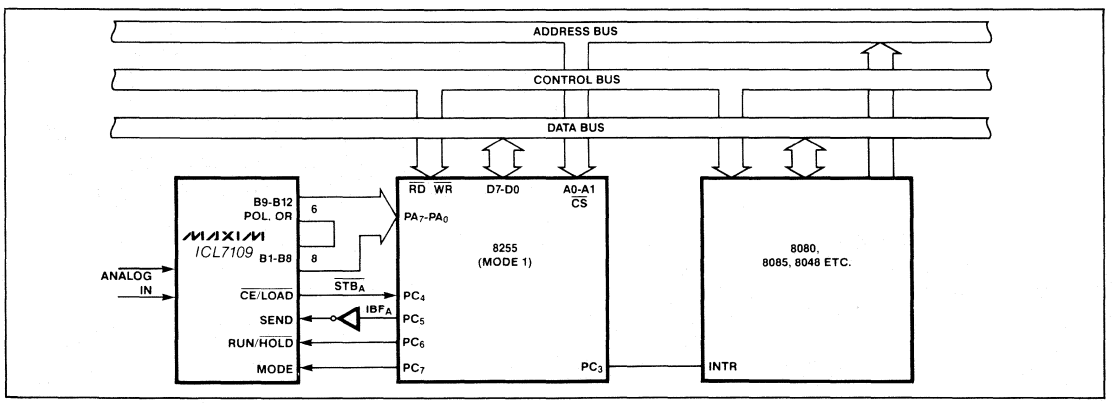


Figure 17. Handshake Interface - ICL7109 to MCS-48, -80, -85

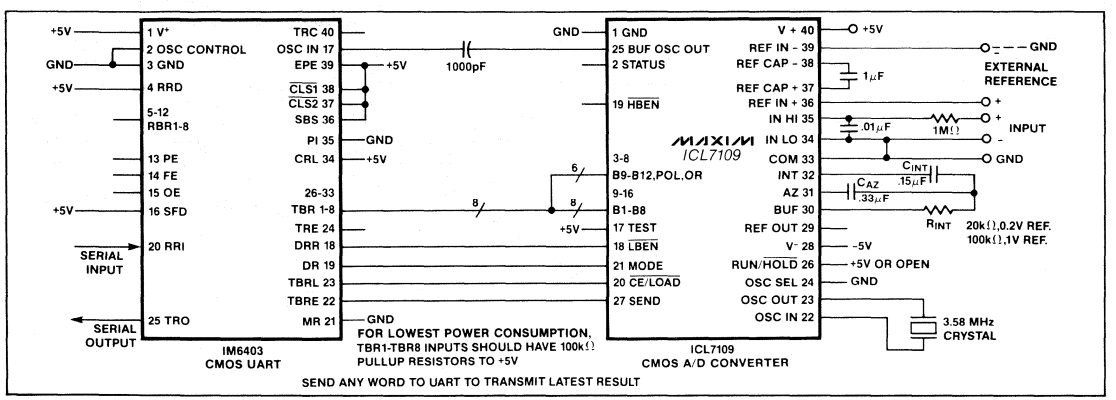
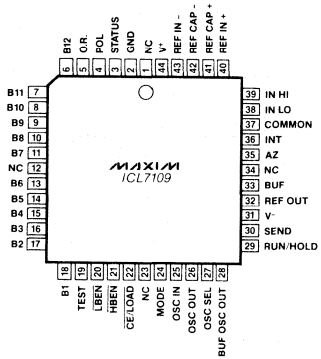


Figure 18. Typical Connection Diagram UART Interface

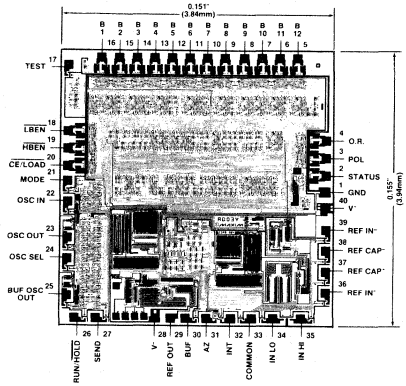
12 Bit A/D Converter With 3-State Binary Outputs

Pin Configuration

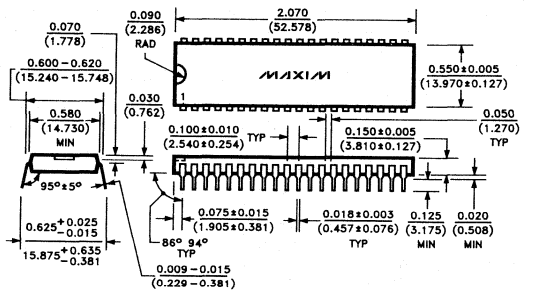


44 Lead Plastic Chip Carrier (Quad Pak)

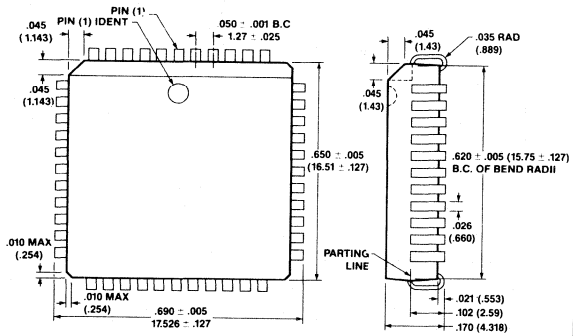
Chip Topography



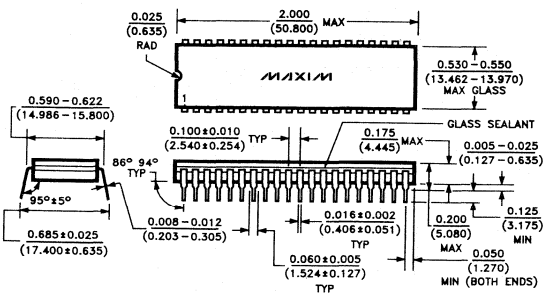
Package Information



40 Lead Plastic (PL)
θ_{JA} = 100°C/W, θ_{JC} = 45°C/W



44 Lead Plastic Chip Carrier (Quad Pack) (Q)



40 Lead Cerdip (JL)
θ_{JA} = 45°C/W

MAXIM
4-1/2 Digit Single-Chip A/D Converter with LCD Driver

General Description

The Maxim ICL7129 is a high precision monolithic 4-1/2 digit A/D converter that directly drives a multiplexed liquid crystal display. Using a novel "successive integration" technique, the ICL7129 has a ±20,000 count resolution on both 2.0000V and 200.00mV ranges. It features high impedance differential inputs, excellent differential linearity, true ratiometric operation and auto polarity. The only external active component required to make precision DVM/DPMs is a reference. The overrange and underrange outputs and the 10:1 range changing input facilitate the design of autoranging systems. The ICL7129 detects and flags a LOW BATTERY condition and also checks for continuity, giving a visual indication and a logic level output which can be used to generate an audible signal.

The ICL7129 has a fullscale accuracy of 0.005%, resolution of 10μV, zero reading drift of 0.5μV/°C, an input bias current of 10pA max, and a rollover error of less than 1 count. Maxim has reduced the noise of the ICL7129A to 3μV — significantly lower than the ICL7129.

Applications

This device can be used for a wide range of precision digital voltmeter, multimeter and panelmeter applications. Most applications involve the measurement and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

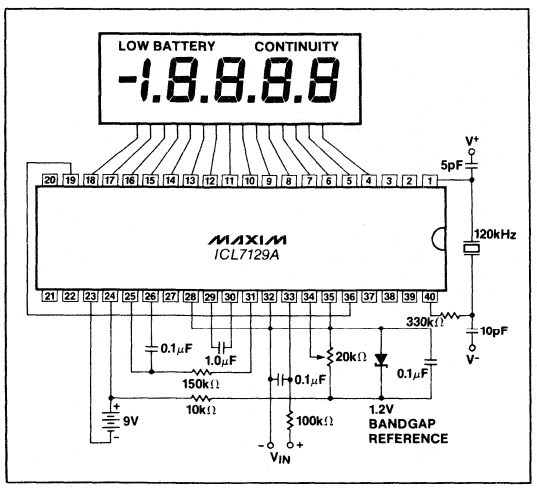
Features

- ±19,999 Count Resolution
- 3μV peak to peak noise (ICL7129A)
- Onboard Multiplexed LCD Display Driver 4-1/2 Digits, 4 Decimal Points, 3 Annunciators
- Instant Continuity Detector
- Low Battery Detector and Indicator
- Overrange/Underrange Outputs
- Precise 10:1 Range Select
- 10μV Resolution on 200mV Full Scale
- Significantly improved ESD protection
- Monolithic, Low Power CMOS Design

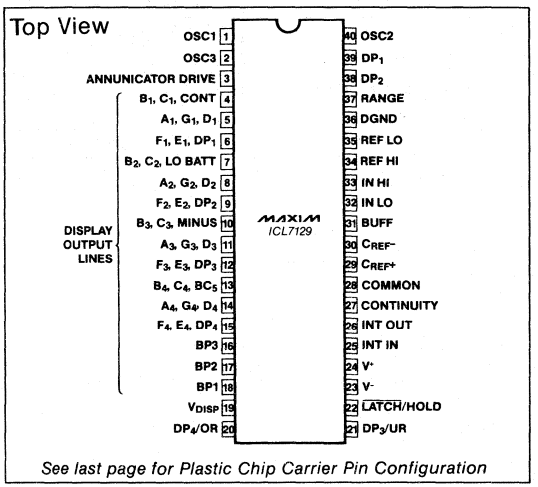
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7129CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7129CJL	0°C to +70°C	40 Lead CERDIP
ICL7129CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7129C/D	0°C to +70°C	Dice
ICL7129ACPL	0°C to +70°C	40 Lead Plastic DIP
ICL7129ACJL	0°C to +70°C	40 Lead CERDIP
ICL7129ACQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7129AC/D	0°C to +70°C	Dice

Typical Operating Circuit



Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... V^+ to DGND - 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+
Analog Input Pins
25, 29, 30 ..... V^+ to V^-

Power Dissipation (Note 2)
CERDIP package 1000mW
Plastic package 800mW
Plastic Chip Carrier
(Quad) Package 700mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Soldering Temperature (10 sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (ICL7129)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		7.0		μV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		1 3	10 40	pA pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	μA
DGND Voltage	V^+ to Pin 36	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current			1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate			100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	μA
"Weak Output" Current	Pin 20, 21	0.25	3/3	10	μA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	μA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	μA μA

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

♦ **Significantly decreased noise — 3μV** ♦ **Suitable for Ratiometric measurements**

♦ **Compensation capacitor (C_c) eliminated**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS (ICL7129A)

(V^+ to V^- = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted. Test Circuit without C_c.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Reading
Zero Reading Drift	V_{IN} = 0V, 0°C ≤ T_A ≤ +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9998	9999	10000	Reading
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ÷ V_{IN} = 0.10000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		0.5	1.0	Counts
Linearity Error	200mV Scale		0.5		Counts
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale	(V^-) + 1.5		(V^+) - 0.5	V
Noise (p-p Value not Exceeded 95% of Time)	V_{IN} = 0V 200mV Scale		3.0	Note 4	μV
Input Leakage Current	V_{IN} = 0V, IN HI V_{IN} = 0V, IN LO		13 15	20 40	pA
Scale Factor Tempco	V_{IN} = 199mV, 0°C ≤ T_A ≤ +70°C External V_{REF} = 0ppm/°C		2	5	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V	0.1	2.0		mA
COMMON Source Current	ΔCommon = -0.1V	1	9	15	μA
DGND Voltage	V^+ to Pin 36, V^+ to V^- = 9V	4.2	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	0.5	1.2		mA
Supply Voltage Range	V^+ to V^-	6	9	14	V
Supply Current Excluding COMMON Current	V^+ to V^- = 9V		1.0	1.4	mA
Clock Frequency			120	360	kHz
Display Multiplex Rate	f_{CLK} = 120kHz		100		Hz
V_{DISP} Resistance	V_{DISP} to V^+	20	50	100	kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	 400	mV mV
Pull-Down Current	Pins 37, 38, 39	0.25	2	10	μA
"Weak Output" Current	Pins 20, 21	0.25	3/3	10	μA
Sink, Source	Pin 27 Sink/Source	0.25	3/9	15	μA
Pin 22 Source Current Pin 22 Sink Current		1 0.25	40 3	100 10	μA μA

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400μA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

Note 3: All pins on Maxim's ICl7129 and ICL7129A are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883, Method 3015.1)

Note 4: The Maxim ICL7129A uses innovative noise reduction techniques to achieve a 3μV noise level. This ensures that for any specific input voltage, the ICL7129A continuously displays one number or fluctuates between two adjacent numbers. In no case will the ICL7129A display three different numbers for a constant input voltage.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

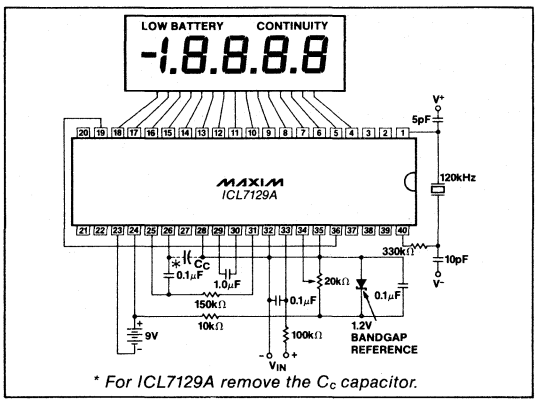


Figure 1. ICL7129/29A Test Circuit

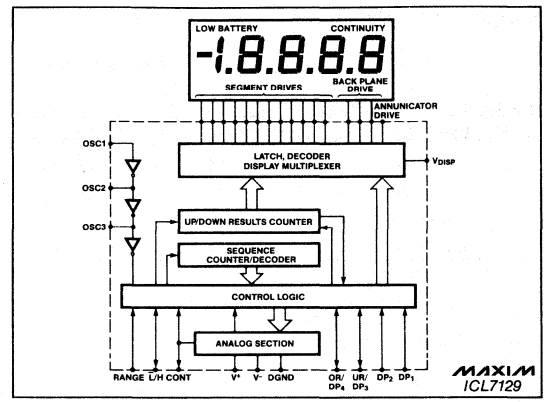


Figure 2. Simplified Block Diagram of ICL7129 Digital Section

PIN	NAME	FUNCTION
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, G_4, D_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative supply for display drivers.
20	DP_4/OR	INPUT: Turns on most significant decimal point when HI. OUTPUT: Pulled HI when result count exceeds ±19,999
21	DP_3/UR	INPUT: Turns on second most significant decimal point when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{LATCH}$/HOLD	INPUT: When floating, ICL7129 operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used as a converter status signal.

PIN	NAME	FUNCTION
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive supply for display drivers.
25	INT IN	Integrator amplifier input.
26	INT OUT	Integrator amplifier output.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc.
29	$C_{REF}+$	Positive side of external reference capacitor.
30	$C_{REF}-$	Negative side of external reference capacitor.
31	BUFFER	Buffer amplifier output.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input.
35	REF LO	Negative reference voltage input.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. Turns on least significant decimal point when HI.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Table 1. PIN ASSIGNMENTS AND FUNCTIONS

Detailed Description

Conversion Technique

The ICL7129 differs from earlier integrating A/Ds in two ways. First, it uses a variant of the dual-slope method called "successive integration". Secondly, it uses digital autozeroing rather than an analog autozero loop requiring an external autozero capacitor. Earlier converters stored an offset correction voltage on the autozero capacitor. Although this method worked well for 100μV resolution A/Ds, the autozero loop resulted in greatly increased noise in the earlier generation of integrating A/Ds, making them unsuitable for 10μV resolution systems. The ICL7129 eliminates the autozero capacitor and the noise associated with the autozero loop by performing two conversions with 5½ digit resolution. The first conversion is performed with the A/D connected to the external inputs, Input HI and Input LO. The second conversion is performed with the A/D inputs internally shorted together. The results of this second conversion, which is proportional to the A/D's offset, is digitally subtracted from the first reading to generate an offset-corrected, autozeroed measurement result.

The ICL7129 enhances the dual slope conversion technique through multiple dual slope conversions, with each successive conversion having 10 times the resolution of the preceding conversion. The key to this "successive integration" technique is the multiplication of the residual voltage on the integrator capacitor after each conversion. The ICL7129 first performs a 3½ digit dual slope conversion. The De-integration cycle terminates on the next positive clock edge after the integrator output crosses zero, leaving a small residue of voltage on the integrator capacitor. Unlike other A/D convertors, the ICL7129 multiplies this residue by a factor of 10, then performs another dual slope conversion. Since the residue on the integrator capacitor has been multiplied by 10 the resolution of the second De-integration cycle is also increased by a factor of 10, and the ICL7129 achieves 4½ digit resolution during this second De-integration cycle. The integrator capacitor residue left after the second De-integration cycle is again multiplied by 10, and the ICL7129 performs a third De-intregation cycle, this time with 5½ digit resolution.

Figure 2 shows a simplified block diagram of the ICL7129 digital section. The sequence counter/decoder section keeps track of the many separate phases required for each conversion cycle and provides timing signals to the control logic. The sequence counter runs continuously and is independent of the up/down results counter, which is activated only when the integrator is De-integrating. The data remaining in the results counter at the end of a conversion is latched, decoded and multiplexed to the liquid crystal display.

Figure 3 shows a block diagram of the analog section including all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the conversion cycle. The reference switching and input schemes are very similar to those in other less accurate, integrating A/D converters. A typical

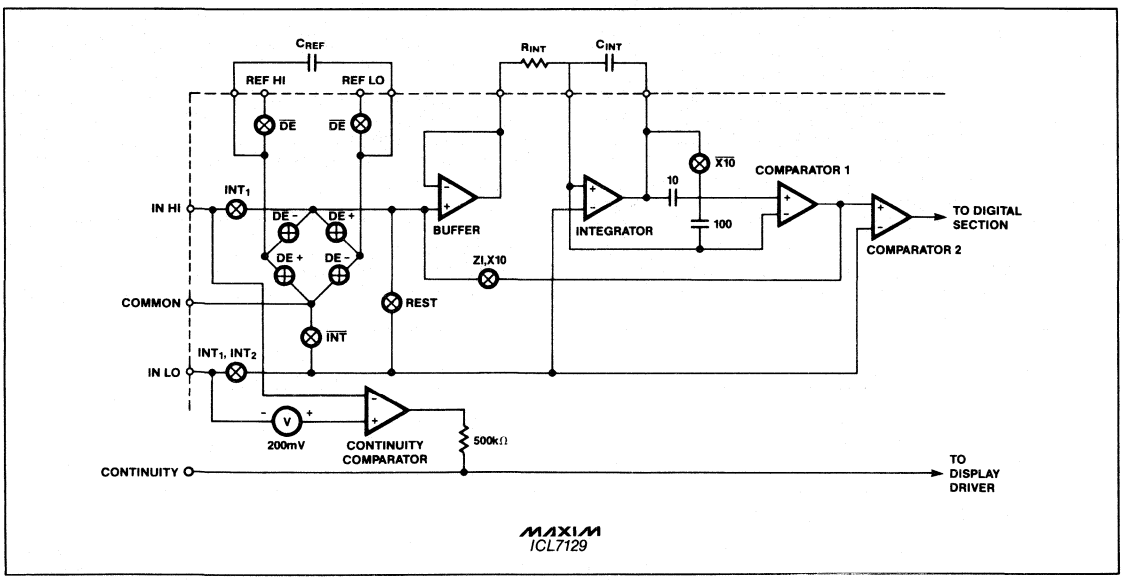


Figure 3. Analog Section Block Diagram

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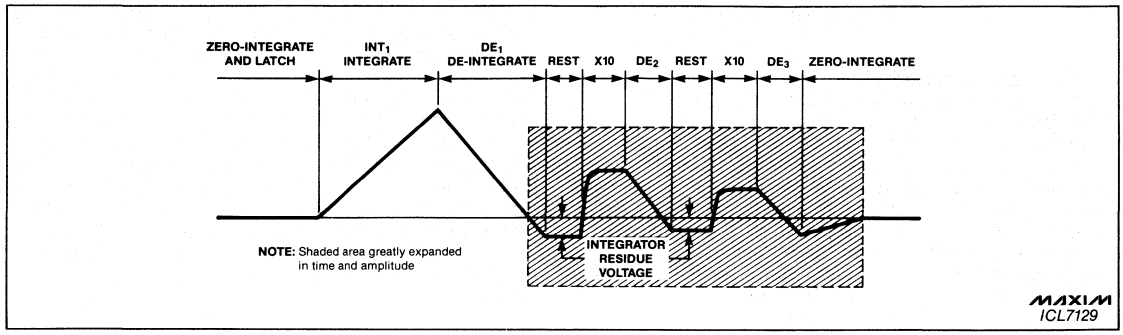


Figure 4. Integrator Waveform for a Negative Input Voltage

waveform on the integrator output is illustrated in Figure 4. INT_1 refers to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage. In the De-integrate phases, DE_1, DE_2, and DE_3, the reference capacitor is connected to the buffer amplifier and the integrator ramps back down towards Common, the level at which it started integrating. Since the De-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by -10 in the X10 phase and DE_2 begins. Similarly DE_2's overshoot is amplified by -10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This result is obtained by feeding counts to the results counter at the 3½ digit level during DE_1, to the 4½ digit level during DE_2 and the 5½ digit level during DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted together and subtracting the results from the original reading. The INT_2 switch for this phase is closed so the integrator's common mode voltage is the same as the measurement cycle, thus ensuring excellent CMRR. The data in the up/down results counter at the end of the conversion cycle, accurate to 0.005% of full scale, is sent to the onboard display driver for decoding and multiplexing.

Digital Section

Oscillator and Clock Generator

The ICL7129 has an oscillator suitable for either crystal or RC operation. The oscillator's output is internally divided by two to generate a system clock with a precise 50% duty cycle. All references to clock cycles in this data sheet refer to the system clock, which is half the frequency of the oscillator.

The crystal oscillator shown in Figure 5A is recommended for most applications. The crystal frequency should be 120kHz for maximum normal mode rejection at 60Hz, and 100kHz for maximum normal mode rejection at 50Hz.

Since an RC oscillator has more short term frequency jitter than a crystal oscillator, a crystal oscillator should be used for 4½ digit, 10μV resolution measurements.

The RC oscillator shown in Figure 5B is adequate for low resolution applications, (3½ digits at 100μV resolution). The capacitor value should be 51pF for all frequencies, and the resistor value calculated from $f_{OSC} = 0.45/RC$.

Sequence Counter and Control Logic

This section provides the signals that control the operation of the analog section. The comparator output is the only input from the analog to the digital

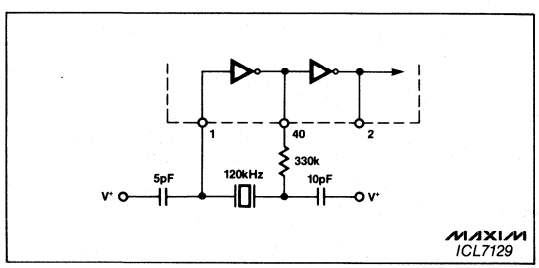


Figure 5A. Crystal Oscillator Circuits

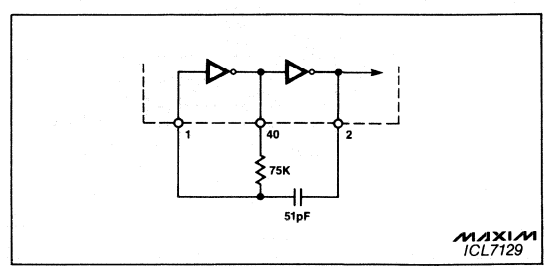


Figure 5B. RC Oscillator Circuit

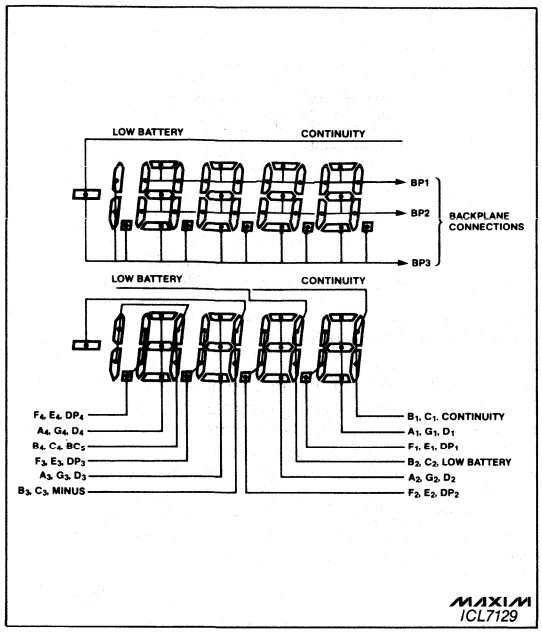


Figure 6. Triplexed Liquid Crystal Display Layout

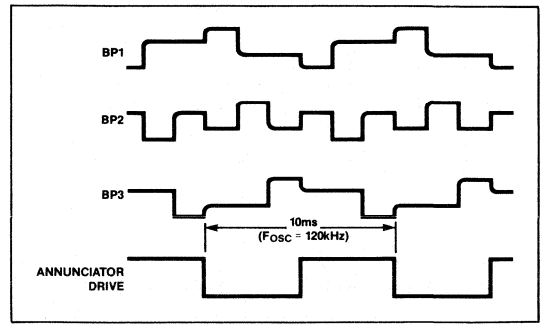


Figure 7. Backplane and Annunciator Drive Waveforms

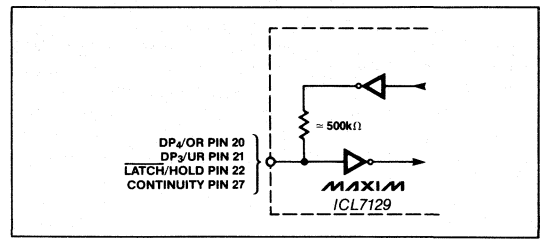


Figure 8. "Weak Output" Digital I/O Pins

section. The digital section uses the comparator output to determine the polarity of the integrator's output and to gate clock counts into the Up/Down Results Counter. The control logic also responds to the external digital inputs: Range, Hold, and Continuity. It also generates the digital outputs: Overrange, Underrange, Latch, and Continuity.

Display Driver

The ICL7129 can be used to drive a triplexed liquid crystal display with three backplanes. In addition to driving 4½—7 segment digits, the ICL7129 can directly drive the decimal points, polarity sign, "Continuity," and "Low Battery" annunciators. Figure 6 shows the assignment of the 36 display segments to the three backplanes and 12 segment drive lines. The ICL7129 divides the oscillator frequency by 1200 to generate the backplane frequency, resulting in a backplane frequency of 100Hz with a 120kHz oscillator crystal or 83.3Hz with a 100kHz crystal. Figure 7 shows the backplane and annunciator output waveforms.

Range Input

With a 1V reference, the ICL7129 has a 2V full scale when the Range input is high and a 200mV full scale when the Range input is low or open. The ICL7129 achieves a precise 10:1 change in scale factor by reducing the integration period from 10,000 clock cycles on the 200mV range to 1000 clock cycles on the 2V range.

Digital I/O Pins

Four of the ICL7129's pins are quasi-bidirectional and can be used as either inputs or outputs. As shown in Table I, DP4/OR, DP3/UR, Latch/Hold, and Continuity each have dual input/output functions. Figure 8 shows a simplified schematic of these input/output pins. Since there is approximately 500kΩ in series with these outputs, they can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. Since the output drive current is limited to only a few microamps, the outputs are easily overdriven by 4000 series CMOS when the pin is used as an input.

Latch/Hold

The Latch/Hold pin puts out a low-going pulse during the last 100 clock cycles of each conversion. This low-going pulse latches the conversion data into the onboard display driver section. The ICL7129 will not update the display, and the display will continue to show the previous reading if the Latch/Hold pin is held high. If the Latch/Hold pin is held low, the display latches are transparent and the counting of the sequence counter can be observed during the deintegrating phases.

OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are valid on the falling edge of Latch/Hold and remain in that state until the end of the next conversion cycle.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

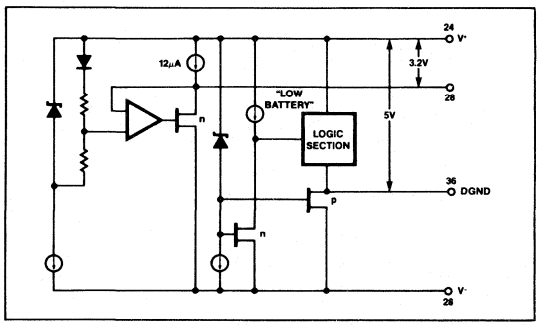


Figure 9. DGND and Common Outputs

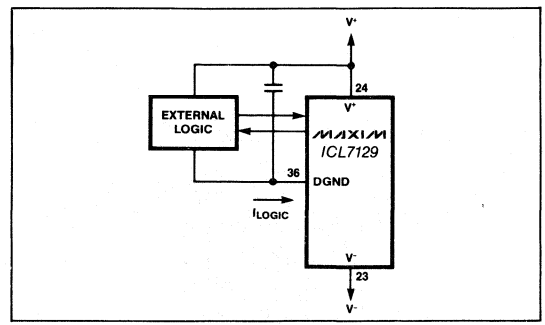


Figure 10. Using DGND as Supply Voltage for External Logic

Overrange and Underrange Outputs

The DP4/OR (Decimal Point 4/Overrange) output goes high if the measurement result is greater than ±19,999. Similarly, the DP3/UR (Decimal Point 3/Underrange) output goes high if the measurement result is less than ±1000. These signals are updated at the end of each conversion, unless Latch/Hold is held high. These pins are also inputs that control the decimal points, DP3 and DP4. A high level input on these pins turns on the decimal point segments of the display. If these decimal points are not required, they can be used as logic level controlled annunciators.

Continuity

An internal comparator with a 200mV threshhold is connected directly between the INPUT HI and INPUT LO pins of the ICL7129 (see Figure 3). The Continuity output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This activates the Continuity annunciator on the display. The Continuity annunciator can also be controlled by an external source if desired, since the Continuity pin is one of the four quasi-bidirectional pins of the ICL7129. A pull-down resistor connected between Continuity and DGND (pin 36) disables the continuity function when it is not desired.

Analog Section

Common, Digital GrouND, and Low Battery

Figure 9 shows how the Common and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes. Common can be used to set the common mode voltage in applications where the input signals float with respect to the ICL7129's power supplies, which is typical for battery-powered applications. Common can also function as a pre-regulator for an external precision reference voltage source.

The voltage between V^+ and DGND is the internal supply voltage for the logic section of the ICL7129. Both Common and DGND are capable of sinking current from external loads, but care should be taken to ensure that these outputs are not overloaded. The connection of external logic circuitry to the ICL7129 is shown in Figure 10. This connection will work provided that the supply current requirements of the logic do not exceed the 1.2mA current sink capability of the DGND pin. The buffer in Figure 10 can be used to keep the loading on DGND to a minimum if more supply current is required. COMMON can source approximately 12μA whereas DGND has no source capability.

Low Battery

The "Low Battery" annunciator of the display turns on when the supply voltage between V^+ and V^- drops below 7.2V. The exact point at which this occurs is determined by the 6.3V zener diode and threshold voltage of the n-channel transistor connected to the V^- rail shown in Figure 9.

Buffer

The ICL7129 buffer has a common mode input voltage range of V^- + 1.5V to V^+ - 0.5V and can supply up to 20μA of output current.

Integrator

The integrator can swing to within 0.3V of the supply rails while delivering 20μA of output current. It should also be noted that, unlike the ICL7129, Maxim's ICL7129A provides stable operation without the need for an additional capacitor between the Integrator Output and Common pins.

X10 Amplifier

The X10 ("times ten") amplifier provides a precise gain of -10, without using any external components. This amplifier, unique to the "successive integrator" A/D, is used to multiply the residue left on the integrator capacitor after the DE_1 and DE_2 phases.

Comparator

The comparator has the high gain and bandwidth needed to rapidly detect zero crossing. The comparator's output is used by the digital control logic to select the correct polarity for De-integration, and to gate clock pulses into the up/down results counter during the De-integration phases.

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

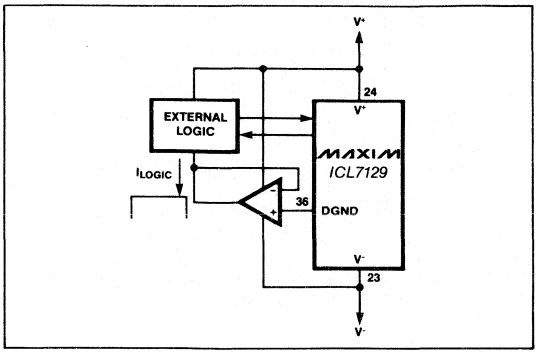


Figure 11. DGND Buffer

Component Selection

Integrating Resistor

Optimum linearity is obtained by choosing the integrating resistor value is chosen so that the buffer's maximum output current is between 5 and 20μA. The quiescent current of the buffer is 70μA, and can supply 13μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the optimum value of integrating resistor can be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{13\mu A} = \frac{2V}{13\mu A} = 150k\Omega$$

Too high a value for the integrating resistor increases the sensitivity to noise pickup and increases errors caused by stray leakage currents. Too low a value degrades integral linearity by attempting to draw more current from the buffer and integrator than they can provide without degrading linearity.

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as

$$Vswing = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

where $I_{INT} = 13\mu A$ if R_{INT} is chosen as described above and T_{INT} = 1,000 clock periods (16.7ms for 120kHz oscillator frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. The integrator will not saturate unless its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. Since Common is a approximately 3V below V^+, the integrator swing should be 2V. Substituting these values in the above formula, C_{INT} can now be calculated as:

$$C_{INT} = \frac{13.3\mu A \times 16.7ms}{2V} = 0.1\mu F$$

Too low a value for C_{INT} increases integrator swing to the point where the integrator saturates and causes integral linearity errors. Too high a value for C_{INT} reduces the integrator swing range and increases the effect of comparator noise. If a positive common mode voltage is applied to IN LO the value of C_{INT} must be reduced to keep the integrator output voltage at least 1V below V^+.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the Input HI is a good indication of the amount of dielectric absorption in the integrator capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon™ capacitors. In less critical applications polystyrene and polycarbonate capacitors may also be used.

Reference Capacitor

The reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are required only where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in digital multimeters.

The reference capacitor must be a low leakage capacitor since it stores the reference voltage while floating during both the Integrate and De-integrate phases. Any leakage or charge loss during these phases causes a change in the scale factor of the ICL7129. Low cost film capacitors such as polyester or polystyrene are suitable for most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. In most applications the Ref Lo Input terminal is connected to Common, and the Ref Hi Input is 1V above Common. During the integration and idle phases the reference capacitor is connected to the Reference Inputs (C_{REF}^+ to Ref Hi and C_{REF}^- to Ref Lo). At the end of the integration phase the comparator determines the polarity at the integrator output and the digital section closes analog switches so that the reference capacitor is connected to Common and the buffer input with a polarity such that the integrator output will return toward Common during the De-integrate phase. A negative input signal during the integrate phase drives the integrator output positive and the ICL7129 digital section will connect the C_{REF}^- terminal to Common during the De-integrate phase. Since the C_{REF}^- terminal was also connected to Common during the Integrate phase, the C_{REF} terminals do not change voltage during the transition from Integrate phase to De-integrate phase. If, however, the input voltage during the Integrate phase is positive, the ICL7129 digital section will connect the Ref Cap$^+$ terminal to Common. In this case the two terminals of

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

the reference capacitor both move 1V more negative. Any stray capacitance on the reference capacitor terminals must also be charged during the 1V movement, thereby reducing the voltage on the reference capacitor and changing the scale factor for positive input voltages. This error, called "rollover error" can be reduced to less than 1 count by using a reference capacitor value of 1μF or greater.

Crystal Oscillator Components

The ICL7129 crystal oscillator is designed to work with tuning fork type crystals such as the Statek CX-1V series. The two capacitors are not critical components and can be the low cost disc ceramic type. The crystal frequency should be 120kHz to reject 60Hz normal mode signals and 100kHz to reject 50Hz normal mode signals. With these crystal frequencies the integration will be 10 cycles of the 60/50Hz signal on the 200mV range and 1 cycle on the 2V range. There is no single oscillator frequency that results in good normal mode rejection of both 50Hz and 60Hz on the 2V range, but a 200kHz oscillator frequency will reject both 50Hz and 60Hz on the 200mV scale.

Component Manufacturers

The following list of component suppliers is intended to be of assistance in identifying suitable external components for use with the ICL7129. This list is not intended to be comprehensive, nor does it constitute an endorsement by Maxim of the companies listed.

Triplexed Liquid Crystal Displays

Epson America, Inc., Torrance, CA.
(213) 373-9511
Part #: LD-H7960A

Crystaloid, Inc., Hudson, OH
(216) 655-2429

Hamlin, Inc., Lake Mills, WI
(414) 648-2361

UCE, Inc., Norwalk, CT
(203) 838-7509

Display Mounting Bezels

Techknits, Inc., Cranford, N.J.
(201) 272-5500

Conductive Rubber Technology, Santa Barbara, CA.
(805) 969-5807

Crystals

Statek, Inc., Orange, CA
(714) 639-7810
Part #: CX-1V 120C

Saronix, Inc., Palo Alto, CA
(415) 856-6900

Polypropylene Capacitors

West Lake Capacitors, West Lake Village, CA
(818) 889-4120

Seacor, Inc., Westwood, N.J.
(201) 666-5600

TRW Capacitors, Ogallala, NE
(308) 284-3611

Sprague Electric Co., North Adams, MA
(413) 664-4411

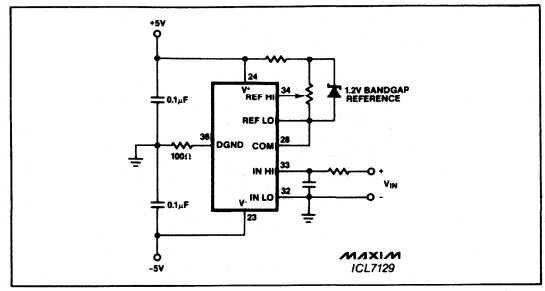


Figure 12. Powering the ICL7129 from +5V and -5V Power Supplies

Applications

Power Supply

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies.

The standard battery connection using a 9V battery is shown in the Typical Operating Circuit on the front page of this data sheet.

Figure 12 shows the power connection for systems with +5V and -5V supplies. Note that measurements are given with respect to ground. COMMON is not connected to INPUT LO and is used only as a pre-regulator for the external voltage reference. Digital ground of the ICL7129 (DGND, pin 36) is not directly connected to power supply ground. The ICL7129's digital inputs have protective diodes to DGND and should not be driven to any voltage below DGND. This problem is handled by placing a 100Ω resistor between the ICL7129's DGND terminal and the ±5V system's digital ground, which pulls down the ICL7129's DGND terminal if it reaches a voltage more positive than the ±5V system's digital ground. This prevents the forward biasing of the input protection diodes. If DGND voltage is more negative than the system digital ground the 100Ω resistor will limit the amount of current that DGND sinks.

A power supply with single polarity can be used to power the ICL7129 in applications where battery operation is not convenient or appropriate. Measurements must be made with respect to COMMON or some other voltage within the ICL7129's input common mode range.

Voltage References

The Common output has a typical temperature coefficient of ±80ppm/°C. Since the ICL7129 has a resolution of 1 count in 20,000 or 50ppm, a precision external reference is needed unless the ambient temperature is held constant. The diagram of the Typical Operating Circuit on the front page of this data sheet shows a 1.2V bandgap voltage source used as the reference for the ICL7129, with Common used only as a pre-regulator for the bandgap reference. The ICL7129

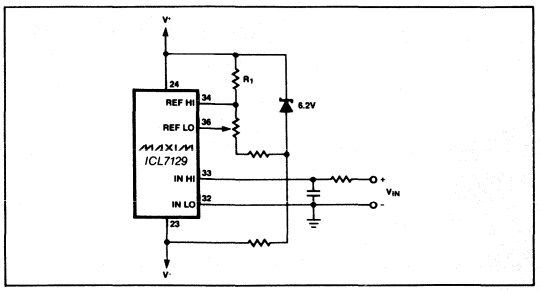


Figure 13. Using a 6.2V Reference Diode with the ICL7129

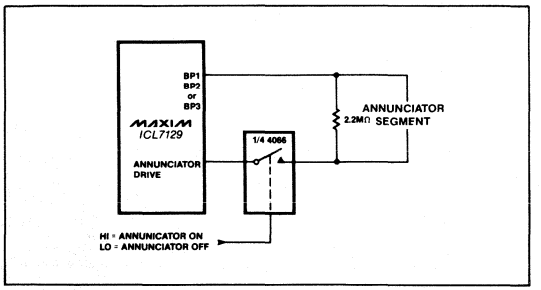


Figure 14. Externally Controlled Annunicators

reference voltage is approximately 1.000V for both 2V and 200mV full-scale operation. To trim the reference voltage, first apply a precise 1000.05mV input voltage, then adjust the reference voltage until the display reading alternates equally between 10000 and 10001.

Figure 13 shows the ICL7129 with an external 6.8V zener reference voltage.

Annunciator Drivers

The Annunciator Drive output is a square wave at the backplane frequency, swinging from V^+ to V_{DISP}. Any segment connected to Annunciator Drive will be turned on, regardless of which backplane drives that segment. Figure 14 shows how to control annunciator segments with external logic levels.

Display Voltage Compensation

An adequate display can be obtained in most applications by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is expected, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers usually specify the temperature variation of the LCD threshold voltage, which is approximately 1/3 of the optimum peak display voltage. The peak display voltage is equal to ($V^+ - V_{DISP}$), so a typical -4mV/°C temperature coefficient of an LCD threshold corresponds to a +12mV/°C temperature coefficient at the V_{DISP} pin. Two circuits that can be adjusted to give a temperature compensation of approximately +12mV/°C at V_{DISP} are shown in Figure 15. The diode between DGND and V_{DISP} should have a low turn-on voltage to ensure that V_{DISP} is never driven more than 300mV negative with respect to DGND.

Input Protection

The input pins of the ICL7129 have protection diodes built in to protect it from electrostatic discharges (ESD) of up to 2000V (Mil Standard 883, Method 3015.1 test circuit). These diodes also protect the ICL7129 from excessive input voltage overload in multimeter circuits, provided that the current into these diodes is limited to less than 1mA. The ICL7129 will therefore be fully protected for input voltages up to 1000V if the input current limiting resistor is 1MΩ.

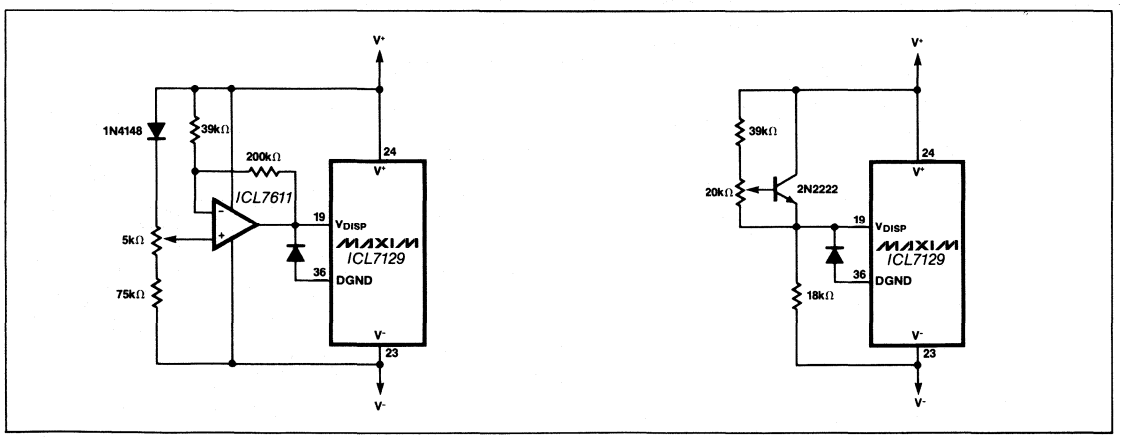
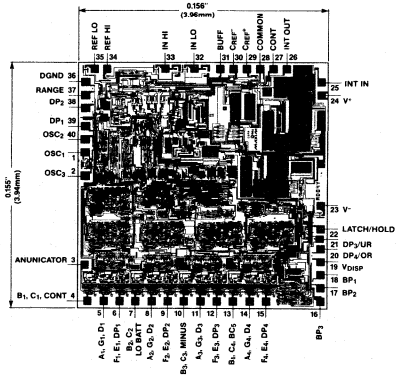


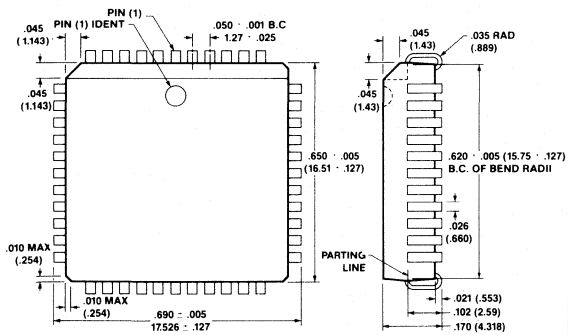
Figure 15. V_{DISP} Temperature Compensation

4-1/2 Digit Single-Chip A/D Converter with LCD Driver

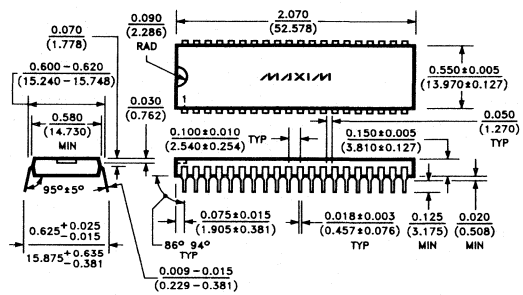
Chip Topography



Package Information

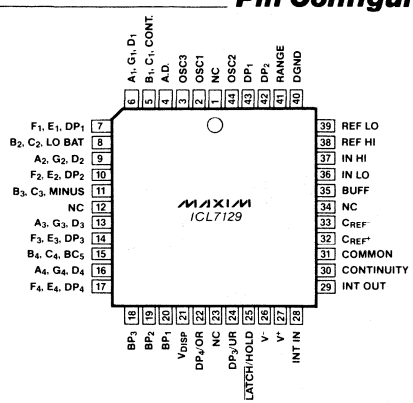


44 Lead Plastic Chip Carrier (Quad Pack) (Q)

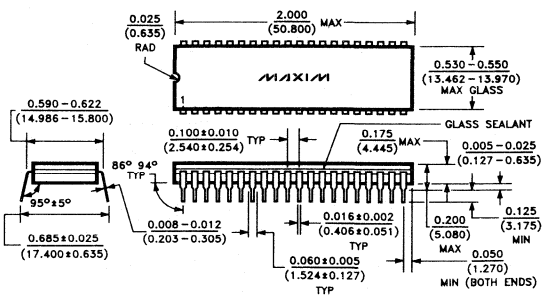


40 Lead Plastic (PL)
θ_{JA} = 100°C/W, θ_{JC} = 45°C/W

Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pak)



40 Lead Cerdip (JL)
θ_{JA} = 45°C/W

4½ Digit A/D Converter with Multiplexed BCD Outputs

General Description

The Maxim ICL7135 is a high precision monolithic 4½ digit A/D converter. Dual slope conversion reliability is combined with ±1 in 20,000 count accuracy and a 2.0000V full scale capability. It features high impedance differential inputs, nearly ideal differential linearity, true ratiometric operation, auto zero and auto-polarity. The multiplexed BCD outputs and digit drivers provide easy interface to external display drivers like the Maxim ICM7211A. The only other external components needed to make precision DVM/DPMs are a reference and a clock. For more complex systems the BCD outputs are enhanced by STROBE, OVERRANGE, UNDERRANGE, RUN/HOLD and BUSY lines providing easy interface to microprocessors and UARTs. This interfacing capability makes the ICL7135 an ideal device for use in microprocessor based data acquisition and control systems.

The ICL7135 has auto-zero accuracy better than 10μV, zero drift of 0.5μV/°C, input bias current of 10pA max. and rollover error of less than 1 count.

Features

- **Improved 2nd Source (See our "Maxim Advantage™" Page 3)**
- **±20,000 Count Resolution**
- **Guaranteed ±1 Count accuracy**
- **Over-range, under-range signals for auto-range capability**
- **Easy interface to UARTs and μPs**
- **TTL compatible, Multiplexed BCD outputs**
- **True differential input. Zero reading guaranteed for 0 volt input**
- **True polarity at zero for precise null detection**
- **Monolithic CMOS design**

Applications

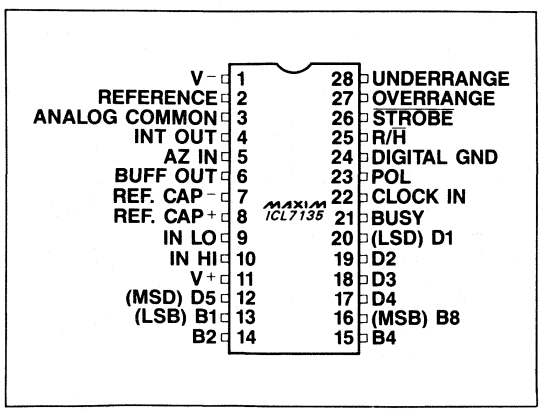
This device is used in a wide range of measurement applications involving the manipulation and display of analog data:

Pressure	Weight
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

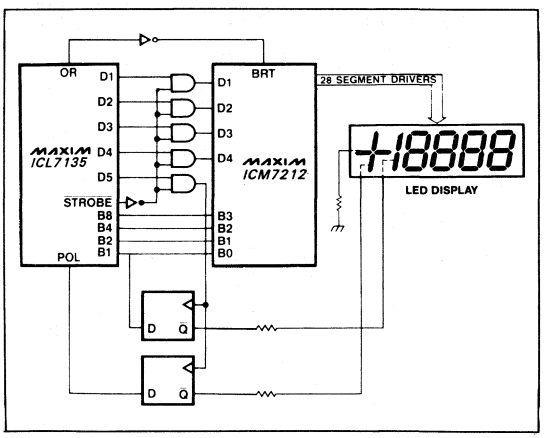
Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7135CJI	0°C to 70°C	28 Lead CERDIP
ICL7135CPI	0°C to 70°C	28 Lead Plastic DIP
ICL7135CQ	0°C to 70°C	28 Lead Plastic chip carrier
ICL7135C/D	0°C to 70°C	Dice

Pin Configuration



Typical Operating Circuit



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit A/D Converter with Multiplexed BCD Outputs

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 2)
- CERDIP Package 1000mW
- Plastic Package 800mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Supply Voltage V+ ..... +6V
V− ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Gnd to V+

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ICL7135 ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

		CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG (Note 1) (Note 2)		Zero Input Reading		$V_{IN} = 0.0V$ Full Scale = 2.000V	−0.0000	±0.0000	+0.0000	Digital Reading
		Ratiometric Reading (2)		$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.9998	+0.9999	+1.0000	Digital Reading
		Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
		Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
		Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	Digital Count Error
		Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$ Full Scale = 2.000V		15		μV
		Leakage Current at Input	I_{ILK}	$V_{IN} = 0V$		1	10	pA
		Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le 70°C$		0.5	2	μV/°C
		Scale Factor Temperature Coefficient (3)	TC	$V_{IN} = +2V$ $0° \le T_A \le 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL	INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH} V_{INL} I_{INL} I_{INH}	 $V_{IN} = 0$ $V_{IN} = +5V$	2.8	2.2 1.6 0.02 0.1	 0.8 0.1 10	V mA μA
	OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5 BUSY, STROBE OVER-RANGE, UNDER-RANGE POLARITY	V_{OL} V_{OH} V_{OH}	$I_{OL} = 1.6mA$ $I_{OH} = -1mA$ $I_{OH} = -10\mu A$	 2.4 4.9	0.25 4.2 4.99	0.40 	V V V
	SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
		−5V Supply Range	V^-		−3	−5	−8	V
		+5V Supply Current	I^+	$f_c = 0$		1.1	3.0	mA
		−5V Supply Current	I^-	$f_c = 0$		0.8	3.0	
		Power Dissipation Capacitance	C_{PD}	vs. Clock Freq		40		pF
	Clock	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" below for limitations on the clock frequency range in a system.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

4½ Digit A/D Converter with Multiplexed BCD Outputs

- **Guaranteed 2mA Max Supply Current**
- **Key Parameters Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Low Noise**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec

	Characteristics	Symbol	Conditions	Min	Typ	Max	Units
ANALOG	**Zero Input Reading**		**$V_{IN} = 0.0V$, Full Scale = 2.000V $0° \le T_A \le +70°C$**	**−0.0000**	**±0.0000**	**+0.0000**	**Digital Reading**
ANALOG	**Ratiometric Reading (Note 2)**		$V_{IN} = V_{REF}$, Full Scale = 2.000V $T_A = 25°C$	+0.9998	+0.9999	+1.0000	**Digital Reading**
			$0° \le T_A \le +70°C$	**+0.9995**	**+0.9999**	**+1.0005**	
ANALOG	Linearity over ± Full Scale (error of reading from best straight line)		$-2V \le V_{IN} \le +2V$		0.5	1	Digital Count Error
ANALOG	Differential Linearity (difference between worse case step of adjacent counts and ideal step)		$-2V \le V_{IN} \le +2V$		.01		LSB
ANALOG	Rollover error (Difference in reading for equal positive & negative voltage near full scale)		$-V_{IN} = +V_{IN} \approx 2V$		0.5	1	Digital Count Error
ANALOG (Note 1) (Note 2)	Noise (P-P value not exceeded 95% of time)	e_n	$V_{IN} = 0V$, Full Scale = 2.000V		15		μV
ANALOG (Note 1) (Note 2)	**Leakage Current at Input**	**I_{ILK}**	$V_{IN} = 0V$ $T_A = 25°C$		1	10	pA
ANALOG (Note 1) (Note 2)			**$0° \le T_A \le +70°C$**			**250**	**pA**
ANALOG (Note 1) (Note 2)	Zero Reading Drift		$V_{IN} = 0V$ $0° \le T_A \le +70°C$		0.5	2	μV/°C
ANALOG (Note 1) (Note 2)	Scale Factor Temperature Coefficient (Note 3)	TC	$V_{IN} = +2V$ $0° \le T_A \le +70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
INPUTS	Clock In, Run/$\overline{Hold}$	V_{INH}	$0° \le T_A \le +70°C$	2.8	2.2		V
		V_{INL}	$0° \le T_A \le +70°C$		1.6	0.8	V
		I_{INL}	$V_{IN} = 0$ $0° \le T_A \le +70°C$		0.02	0.1	mA
		I_{INH}	$V_{IN} = +5V$ $0° \le T_A \le +70°C$		0.1	10	μA
DIGITAL OUTPUTS	All Outputs B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OL}	$I_{OL} = 1.6mA$		0.25	0.40	V
		V_{OH}	$I_{OH} = -1mA$	2.4	4.2		V
	BUSY, $\overline{STROBE}$ OVER-RANGE, UNDER-RANGE POLARITY	V_{OH}	$I_{OH} = -10\mu A$	4.9	4.99		V
DIGITAL SUPPLY	+5V Supply Range	V^+		+4	+5	+6	V
DIGITAL SUPPLY	−5V Supply Range	V^-		−3	−5	−8	V
DIGITAL SUPPLY	**+5V Supply Current**	**I^+**	**$f_C = 0$ $T_A = 25°C$**		**1.1**	**2.0**	**mA**
DIGITAL SUPPLY			**$0° \le T_A \le +70°C$**			**3.0**	**mA**
DIGITAL SUPPLY	**−5V Supply Current**	**I^-**	**$f_C = 0$ $T_A = 25°C$**		**0.8**	**2.0**	**mA**
DIGITAL SUPPLY			**$0° \le T_A \le +70°C$**			**3.0**	**mA**
DIGITAL SUPPLY	Power Dissipation Capacitance	C_{PD}	(Note 5)		40		pF
CLOCK	Clock Freq. (Note 4)			DC	2000	1200	kHz

Note 1: Tested in 4½ digit (20,000 count) circuit shown in Fig. 1, clock frequency 120kHz.

Note 2: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

Note 3: The Temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

Note 4: This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Clock Frequency" below for limitations on the clock frequency range in a system.

Note 5: +5V Supply current for $f_c \neq 0$ is $I^+ = I^{+}_{(f_c = 0)} + C_{PD} \times 5V \times f_c$.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

4½ Digit A/D Converter with Multiplexed BCD Outputs

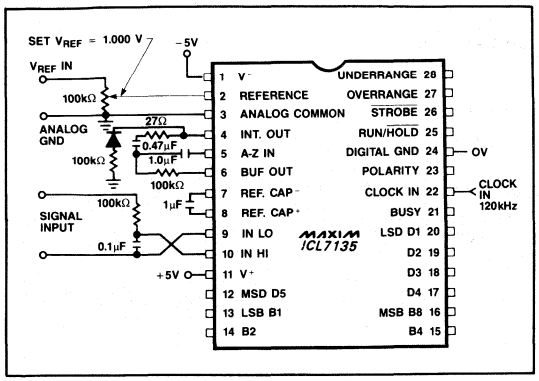


Figure 1. ICL7135 Test Circuit

Detailed Description

General Operation

The ICL7135 is divided into an Analog section and a Digital section. The digital section includes the counters, input and output interfaces, and control logic which controls the timing of each measurement cycle. Each measurement is divided into four phases: 1) auto-zero (AZ), 2) signal integrate (INT), 3) reference deintegrate (DE), and 4) zero integrator (ZI). The digital section controls the operation of the analog section during each of these phases, using counters and the state of the comparator to determine when to start each of the four phases.

Auto-Zero Phase

During auto-zero Input HI and Input LO are disconnected from the input pins and are internally shorted to Analog COMMON. The output of the comparator is connected to the inverting input of the Integrator, and at the same time the non-inverting input of the integrator is connected to the input of the buffer. This feedback loop charges the autozero capacitor, C_{AZ}, to compensate for the offset voltages of the buffer amplifier, integrator, and comparator. Also during auto-zero, the reference capacitor is connected to the voltage reference and is charged to the reference voltage. The auto-zero cycle is a minimum of 9800 clock cycles, except after an over-range reading. After an over-range, the extended zero integrate phase reduces the auto-zero phase to 3800 clock cycles.

Signal Integrate Phase

At the end of the auto-zero phase the auto-zero loop is opened, and the Input High and Input Low are switched to the external pins IN-HI and IN-LO. The analog section integrates the differential voltage between Input High and Input Low. The differential voltage must be within the ICL7135's common mode range. The voltage on the integrator capacitor at the end of signal integrate is directly proportional to the differential voltage between Input High and Input Low, and is also directly proportional to the length of the signal integrate phase. The signal integrate phase lasts precisely 10,000 clock cycles. At the end of this phase the input signal polarity is determined.

De-Integrate Phase

At the end of signal integrate, Input High and Input Low are disconnected from the external pins. The integrator non-inverting input pin is then internally connected to Analog Common and the buffer input is connected to one side of the reference capacitor. The other side of the reference capacitor is connected to Analog Common. The polarity at the output of the integrator (as detected by the comparator at the end of signal integrate phase) determines which terminal of the reference capacitor is connected to the buffer input. The reference capacitor polarity is chosen so that the integrator output will always return towards Analog Common. Since the reference capacitor was charged to the reference voltage during the auto-zero phase, the integrator input voltage is now the reference voltage. The De-Integrate phase lasts for 20,001 counts, or until the comparator detects that the integrator output has crossed zero, whichever occurs first. The time required to return to zero is proportional to the input signal and is inversely proportional to the reference voltage. The number of clock cycles required to return to zero is counted by the digital section and is latched as the measurement result.

$$\text{Displayed reading} = 10{,}000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

The last of the four phases is the zero integrator phase. The non-inverting input of the integrator is internally shorted to Analog Common and the buffer input is internally connected to the output of the comparator. This closes a loop that forces the integrator output to zero. Normally this phase lasts only 100 to 200 counts, sufficient time to remove the small residual charge on the integrator capacitor caused by the comparator delay and the one count delay created by sampling the comparator output only once per clock cycle. However, an overrange condition will exist when the integrator output does not return to zero by the end of the De-Integrate phase, and can leave a residual voltage on the integrator capacitor. In this case, the Zero Integrator phase is increased to 6200 counts to ensure that the integrator capacitor is fully discharged before the next measurement cycle is started.

Analog Section

Analog COMMON

Analog COMMON is the Analog ground reference for the ICL7135. If Input Low is at a voltage other than Analog

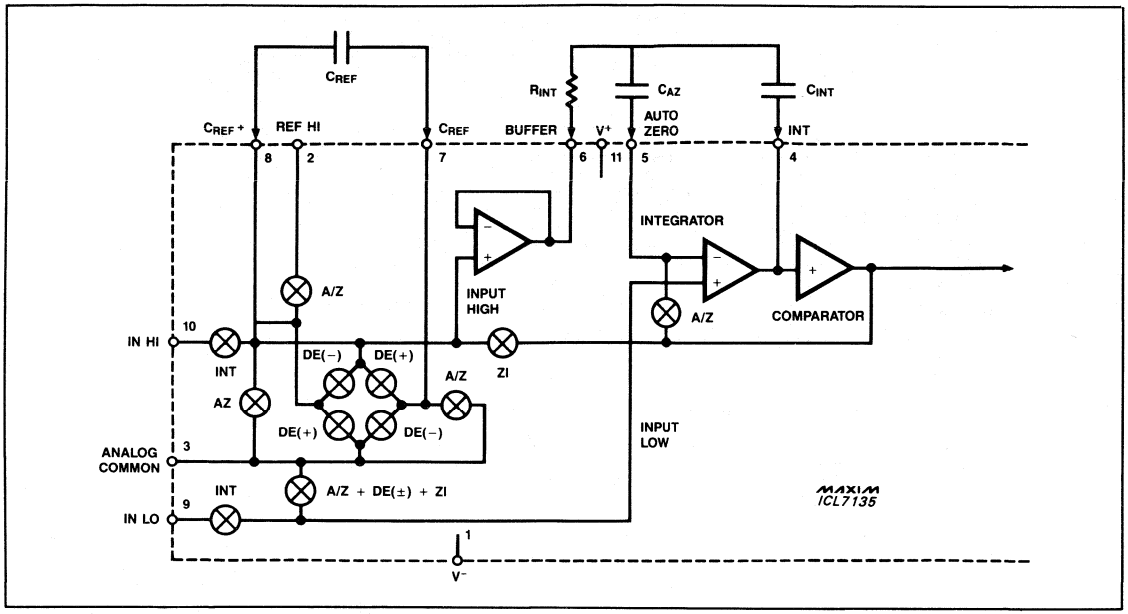


Figure 2. Analog Section of ICL7135

COMMON a common mode voltage will be introduced and, although the ICL7135 has an excellent CMRR, Input Low and Analog COMMON should be connected together whenever possible. Analog COMMON is also the reference point for the reference voltage. The Analog Common voltage is normally connected to the system ground when using ±5V supplies. When the ICL7135 is operated from a single supply voltage the Analog Common should be connected to a voltage source approximately halfway between V^+ and ground.

Input Buffer

The ICL7135 input buffer is a CMOS buffer with a common mode input voltage range of approximately $V^+ - 1.0V$ to $V^- + 1.0V$. The quiescent current is approximately 100μA and the buffer can deliver up to 40μA of output current with excellent linearity.

Integrator

The integrator amplifier, similar to the buffer amplifier, can deliver 20μA of output current with high linearity while swinging to within 0.3V of either supply rail. The integrator's non-inverting terminal is connected to IN LO during the signal integrate phase, so the voltage on the IN LO terminal sets the starting point for the integrator output during signal integrate. If IN LO is at a voltage other than ground, this will limit the maximum allowable swing at the integrator output, and the value of the integrating capacitor should be increased. (Refer to Component Selection)

Comparator

The comparator monitors the voltage on the integrator capacitor during deintegrate. The digital section samples the comparator output once per clock cycle and terminates the deintegrate cycle when the comparator changes its state as the integrator voltage passes through zero. The offset voltage of the comparator is not critical since the auto-zero phase compensates for the offset. The output of the comparator is the only output from the analog section to the digital section.

Digital Section

As shown in Figure 3, the digital section consists of counters, latches, output multiplexer, and control logic. The control logic monitors the counters and the comparator to determine the start of each phase, and sends control signals to the analog section to drive the analog switches to the proper state for each measurement phase. The control section also responds to the external input, RUN/$\overline{\text{HOLD}}$, and creates the control outputs; OVERRANGE, UNDERRANGE, BUSY, and $\overline{\text{STROBE}}$.

RUN/$\overline{\text{HOLD}}$

When RUN/$\overline{\text{HOLD}}$ is high or open the ICL7135 will continuously perform conversions with each measurement being 40,002 clock cycles long. When RUN/$\overline{\text{HOLD}}$ goes low, the ICL7135 will complete the measurement in progress then remain in the auto-zero cycle, holding the last reading. If RUN/$\overline{\text{HOLD}}$ goes high after the maximum period assigned to deintegrate, a new conversion will start, with a delay of 1 to 10,001 clock cycles between the

4½ Digit A/D Converter with Multiplexed BCD Outputs

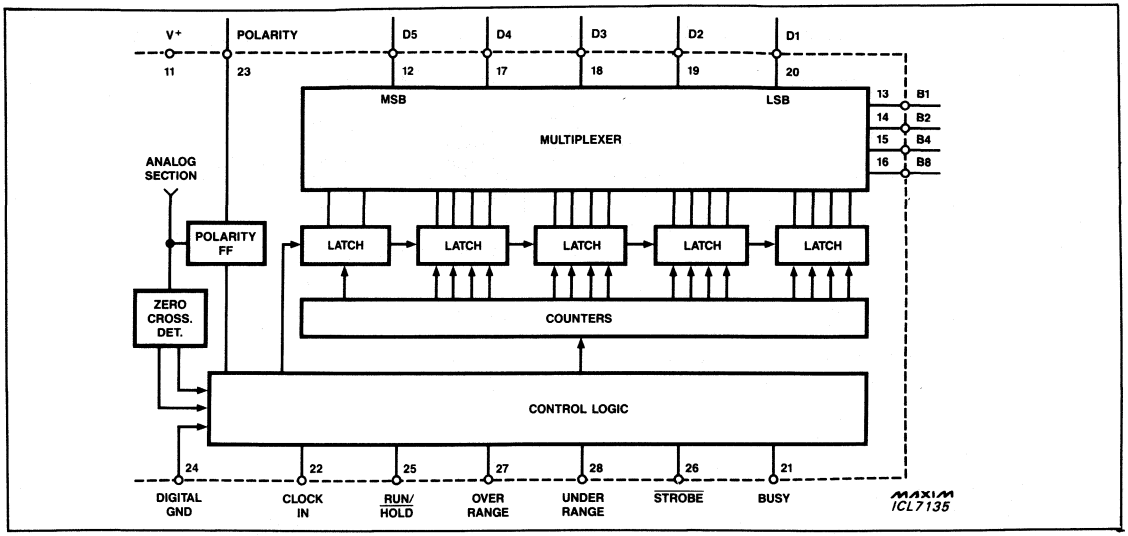


Figure 3. ICL7135 Digital Section

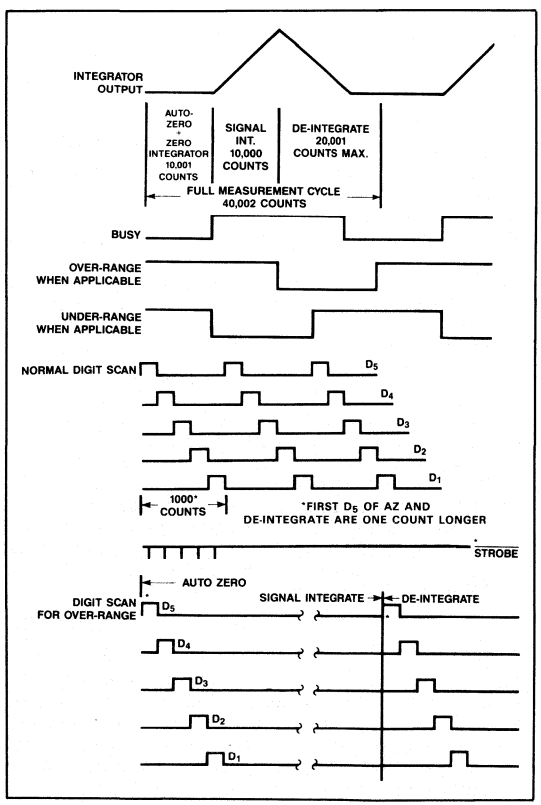


Figure 4. Timing Diagram

rising edge of the RUN/$\overline{\text{HOLD}}$ input and the BUSY output. A RUN/$\overline{\text{HOLD}}$ pulse during the unused portion of deintegrate phase will be ignored, but when in the auto-zero phase a positive pulse of only 300ns (typical) will start the conversion. Figure 5 shows a simple method of obtaining one, and only one, conversion for each measurement request.

BUSY

BUSY is a status output that goes high at the beginning of signal integrate and stays high until the first clock pulse after zero crossing during De-integrate (or end of De-Integrate if overranged). The internal data latches are loaded during the next clock cycle after the falling edge of BUSY. Since BUSY is high for the 10,000 counts of signal integrate + number of counts during De-Integrate + 1 clock cycle, a simple way of sending conversion data down a single pair of wires is to logically 'AND' BUSY with the clock and to subtract 10,001 counts from the number received. Figure 6 shows a system using this method to remotely display data.

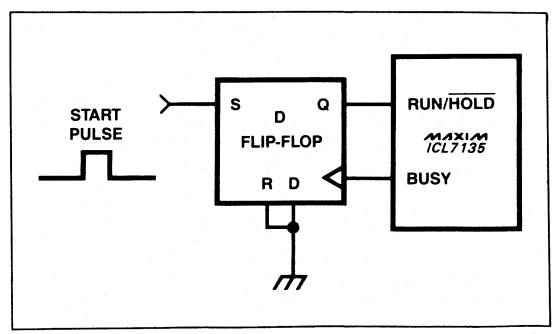


Figure 5. External RUN/$\overline{\text{HOLD}}$ Latch

4½ Digit A/D Converter with Multiplexed BCD Outputs

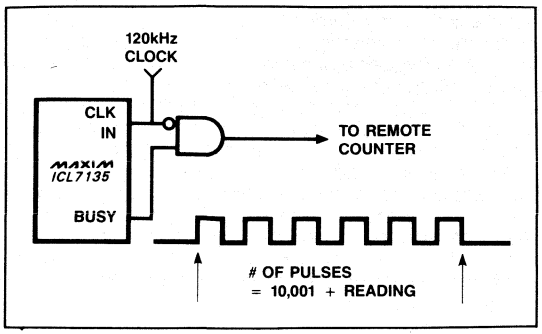


Figure 6. Serial Pulse Stream for Remote Reading

Digit Outputs

The digit outputs go high sequentially, D5 to D1, for a period of 200 clock cycles per digit. The 5 digits are continuously scanned except after an over-range measurement. After an over-range reading the digit scan stops after the strobe sequence, and remains stopped until the start of De-Integrate. For a continuous series of over-range readings, the digits will be scanned for 21,000 counts out of 40,002, resulting in a flashing display as an over-range indicator.

BCD Outputs

The 4 BCD output pins are positive logic signals whose BCD data corresponds to the currently active digit strobe. The ICL7135 does not have inter-digit blanking and the BCD data changes simultaneously with the edges of the digit outputs.

$\overline{\text{STROBE}}$

The $\overline{\text{STROBE}}$ output is a negative going pulse that is useful for latching the multiplexed BCD outputs into external BCD latches. Five negative going $\overline{\text{STROBE}}$ pulses occur in the center of the data corresponding to each of the 5 digits of measurement results, once and only once after the end of each conversion (immediately after the falling edge of BUSY). The BCD data is valid at both edges of $\overline{\text{STROBE}}$, and data can be latched in either a level sensitive latch, or an edge triggered latch. Figures 11, 12 and 14 show the use of $\overline{\text{STROBE}}$ to latch the BCD data.

Over-range and Under-range Outputs

These active high status outputs are set to a high level at the end of BUSY if the measurement result is 1800 or less (Under-range), or greater than 19,999 (Over-range). Under-range is reset at the beginning of the signal integrate phase; over-range is reset at the beginning of the de-integrate phase.

Polarity

The Polarity output is updated at the beginning of each de-integrate phase, and is high for a positive input signal. The Polarity output is valid for all inputs, including ±0 and overrange signals.

Component Selection

The analog component values must be selected with care to achieve optimum performance in each application. Factors that affect the proper values include the reading rate, input common mode voltage, the full scale and reference voltages, and the power supply voltages.

Integrating Resistor

Good linearity is obtained when the integrating resistor value is chosen such that the buffer's maximum output current is between 5 and 40μA. The quiescent current of the buffer is 100μA, and it can supply 20μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the integrating resistor value may be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as:

$$\text{Vswing} = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

Where $I_{INT} = 20\mu A$ if R_{INT} is chosen as described above and $T_{INT} = 10{,}000$ clock periods (83.3ms for 120kHz clock frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. Normally the integrator will not saturate until its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. For ±5V supply and Analog Common and IN LO connected to ground, a ±3.5V to ±4V swing range is optimum. Rearranging the above formula and inserting values as described above, C_{INT} may be calculated as:

$$C_{INT} = \frac{20\mu A \times 83.3ms}{3.5V} = 0.47\mu F$$

The integrator swing must be reduced if either Analog Common or IN LO is not grounded, or if the supply voltage is less than ±5V.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the IN HI is a good indication of the

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amount of dielectric absorption in the integrating capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon capacitors. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero Capacitor

The size of the auto-zero capacitor will have a significant effect on the overall system noise, with larger auto-zero capacitors resulting in a quieter system. The dielectric absorption of the auto-zero capacitor affects only the speed of settling at power-up or recovery from overload and nearly any capacitor type can be used. The zero integrator phase of the ICL7135 allows the use of large auto-zero capacitors while avoiding the "over-range hangover" and hysteresis effects that occur in A/D converters without the zero integrator phase.

Reference Capacitor

Like the auto-zero capacitor, the reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are only required where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in multimeters.

The reference capacitor DOES need to be a low leakage capacitor since it must store the reference voltage while floating during both the signal integrate and the reference deintegrate phases. Any leakage or charge loss during these two phases results in an effective change in the scale factor of the ICL7135. Low cost film capacitors such as polyester or polystyrene have been found to be suitable in most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. For a negative polarity input signal, the reference capacitor does not shift its common mode voltage, but with a positive polarity input signal it undergoes a negative common mode shift equal to the reference voltage. If there are stray capacitances on the reference capacitor terminals, some of the charge on the reference capacitor will be used to charge these stray capacitances as the reference capacitor makes this common mode voltage shift. This loss of charge reduces the voltage on the reference capacitor, and causes positive polarity signals to have a higher measured result than a corresponding negative voltage. This error can be reduced by minimizing the stray capacitance on the reference capacitor terminals, and by increasing the value of the reference capacitor.

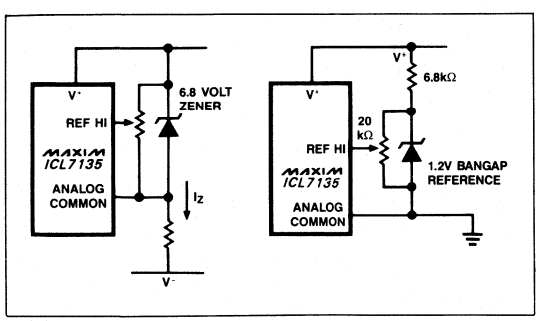

Figure 7. External Reference Voltage

Reference Voltage

The full scale reading of 20,000 will occur when $V_{IN} = 2 \times V_{REF}$. Since the 20,000 count resolution of the ICL7135 is equivalent to a 50ppm resolution, a high stability reference is recommended for high accuracy absolute measurements. Figure 7 shows two suitable methods of generating the reference voltage.

Rollover Resistor and Diode

The ICL7135 is tested for rollover using the circuit of Figure 1, with the 100kΩ resistor and diode in the circuit. The diode is noncritical, and is typically a low cost 1N4148. The resistor value is dependent on many factors including integrator swing, clock frequency, and the amount of rollover error due to "charge suckout" on the reference capacitor. 100kΩ is the optimum value for most circuits and is the value used in testing the ICL7135.

Speedup Resistor

The 27Ω speedup resistor in series with the integrating capacitor adds a pedestal voltage on top of the integrating capacitor voltage. This pedestal voltage causes zero crossing to occur earlier than would occur without the resistor. The effect of the earlier zero crossing is to give the comparator an overdrive voltage, speeding its response and reducing the conversion error due to comparator delay. If the integrator current is changed, the speedup resistor value should be changed so that the $I_{INT} \times R_{SPEEDUP} = 500\mu V$.

Clock Frequency

The clock source should be free of short-term phase and frequency jitter during the conversion period, but long term stability is not critical. The clock frequency is chosen to obtain the desired conversion rate, and to maximize the normal mode rejection of power line frequency interference. The conversion rate is directly proportional to the clock frequency, with each conversion taking 40,002 clock cycles. For maximum normal mode rejec-

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tion, the signal integration period should be an integral multiple of the power line cycles.

$$\text{Reading Rate (in readings per second)} = \frac{f_{CLK}}{40{,}002}$$

$$f_{CLK} \text{ for maximum normal mode rejection} = \frac{f_{LINE} \times 10{,}000}{N}$$

Where f_{LINE} is the line frequency, normally 50Hz or 60Hz and N is the number of line cycles that occur during a signal integration period. For maximum normal mode rejection, N should be an integer.

For 60Hz rejection, suitable clock frequencies include 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, and 75kHz. Suitable frequencies for use with 50Hz power include 250kHz, 166⅔kHz, 125kHz, and 100kHz. The two most common clock frequencies are 120kHz (3 readings per second) and 100kHz (2½ readings per second). Note that a 100kHz clock frequency rejects both 50Hz and 60Hz normal mode signals.

The maximum clock rate is limited by the maximum rate at which the digital logic will correctly function (typically 2MHz), and by the speed of response of the comparator. The comparator delay, about 3μs, has the same effect on the measurement result as does an offset voltage with the same polarity of the input signal. At the recommended clock frequency of 120kHz, this small offset is slightly less than ½ count. At higher clock frequencies the value of the speedup resistor in series with the integration capacitor (normally 27Ω) should be increased. At frequencies above 120kHz, ringing on the integrator output may cause nonlinearities in the first few counts.

The minimum clock frequency is limited by the leakage of the auto-zero and reference capacitors. While seldom desired, measurement cycles as long as 10 seconds can be performed with negligible error at room temperature. Figures 8A and 8B show two methods of generating a suitable clock signal for the ICL7135.

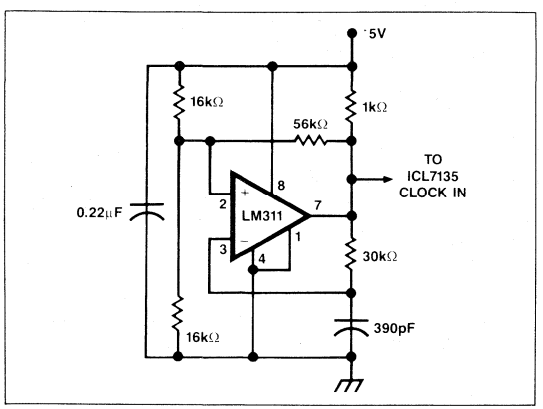


Figure 8A. LM311 Clock Source

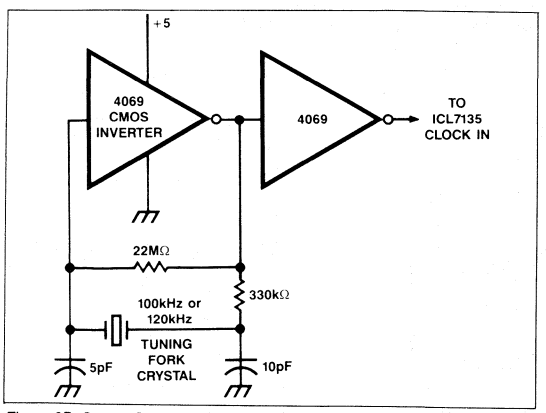


Figure 8B. Crystal Oscillator Clock Source

Application Hints

Grounds

As with all sensitive analog circuitry, it is important to keep the Digital Ground separate from the analog ground (called Analog Common on the ICL7135) to minimize errors caused by the coupling of noise from the digital circuitry into the sensitive analog section. Analog Common should be connected to Digital Ground at only one point, and return currents from digital loads must not flow through the analog ground lines. Avoid any unnecessary current flow in the analog ground path.

Single 5V Supply Operation

The ICL7135 normally uses ±5V supplies, however, in some applications the negative supply is not needed. Specifically, the negative 5V supply is not required if the input signal can be referenced to the center of the ICL7135's common mode voltage range AND the signal voltage is less than ±1.5V. The integrator swing must be reduced, and there will be a slight increase in system noise and nonlinearity. See Figure 9 for recommended component values.

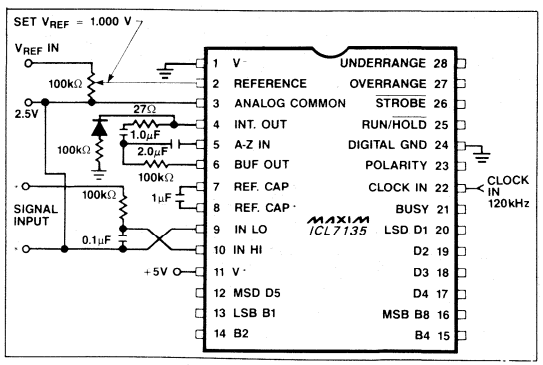


Figure 9. Single +5V Supply Operation

4½ Digit A/D Converter with Multiplexed BCD Outputs

Generating a Negative Supply from +5V

Figures 10A and 10B show two methods of generating a negative supply for the ICL7135. The Maxim ICL7660 will supply 2mA (the maximum supply current of the ICL7135) at 4.85V drop, while the circuit using the CMOS inverter will deliver approximately −3.5V. If the CMOS inverter is used to generate a minus supply, the integrator swing should be reduced to 2.5 to 3V.

Noise

The normal system noise around zero is about 15μV peak-to-peak (not exceeded 95% of the time). Near full scale, the noise increases to about 30μV. The main noise source is the auto-zero loop, and increasing the value of the auto-zero capacitor will reduce the noise. Other noise sources include the buffer and integrator noise; comparator noise; and stray pickup in the input circuitry, the integrator, and the reference capacitor. The noise caused by stray pickup of interfering signals can be reduced by a tight layout and shielding. If the interfering signal frequency is constant, the effects of stray pickup in the input and integrator can be reduced by choosing a clock frequency such that the signal integration period is an integral multiple of the interfering signal's period. Since the length of the de-integration period depends on the input signal level, no single clock frequency can be chosen to reject interfering signals during the de-integrate phase.

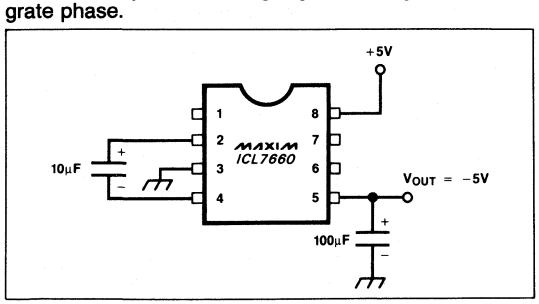


Figure 10A. Generating a Negative Supply

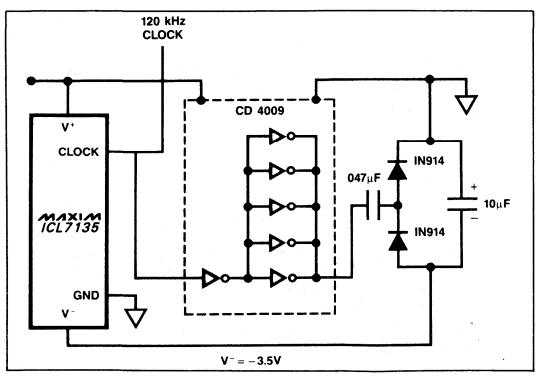


Figure 10B. Generating a Negative Supply

Typical Applications

Figure 11 uses Maxim's ICL7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICL7211 and the CMOS exclusive OR gates are used to drive the ½ digit and the polarity sign. The four AND gates combine the digit outputs with the STROBE output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is ample data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when over-range goes high. The ICL7211A will blank the display when all ones (hex F) is loaded.

The typical operating circuit on the first page of this data sheet shows a 4½ digit A/D with LED drive using the Maxim ICL7212 display driver. In this case the polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135 Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Some applications require non-multiplexed, latched BCD outputs. The circuit shown in Figure 12 will demultiplex and latch the ICL7135 output. If only the first rank of latches is used, the data should not be used during the 800 clock cycle update period that takes place at the end of each conversion since during this update period the

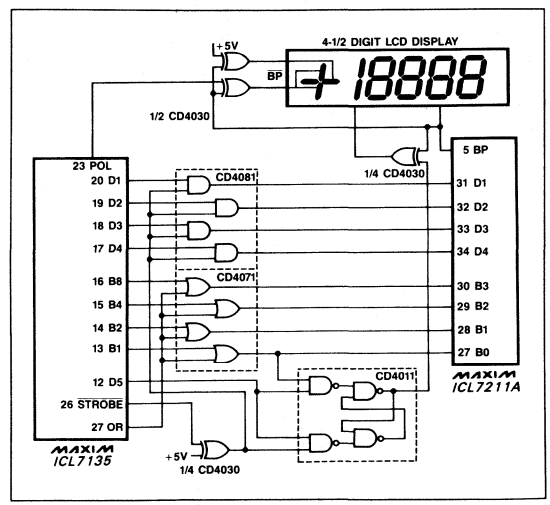


Figure 11. LCD Display with Digit Blanking on Overrange

4½ Digit A/D Converter with Multiplexed BCD Outputs

most significant digit (MSD) data will correspond to the new reading and the least significant digit (LSD) data will be old data from the previous converison. The second rank of latches shown in dotted lines will eliminate this problem by updating all digits simultaneously with the rising edge of D5.

There are many different possible ways of interfacing the ICL7135 to a microprocessor. Figure 13 shows a method that uses only 8 I/O lines. The digit outputs drive a priority encoder, which converts the 1-of-5 format of the digit outputs to a 3 bit binary code. When no digit is active (as in over-range), the binary output code is 0, otherwise the output corresponds to the digit number of the active digit. By sensing BUSY as either an input or as an interrupt, the microprocessor can detect when new data is available.

Another possible interface scheme is to sense only digit D5, then use time delays to choose when to read the other digits' data.

Interfacing With UARTs and Microprocessors

Figure 14 shows a simple interface between a UART and a free running ICL7135. The transmission of the five data words is started by the five STROBE pulses. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. The polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). A parity flag at the receiver can be decoded as a positive signal, no flag as negative, if EPE of the receiver is held low. Figure 15 shows a more complex arrangement. DR goes high when the UART receives a byte via the send input, $\overline{RRI}$. Since DR is connected to the ICL7135's RUN/$\overline{HOLD}$ input this starts a new conversion. At the end of the conversion the falling edge of BUSY resets DR via the UART's DRR input. The transmit sequence is again started by STROBE. A quad 2-input multiplexer is used to superimpose polarity, over-range, and under-range onto the D5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

To insure proper operation, it is necessary that the UART clock be fast enough that each word is transmitted before the next STROBE pulse arrives.

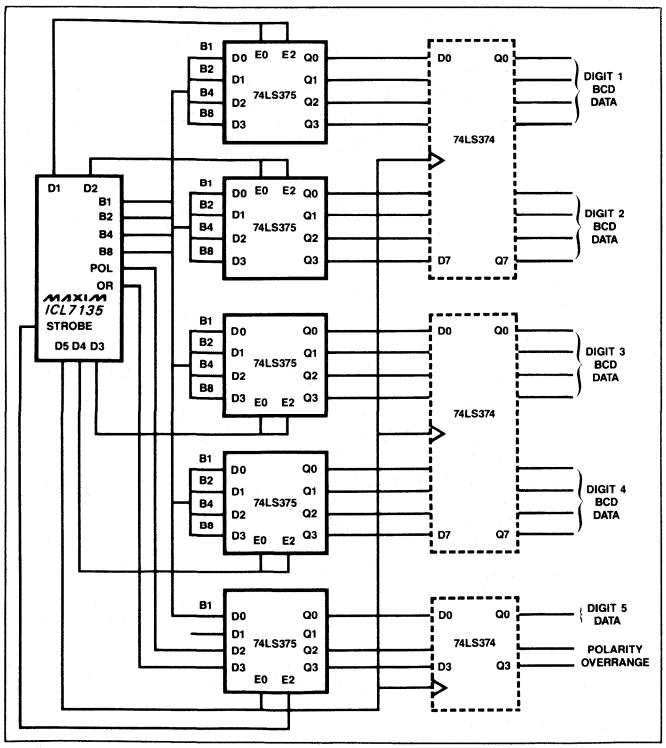


Figure 12. Non-Multiplexed, Latched BCD Output

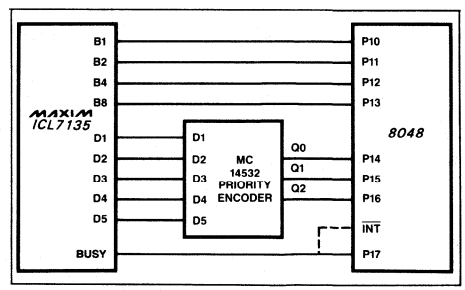


Figure 13. µP Interface

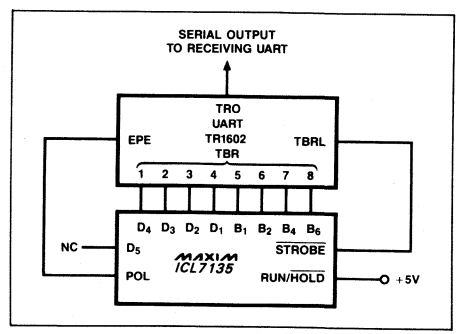


Figure 14. ICL7135 to UART Interface

4½ Digit A/D Converter with Multiplexed BCD Outputs

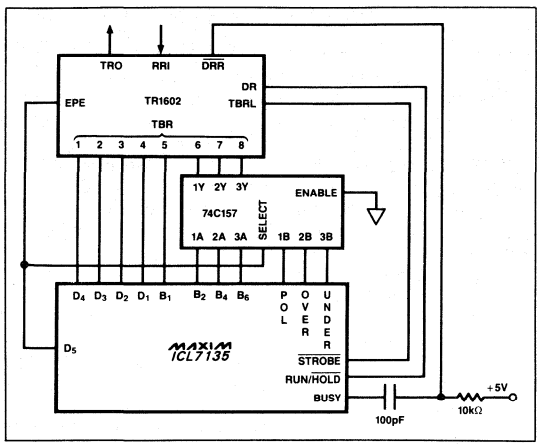
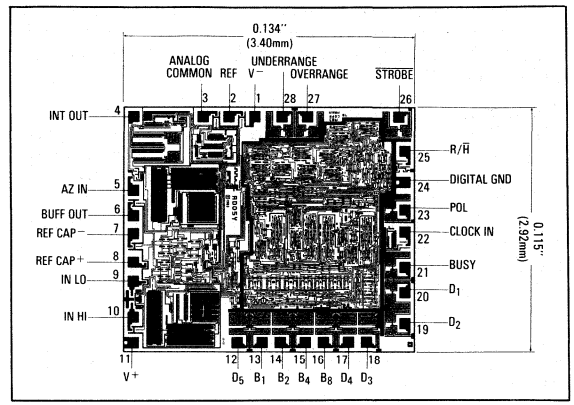
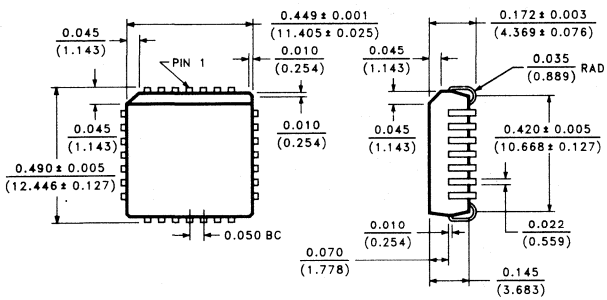


Figure 15. Complex ICL7135 to UART Interface

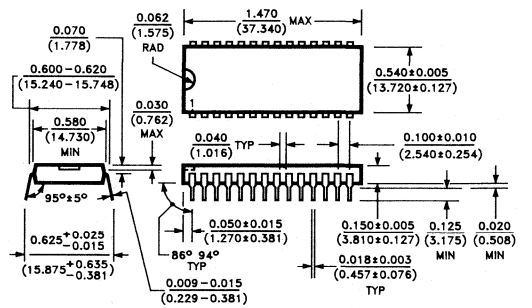
Chip Topography



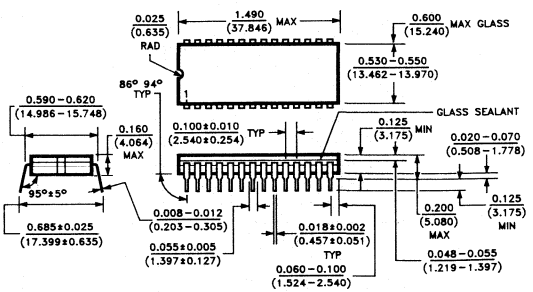
Package Information



28 Lead Plastic Chip Carrier (Quad Pak) (Q)



28 Lead Plastic (PI)
θ_{JA} = 110°C/W, θ_{JC} = 50°C/W



28 Lead Cerdip (JI)
θ_{JA} = 55°C/W

Operational Amplifiers

MAXIM

Single/Dual/Triple/Quad Operational Amplifiers

General Description

The ICL761X/762X/763X/764X family of monolithic CMOS op amps combine ultra low input current with low power operation over a wide supply voltage range. With pin selectable quiescent currents of 10, 100, or 1000 μA per amplifier, these op amps will operate from ±1V to ±8V power supplies, or from single supplies from 2V to 16V. The CMOS outputs swing to within millivolts of the supply voltages.

The ultra low bias current of 1 pA makes this family of op amps ideal for long time constant integrators, picoammeters, low droop rate sample/hold amplifiers and other applications where input bias and offset currents are critical. A low noise current of 0.01 pA/$\sqrt{Hz}$ and an input impedance of 10^{12} ohms ensure optimum performance with very high source impedances in such applications as pH meters and photodiode amplifiers.

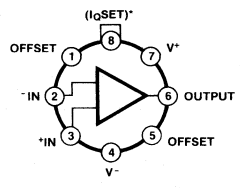
Applications

Battery Powered Instruments
Low Leakage Amplifiers
Long Time Constant Integrators
Low Frequency Active Filters
Hearing Aids and Microphone Amplifiers
Low Droop Rate Sample/Hold Amplifiers
Picoammeters

Pin Configuration

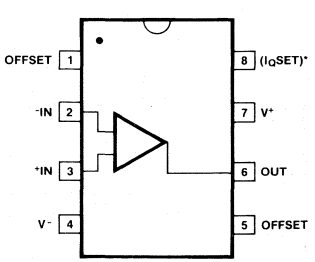
Top View

SINGLES—ICL7611/12/14/16 TO—99



*PIN 7 CONNECTED TO CASE

8 PIN DIP



*EXTERNAL COMPENSATION (ICL7614)

Features

- **Pin-for Pin 2nd Source!**
- **1 pA Typical Bias Current—4 nA Maximum @ 125°C**
- **Wide Supply Voltage Range ±1V to ±8V**
- **Industry Standard Pinouts**
- **Programmable Quiescent Currents of 10, 100 and 1000 μA**
- **Monolithic, Low Power CMOS Design**

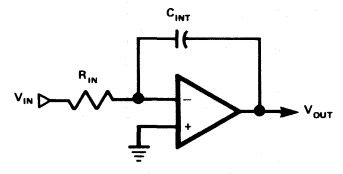
Ordering Information

ICL76XX M N O P

V_{OS} SELECTION	TEMP. RANGE	PACKAGE CODE
A = 2mV	C = 0°C TO 70°C	TV - TO-99, 8 PIN
B = 5mV	M = −55°C to +125°C	PA - PLASTIC 8 PIN MINIDIP
C = 10mV		PD - 14 PIN PLASTIC
D = 15mV		PE - 16 PIN PLASTIC
E = 20mV		JD - 14 PIN CERDIP
		JE - 16 PIN CERDIP

	Singles				Duals		Triples		Quads	
	ICL7611	ICL7612	ICL7614	ICL7616	ICL7621	ICL7622	ICL7631	ICL7632	ICL7641	ICL7642
Compensated	X	X		X	X	X	X		X	X
Externally Compensated			X					X		
Extended CMVR		X		X						
Offset null capability	X	X	X	X		X				
Programmable I_Q	X	X		X			X	X		
Fixed I_Q 10μA										X
Fixed I_Q 100μA			X		X	X				
Fixed I_Q 1mA									X	

Typical Operating Circuit



Long Time Constant Integrator
(Detailed Circuit Diagram — Figure 10)

Single/Dual/Triple/Quad Operational Amplifiers

Ordering Information

Single & Dual

PART	TEMP. RANGE	PACKAGE
ICL761XACPA	0°C to +70°C	8 Lead Plastic DIP
ICL761XACTV	0°C to +70°C	TO-99 Can
ICL761XAMTV	−55°C to +125°C	TO-99 Can
ICL761XBCPA	0°C to +70°C	8 Lead Plastic DIP
ICL761XBCTV	0°C to +70°C	TO-99 Can
ICL761XBMTV	−55°C to +125°C	TO-99 Can
ICL761XDCPA	0°C to +70°C	8 lead Plastic DIP
ICL761XDCTV	0°C to +70°C	TO-99 Can
ICL761XDC/D	0°C to +70°C	Dice
ICL7621ACPA	0°C to +70°C	8 Lead Plastic DIP
ICL7621ACTV	0°C to +70°C	TO-99 Can
ICL7621AMTV	−55°C to +125°C	TO-99 Can
ICL7621BCPA	0°C to +70°C	8 Lead Plastic DIP

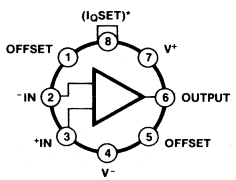
PART	TEMP. RANGE	PACKAGE
ICL7621BCTV	0°C to +70°C	TO-99 Can
ICL7621BMTV	−55°C to +125°C	TO-99 Can
ICL7621DCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7621DCTV	0°C to +70°C	TO-99 Can
ICL7621DC/D	0°C to +70°C	Dice
ICL7622ACPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622ACJD	0°C to +70°C	14 Lead CERDIP
ICL7622AMJD	−55°C to +125°C	14 Lead CERDIP
ICL7622BCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622BCJD	0°C to +70°C	14 Lead CERDIP
ICL7622BMJD	−55°C to +125°C	14 Lead CERDIP
ICL7622DCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7622DCJD	0°C to +70°C	14 Lead CERDIP
ICL7622DC/D	0°C to +70°C	Dice

(X above is replaced by: 1, 2, 4, 6)

Pin Configuration

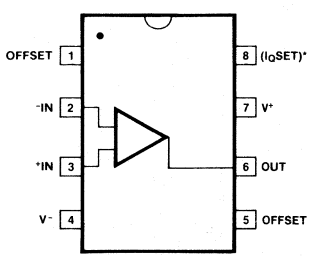
Top View

SINGLES—ICL7611/12/14/16
TO—99



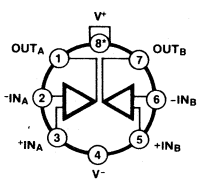
*PIN 7 CONNECTED TO CASE

8 PIN DIP

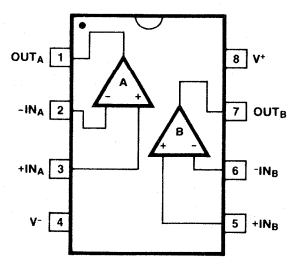


*EXTERNAL COMPENSATION (ICL7614)

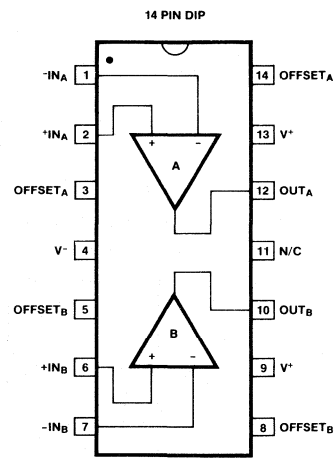
DUALS—ICL7621/22
TO—99



8 PIN DIP



14 PIN DIP



Note: PINS 9 & 13 ARE INTERNALLY CONNECTED

ABSOLUTE MAXIMUM RATINGS[1] — Single & Dual

Total Supply Voltage V^+ to V^- 18V
Input Voltage . . . . . V^++0.3 to V^-−0.3V
Differential Input Voltage[2] . . . . . ±|(V^++0.3)−(V^-−0.3)|V
Duration of Output Short Circuit[3] . . . . . Unlimited

Continuous Power Dissipation @ 25°C		Above 25°C derate as follows:
TO-99 Can	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range . . . . . −55°C to +150°C

Operating Temperature Range
M Series . . . . . −55°C to +125°C
C Series . . . . . 0°C to +70°C
Lead Temperature Soldering, 10 sec . . . . . 300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS — Single & Dual

($V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		10			15		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range (Except ICL7612, ICL7616)	V_{CMR}		±0.6			±0.6			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		+0.6 to −1.1			+0.6 to −1.1			V
Extended Common Mode Voltage Range (ICL7616 Only)	V_{CMR}	$I_Q = 10\mu A$	−1.3		-0.3	−1.3		-0.3	V
Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$, $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$		80			80		dB
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Slew Rate	SR	$A_{VOL} = 1$, $C_L = 100pF$, $V_{IN} = 0.2V_{p-p}$ $R_L = 1M\Omega$		0.016			0.016		V/μs
Rise Time	t_r	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

Single/Dual/Triple/Quad Operational Amplifiers

ELECTRICAL CHARACTERISTICS — Single & Dual
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, T_A = 25°C $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7			15 20	mV mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		10			15			25		µV/°C
Input Offset Current	I_{OS}	T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
Common Mode Voltage Range (Except ICL7612, ICL7616)	V_{CMR}	I_Q = 10µA[1]	+4.4 −4.0			+4.4 −4.0			+4.4 −4.0			V
		I_Q = 100µA[1]	+4.2 −4.0			+4.2 −4.0			+4.2 −4.0			V
		I_Q = 1mA[1]	+3.7 −3.7			+3.7 −3.7			+3.7 −3.7			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	I_Q = 10µA	±5.3			±5.3			±5.3			V
		I_Q = 100µA	+5.3 −5.1			+5.3 −5.1			+5.3 −5.1			V
		I_Q = 1mA	+5.3 −4.5			+5.3 −4.5			+5.3 −4.5			V
Extended Common Mode Voltage Range (ICL7616 Only)	V_{CMR}	I_Q = 10µA	−5.3 +3.7			−5.3 +3.7			−5.3 +3.5			V
		I_Q = 100µA	−5.1 +3.0			−5.1 +3.0			−5.1 +2.7			V
		I_Q = 1mA	−4.5 +2.0			+4.5 +2.0			−4.5 +1.7			V
Output Voltage Swing	V_{OUT}	(1) I_Q = 10µA, R_L = 1MΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			V
		I_Q = 100µA, R_L = 100kΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			V
		(1) I_Q = 1mA, R_L = 10kΩ T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			V
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ I_Q = 10µA, T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 86 80 74	 104		 80 75 68	 104		 80 75 68	 104		dB
		V_O = ±4.0V, R_L = 100kΩ I_Q = 100µA, T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 86 80 74	 102		 80 75 68	 102		 80 75 68	 102		dB
		V_O = ±4.0V, R_L = 10kΩ I_Q = 1mA[1], T_A = 25°C 0°C≤T_A≤+70°C −55°C≤T_A≤+125°C	 80 76 72	 83		 76 72 68	 83		 76 72 68	 83		dB
Unity Gain Bandwidth	G_{BW}	I_Q = 10µA[1] I_Q = 100µA I_Q = 1mA[1]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz

Note 1: ICL7611, 7612, 7616 only
Note 2: ICL7614; 39 pF from pin 6 to pin 8.

ELECTRICAL CHARACTERISTICS — Single & Dual (Continued)
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXA			76XXB			76XXD			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, $I_Q = 10\mu A$[1] $R_S \leq 100k\Omega$, $I_Q = 100\mu A$ $R_S \leq 100k\Omega$, $I_Q = 1mA$[1]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$, $I_Q = 10\mu A$[1] $R_S \leq 100k\Omega$, $I_Q = 100\mu A$ $R_S \leq 100k\Omega$, $I_Q = 1mA$[1]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load $I_Q = 10\mu A$[1] $I_Q = 100\mu A$ $I_Q = 1mA$[1]		 0.01 0.1 1.0	 0.02 0.25 2.5		 0.01 0.1 1.0	 0.02 0.25 2.5		 0.01 0.1 1.0	 0.02 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL} = 100		120			120			120		dB
Slew Rate[2]	SR	A_{VOL} = 1, C_L = 100pF $V_{IN} = 8V_{p-p}$ $I_Q = 10\mu A$,[1] $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$,[1] $R_L = 10k\Omega$		 0.016 0.16 1.6			 0.016 0.16 1.6			 0.016 0.16 1.6		V/μs
Rise Time[2]	t_r	V_{IN} = 50mV, C_L = 100pF $I_Q = 10\mu A$,[1] $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$,[1] $R_L = 10k\Omega$		 20 2 0.9			 20 2 0.9			 20 2 0.9		μs
Overshoot Factor[2]		V_{IN} = 50mV, C_L = 100pF $I_Q = 10\mu A$,[1] $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$,[1] $R_L = 10k\Omega$		 5 10 40			 5 10 40			 5 10 40		%

Note 1: ICL7611, 7612, 7616 only.
Note 2: ICL7614; 39 pF from pin 6 to pin 8.

Single/Dual/Triple/Quad Operational Amplifiers

Ordering Information

Triple & Quad

PART	TEMP. RANGE	PACKAGE
ICL763XBCPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XCCPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XECPE	0°C to +70°C	16 Lead Plastic DIP
ICL763XBCJE	0°C to +70°C	16 Lead CERDIP
ICL763XCCJE	0°C to +70°C	16 Lead CERDIP
ICL763XECJE	0°C to +70°C	16 Lead CERDIP
ICL763XBMJE	−55°C to +125°C	16 Lead CERDIP
ICL763XCMJE	−55°C to +125°C	16 Lead CERDIP
ICL763XEC/D	0°C to +70°C	Dice

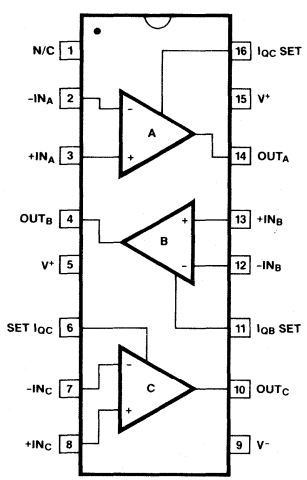
PART	TEMP. RANGE	PACKAGE
ICL764XBCPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XCCPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XECPD	0°C to +70°C	14 Lead Plastic DIP
ICL764XBCJD	0°C to +70°C	14 Lead CERDIP
ICL764XCCJD	0°C to +70°C	14 Lead CERDIP
ICL764XECJD	0°C to +70°C	14 Lead CERDIP
ICL764XBMJD	−55°C to +125°C	14 Lead CERDIP
ICL764XCMJD	−55°C to +125°C	14 Lead CERDIP
ICL764XEC/D	0°C to +70°C	Dice

(X above is replaced by: 1, 2)

Pin Configuration

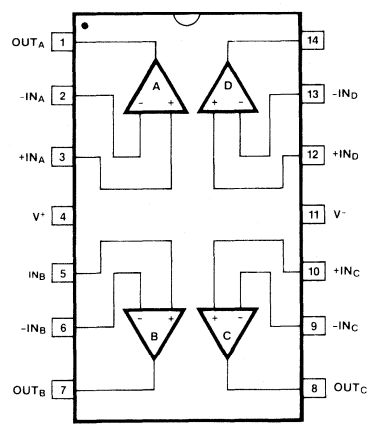
Top View

ICL7631/32
16 PIN DIP



Note: Pins 5 & 15 are internally connected

ICL7641/42
14 PIN DIP



ABSOLUTE MAXIMUM RATINGS[1] — Triple & Quad

Total Supply Voltage V^+ to V^- 18V
Input Voltage . . . . . $V^+ + 0.3$ to $V^- - 0.3$V
Differential Input Voltage[2] . . . . . $\pm\|(V^+ + 0.3) - (V^- - 0.3)\|$V
Duration of Output Short Circuit[3] . . . . . Unlimited

Continuous Power Dissipation @ 25°C		Above 25°C derate as follows:
TO-99 Can	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range . . . . . −55°C to +150°C
Operating Temperature Range
M Series . . . . . −55°C to +125°C
C Series . . . . . 0°C to +70°C
Lead Temperature Soldering, 10 sec . . . . . 300°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
3. The outputs may be shorted to ground or to either supply for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS — Triple & Quad

($V_{SUPP} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless noted)
Specs apply to ICL7631/7632/7642 only.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			5 7			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		15			20		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		0.5	30 300		0.5	30 300	pA
Input Bias Current	I_{BIAS}	$T_A = 25°C$ $0°C \leq T_A \leq +70°C$		1.0	50 500		1.0	50 500	pA
Common Mode Voltage Range	V_{CMR}		±0.6			±0.6			V
Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$, $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		±0.98 ±0.96			±0.98 ±0.96		V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $0°C \leq T_A \leq +70°C$		90 80			90 80		dB
Unity Gain Bandwidth	G_{BW}			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$		80			80		dB
Power Supply Rejection Ratio	PSRR			80			80		dB
Input Referred Noise Voltage	e_n	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15	μA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL} = 100$		120			120		dB
Slew Rate	SR	$A_{VOL} = 1$, $C_L = 100pF$, $V_{IN} = 0.2V_{p-p}$ $R_L = 1M\Omega$		0.016			0.016		V/μs
Rise Time	t_r	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
Overshoot Factor		$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

Single/Dual/Triple/Quad Operational Amplifiers

ELECTRICAL CHARACTERISTICS — Triple & Quad
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$, T_A = 25°C			5			10			20	mV
		$T_{MIN} \leq T_A \leq T_{MAX}$			7			15			25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$		15			20			30		µV/°C
Input Offset Current	I_{OS}	T_A = 25°C		0.5	30		0.5	30		0.5	30	pA
		0°C≤T_A≤+70°C			300			300			300	
		−55°C≤T_A≤+125°C			800			800			800	
Input Bias Current	I_{BIAS}	T_A = 25°C		1.0	50		1.0	50		1.0	50	pA
		0°C≤T_A≤+70°C			500			500			500	
		−55°C≤T_A≤+125°C			4000			4000			4000	
Common Mode Voltage Range	V_{CMR}	I_Q = 10µA[1]	+4.4 −4.0			+4.4 −4.0			+4.4 −4.0			V
		I_Q = 100µA[3]	+4.2 −4.0			+4.2 −4.0			+4.2 −4.0			
		I_Q = 1mA[2]	+3.7 −3.7			+3.7 −3.7			+3.7 −3.7			
Output Voltage Swing	V_{OUT}	(1) I_Q = 10µA, R_L = 1MΩ										V
		T_A = 25°C	±4.9			±4.9			±4.9			
		0°C≤T_A≤+70°C	±4.8			±4.8			±4.8			
		−55°C≤T_A≤+125°C	±4.7			±4.7			±4.7			
		I_Q = 100µA, R_L = 100kΩ										
		(3) T_A = 25°C	±4.9			±4.9			±4.9			
		0°C≤T_A≤+70°C	±4.8			±4.8			±4.8			
		−55°C≤T_A≤+125°C	±4.5			±4.5			±4.5			
		(2) I_Q = 1mA, R_L = 10kΩ										
		T_A = 25°C	±4.5			±4.5			±4.5			
		0°C≤T_A≤+70°C	±4.3			±4.3			±4.3			
		−55°C≤T_A≤+125°C	±4.0			±4.0			±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O = ±4.0V, R_L = 1MΩ[1]										dB
		I_Q = 10µA,[1] T_A = 25°C	86	104		80	104		80	104		
		0°C<T_A<+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
		V_O = ±4.0V, R_L										
		I_Q = 100µA, T_A = 25°C	86	102		80	102		80	102		
		0°C≤T_A≤+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
		V_O = ±4.0V, R_L = 10kΩ[2]										
		I_Q = 1mA,[1] T_A = 25°C	86	98		80	98		80	98		
		0°C≤T_A≤+70°C	80			75			75			
		−55°C≤T_A≤+125°C	74			68			68			
Unity Gain Bandwidth	G_{BW}	I_Q = 10µA[1]		0.044			0.044			0.044		MHz
		I_Q = 100µA[3]		0.48			0.48			0.48		
		I_Q = 1mA[2]		1.4			1.4			1.4		
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, I_Q = 10µA[1]	76	96		70	96		70	96		dB
		$R_S \leq 100k\Omega$, I_Q = 100µA	76	91		70	91		70	91		
		$R_S \leq 100k\Omega$, I_Q = 1mA[2]	66	87		60	87		60	87		
Power Supply Rejection Ratio	PSRR	$R_S \leq 100k\Omega$, I_Q = 10µA[1]	80	94		80	94		80	94		dB
		$R_S \leq 100k\Omega$, I_Q = 100µA	80	86		80	86		80	86		
		$R_S \leq 100k\Omega$, I_Q = 1mA[2]	70	77		70	77		70	77		

Note 1: Does not apply to 7641.
Note 2: Does not apply to 7642.
Note 3: ICL7631/32 only.
Note 4: Does not apply to 7632.

ELECTRICAL CHARACTERISTICS — Triple & Quad (Continued)
(V_{SUPP} = ±5.0V, T_A = 25°C, unless noted)

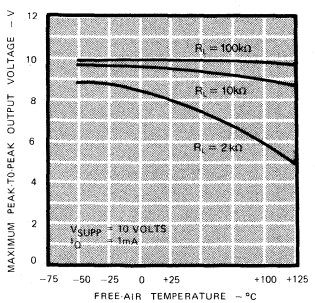
PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXC MIN.	76XXC TYP.	76XXC MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Referred Noise Voltage	e_n	R_S = 100Ω, f = 1kHz		100			100			100		nV/√Hz
Input Referred Noise Current	i_n	R_S = 100Ω, f = 1kHz		0.01			0.01			0.01		pA/√Hz
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load I_Q = 10μA[1] I_Q = 100μA I_Q = 1mA[2]		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL} = 100		120			120			120		dB
Slew Rate[4]	SR	A_{VOL} = 1, C_L = 100pF V_{IN} = 8V_{p-p} I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[2] R_L = 10kΩ		 0.016 0.16 1.6			 0.016 0.16 1.6			 0.016 0.16 1.6		V/μs
Rise Time[4]	t_r	V_{IN} = 50mV, C_L = 100pF I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[2] R_L = 10kΩ		 20 2 0.9			 20 2 0.9			 20 2 0.9		μs
Overshoot Factor[4]		V_{IN} = 50mV, C_L = 100pF I_Q = 10μA,[1] R_L = 1MΩ I_Q = 100μA, R_L = 100kΩ I_Q = 1mA,[2] R_L = 10kΩ		 5 10 40			 5 10 40			 5 10 40		%

Note 1: Does not apply to 7641.
Note 2: Does not apply to 7642.
Note 3: ICL7631/32 only.
Note 4: Does not apply to 7632.

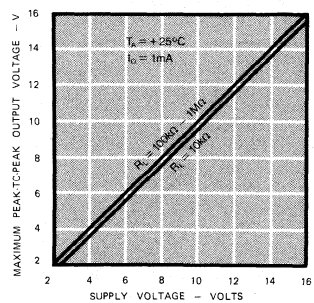
2

Typical Operating Characteristics

MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



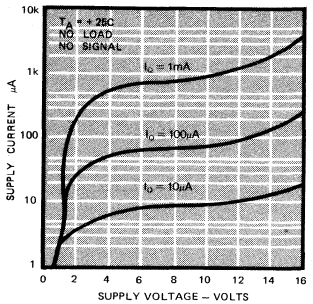
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



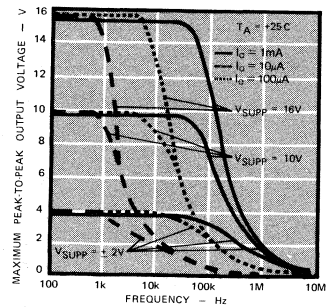
Single/Dual/Triple/Quad Operational Amplifiers

Typical Operating Characteristics

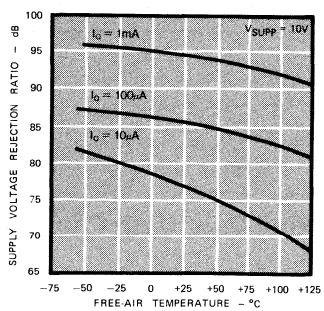
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



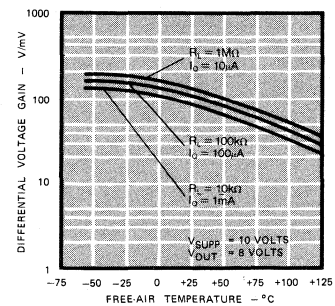
PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



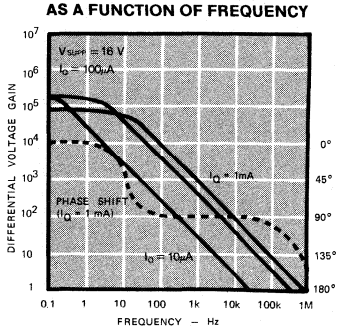
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



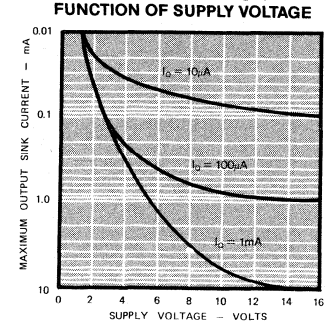
LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY

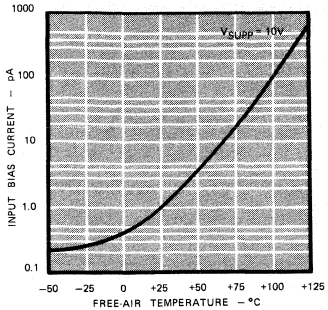


MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

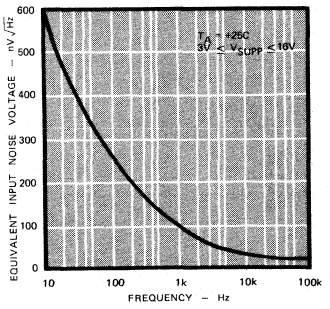


Typical Operating Characteristics

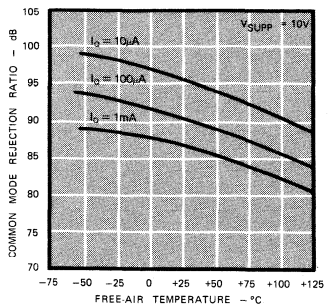
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



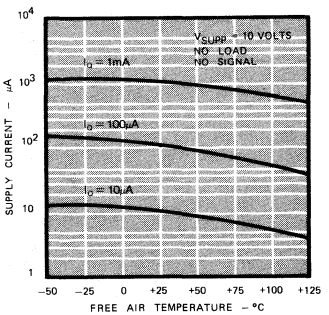
EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



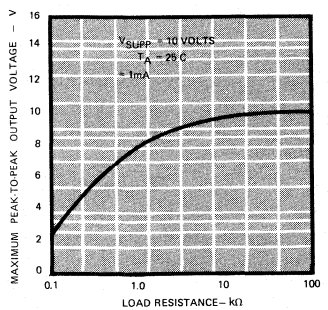
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



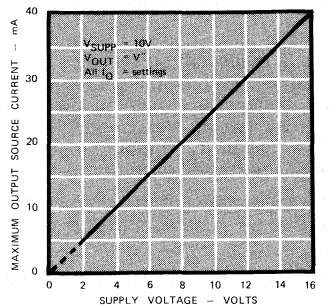
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



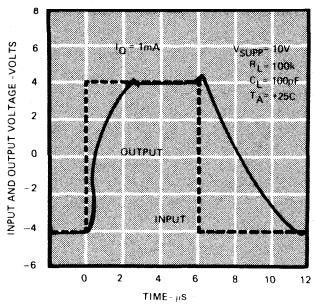
MAXIMUM OUTPUT/SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



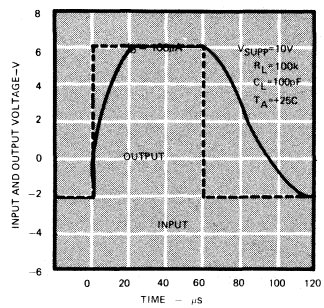
Single/Dual/Triple/Quad Operational Amplifiers

Typical Operating Characteristics

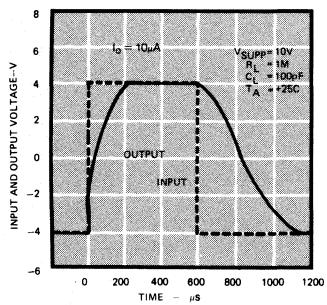
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



Detailed Description

Quiescent Current Selection

The voltage input to the I_Q pin of the single and triple amplifiers selects a quiescent current (I_Q) of 10, 100 or 1000 µA. The dual and quad amplifiers have fixed quiescent current (I_Q) settings. Unity gain bandwidth and slew rate increase with increasing quiescent current, as does output sink current capability. The output source current capability is independent of quiescent current.

The lowest I_Q setting that results in sufficient bandwidth and slew rate should be selected for each specific application.

The I_Q pin of the single and triple amplifiers controls the quiescent current as follows:

I_Q = 10 µA..... I_Q pin to V^+
I_Q = 100 µA..... I_Q pin between V^- +0.8V and V^+ −0.8V
I_Q = 1 mA..... I_Q pin to V^-

Input Offset Nulling

The input offset can be nulled by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 µA, the nulling range provided is adequate for all V_{OS} selections. However with higher values of V_{OS}, and an I_Q of 10 µA, nulling may not be possible.

Frequency Compensation

All of the ICL7611 and ICL7621 Series except the ICL7614 are internally compensated for unity gain operation. The ICL7614 is externally compensated by a capacitor connected between COMP and OUT pins, with 39 pF being sufficient compensation for a unity gain buffer. For gains greater than unity, the compensation capacitor value may be reduced to increase the bandwidth and slew rate.

Output Loading Considerations

Approximately 70% of the amplifier's quiescent current flows in the output stage. The output swing can approach the supply rails for output loads of 1M, 100k and 10k, using the output stage in a highly linear class A mode. Crossover distortion is avoided and the voltage gain is maximized in this mode. The output stage, however, can also be operated in Class AB, which supplies higher output currents. (See graphs under Typical Operating Characteristics). The voltage gain decreases and the output transfer characteristic is non-linear during the transition from Class A to Class B operation.

The output stage, with a gain that is directly proportional to load impedance, approximates a transconductance amplifier. Approximately the same open loop gains are obtained at each of the I_Q settings if corresponding loads of 10k, 100k, and 1M are used.

The maximum output source current is higher than the maximum sink current, and is independent of I_Q.

Like most amplifiers, there are output loads for which the amplifier stability is not guaranteed. In particular, avoid capacitive loads greater than 100 pF; and while on the 1mA I_Q setting, avoid loads less than 5 kΩ. Since the output stage is a transconductance output, very large (>10 μF) capacitive loads will create a dominant pole and the output will be stable, even with loads that are less than 5 kΩ.

Extended Common Mode Voltage Range, ICL7612 and ICL7616

A common mode voltage range that includes both V^+ and V^- is often desirable, especially in single supply operation. The ICL7612 and ICL7616 extended common mode range op amps are designed specifically to meet this need. The ICL7612 input common mode voltage range (CMVR) extends beyond both power supply rails when operated with at least 3V total supply and an I_Q of 10μA or 100μA. The ICL7616 CMVR includes the negative supply voltage (or ground when operated with a single supply) at an I_Q of 10μA or 100μA.

Printed Circuit Board Layout

Careful PCB layout techniques must be used to take full advantage of the very low bias current of the ICL7611 family. The inputs should be encircled with a low impedance trace, or guard, that is at the same potential as the inputs. In an inverting amplifier this is normally ground; in a unity gain buffer connect the guard to the ouput. A convenient way of guarding the 8 pin TO-99 version of the ICL7611 is to use a 10 pin circle, with the two extra pads on either side of the input pins to provide space for a guard ring (see Figure 8). Assembled boards should be carefully cleaned, and if a high humidity environment is expected, conformally coated.

Single Supply Operation

The ICL7611 family will operate from a single 2V to 16V power supply. The common mode voltage range of the standard amplifier types when operated from a single supply is 1.0V to (V^+ − 0.6V) at 10 μA I_Q. At 100 μA I_Q the CMVR is 1.0V to (V^+ − 0.8V), and at 1 mA I_Q the CMVR is 1.3V to (V^+ − 1.3V). If this CMVR range is insufficient, use the ICL7612, whose CMVR includes both ground and V^+ or the ICL7616, whose CMVR includes ground.

A convenient way to generate a psuedo-ground at $V^+/2$ is to use one op amp of a quad to buffer a $V^+/2$ voltage from a high impedance resistive divider.

Low Voltage Operation

Operation at V_{SUPP} = ±1.0V is only guaranteed at I_Q = 10 μA. Output swings to within a few millivolts of the supply rails are achievable for R_L (> or =) 1 MΩ. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to −0.7V at V_{SUPP} = ±1.0V. For applications where greater common mode range is desirable, refer to description of ICL7612 and ICL7616 above.

Applications

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.

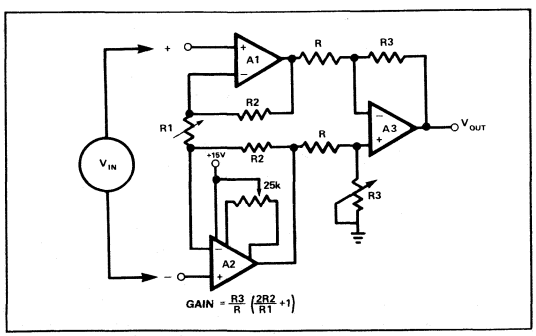


Figure 1. Instrumentation Amplifier—Adjust R3 to improve CMRR. The offset of all three amplifiers is nulled by the offset adjustment of A2.

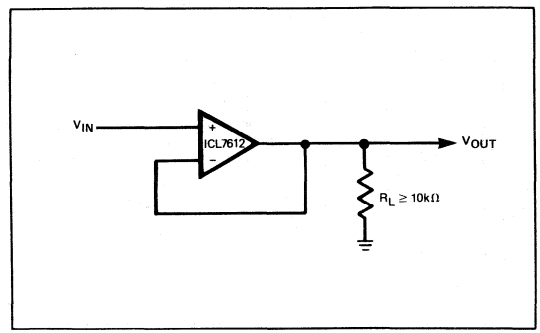


Figure 2. Simple Follower—By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

Single/Dual/Triple/Quad Operational Amplifiers

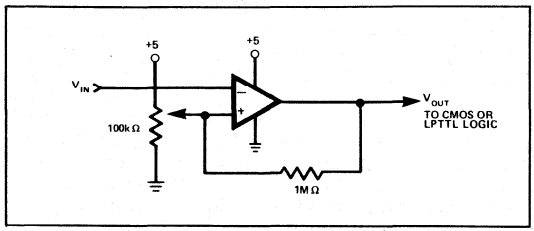


Figure 3. Level Detector — By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

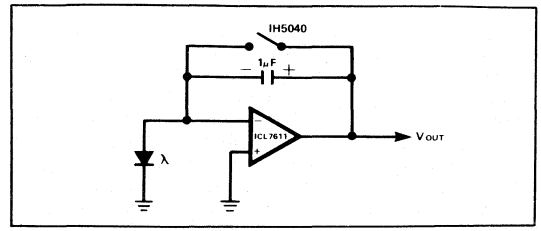


Figure 4. Photocurrent Integrator — Low leakage currents allow integration times up to several hours.

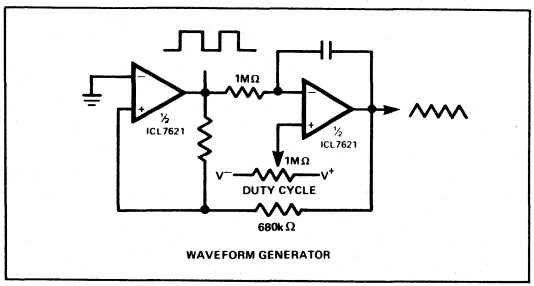


Figure 5. Precise Triangle/Square Wave Generator — The frequency and duty cycle are virtually independent of power supply.

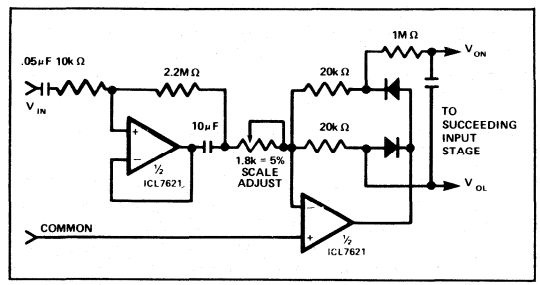


Figure 6. Averaging AC to DC Converter — Recommended Maxim's ICL7106/07/09 A/D Converters.

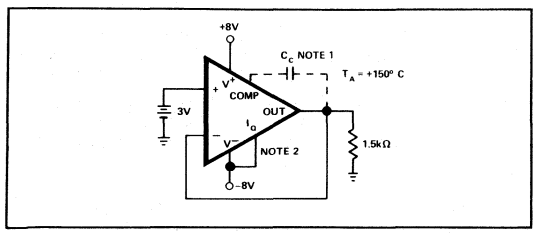


Figure 7. Burn-In and Life Test Circuit

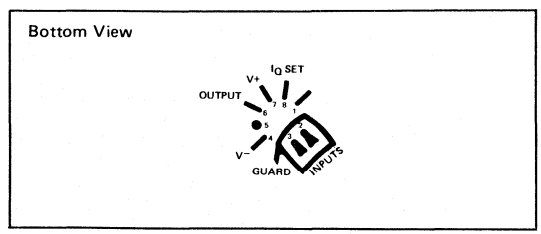


Figure 8. Input Guard for TO-99

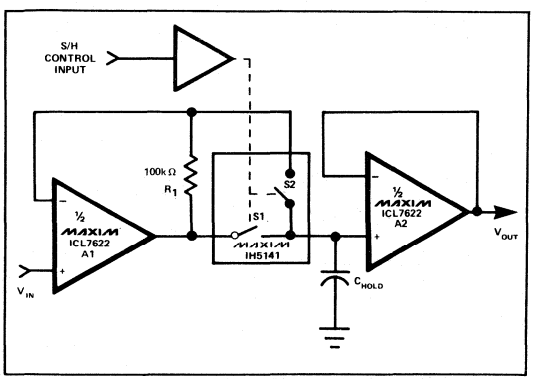


Figure 9. Low Droop Rate Sample & Hold — S2 improves accuracy and acquisition time by including the voltage drop across S1 inside the feedback loop. R1 closes the feedback loop of A1 during the hold phase. The droop rate is $[I_{BIAS(AZ)} + I_{LEAK(S1)} + I_{LEAK(S2)}]/C_{HOLD}$.

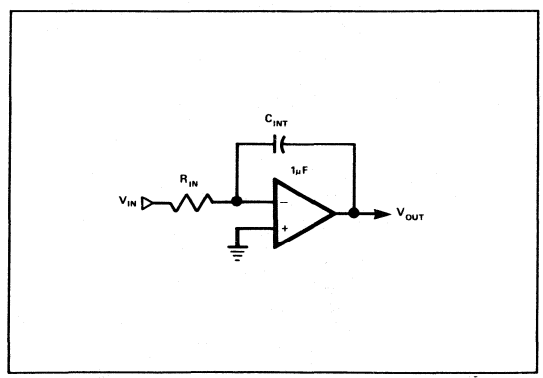


Figure 10. Long Time Constant Integrator — With R_{IN} = 10" ohm, the time constant of this integrator is 100,000 seconds. Since the input voltage is converted to a current by R_{IN}, the input voltage can far exceed the power supply voltage.

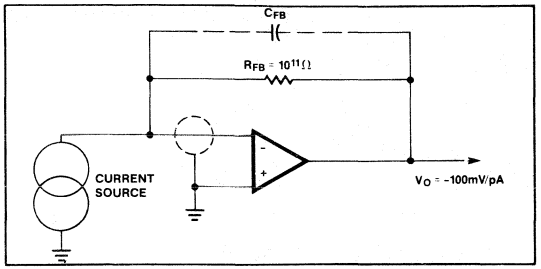


Figure 11. Pico Ammeter — The response time of this circuit is $R_{FB} \times C_{FB}$, where C_{FB} is the stray capacitance between the output and the inverting terminal of the amplifier.

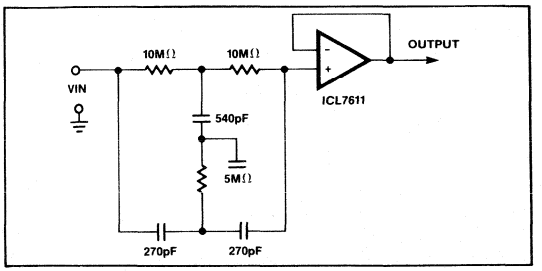
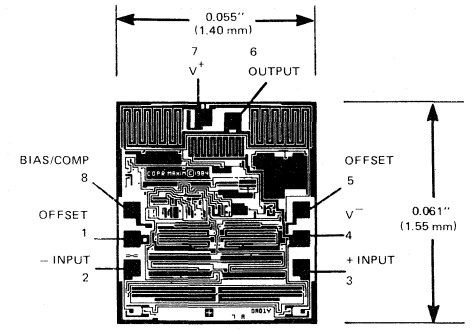


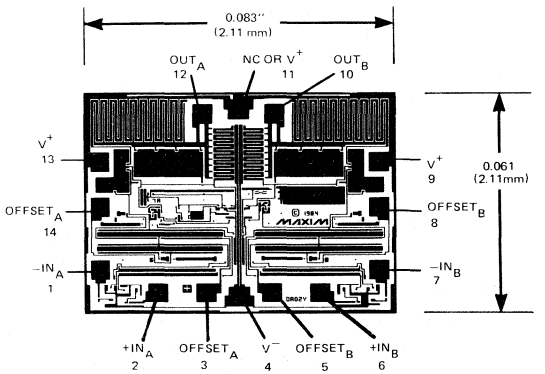
Figure 12. 60 Hz Twin "T" Notch Filter — The low, 1 pA bias current of the ICL7611 allows use of small 540 pF and 270 pF capacitors, even with a notch frequency of 60 Hz. The 60 Hz rejection is approximately 40 dB.

Chip Topographies

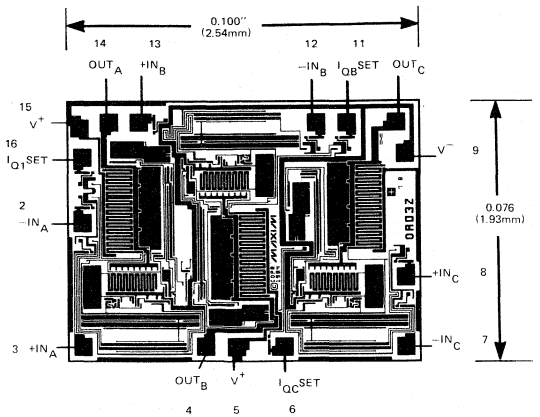
ICL7611/12/14/16 SINGLE



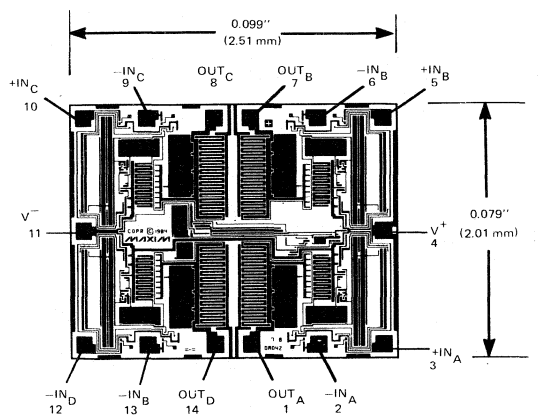
ICL7621/22 DUAL



ICL7631/32 TRIPLE

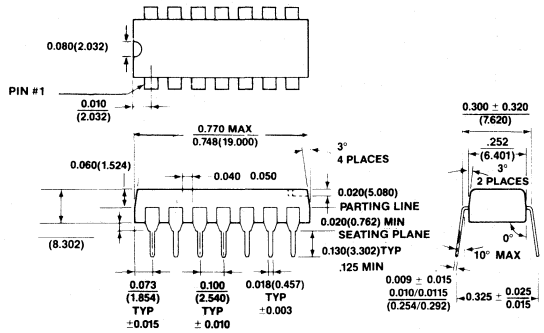


ICL7641/42 QUAD

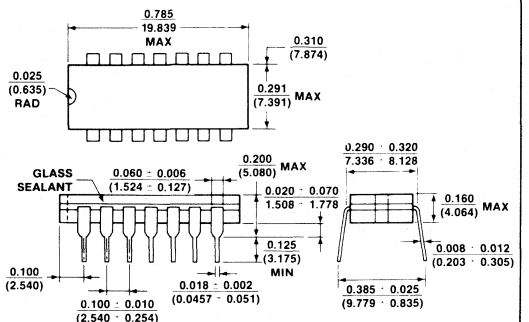


Single/Dual/Triple/Quad Operational Amplifiers

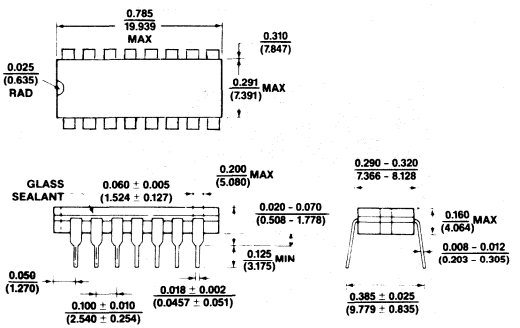
Package Information



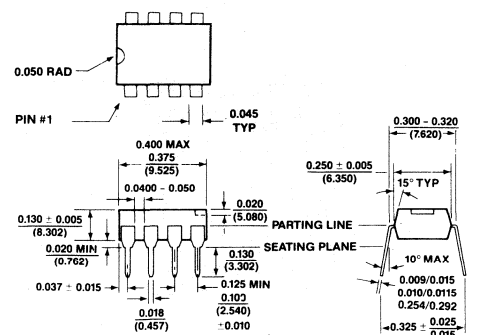
14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W



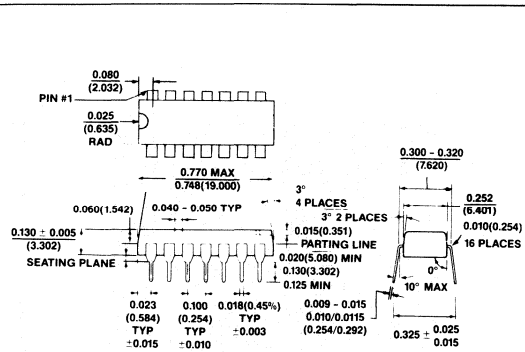
14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W



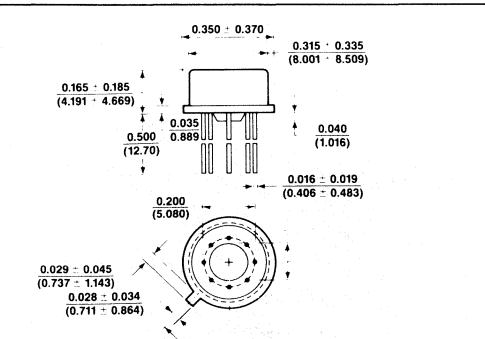
16 Lead CERDIP (JE)
θ_{JA} = 100°C/W
θ_{JC} = 50°C/W



8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



16 Lead Plastic (PE)
θ_{JA} = 135°C/W
θ_{JC} = 65°C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

MAXIM
Chopper Stabilized Operational Amplifier

General Description

The Maxim ICL7650 is a chopper-stabilized amplifier, ideal for low-level signal processing applications. Featuring high performance and versatility, this device combines low input offset voltage, low input bias current, wide bandwidth and exceptionally low drift over time and temperature. Low offset is achieved through a nulling scheme that provides continuous error correction. A nulling amplifier alternately nulls itself and the main amplifier. The result is an input offset voltage that is held to a minimum over the entire operating temperature range.

The ICL7650B is an exact replacement for the Intersil ICL7650B. This device has a maximum offset voltage of 10μV, a maximum input offset voltage temperature coefficient of 0.1μV/°C, and a maximum bias current of 20 pA; all specified over the commercial temperature range.

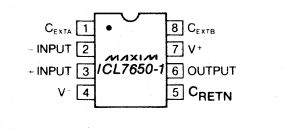
A 14 lead version is available which can be used with either an internal or external clock. The 14 lead version has an output voltage clamp circuit to minimize overload recovery time.

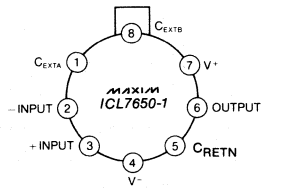
Applications

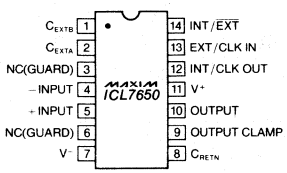
Condition Amplifier
Precision Amplifier
Instrumentation Amplifier
Thermocouples
Thermistors
Strain Gauges

Pin Configuration

Top View







NC = NO INTERNAL CONNECTION

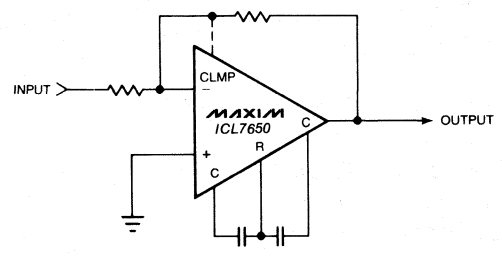
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Lower Supply Current: 2.0 mA**
- **Low Offset Voltage: 1 μV**
- **No Offset Voltage Trimming Needed**
- **High Gain, CMRR and PSRR (120 dB min)**
- **Lower Offset Drift With Time and Temperature**
- **Extended Common Mode Voltage Range**
- **Low DC Input Bias Current: 10 pA**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7650CDP	0°C to +70°C	14 Lead Plastic DIP
ICL7650IJD	-20°C to +85°C	14 Lead CERDIP
ICL7650MJD	-55°C to +125°C	14 Lead CERDIP
ICL7650CPA-1	0°C to +70°C	8 Lead Plastic DIP
ICL7650CTV-1	0°C to +70°C	TO-99 Can
ICL7650ITV-1	-20°C to +85°C	TO-99 Can
ICL7650MTV-1	-55°C to +125°C	TO-99 Can
ICL7650C/D	0°C to +70°C	Dice
ICL7650BCPD	0°C to +70°C	14 Lead Plastic DIP
ICL7650BCPA-1	0°C to +70°C	8 Lead Plastic DIP
ICL7650BCTV-1	0°C to +70°C	TO-99 Can
ICL7650BC/D	0°C to +70°C	Dice

Typical Operating Circuit



Inverting Amplifier with Optional Clamp

(Detailed Circuit Diagram—Figure 5)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) ..... 18 Volts
Input Voltage ..... (V^+ + 0.3) to (V^- − 0.3) Volts
Storage Temp. Range ..... −65°C to 160°C
Operating Temp. Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on oscillator control pins ..... V^+ to V^-
except EXT CLOCK IN: ...(V^+ + 0.3) to (V^+ − 6.0) Volts
Duration of Output short circuit ..... Indefinite
Current into any pin 10mA
—while operating (Note 4) ..... 100 μA

Cont. Total Power Dissipation (T_A = 25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW
TO-99 ..... 250 mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS — ICL7650

(V^+ = +5V, V^- = −5V, T_A = 25°C, Test Circuit, Unless Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C −55°C < T_A < +85°C −55°C < T_A < +125°C		±0.7 ±1.0	±5 5.0	μV
Average Temp. Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	−20°C < T_A < +85°C		0.01 50	0.05	μV/°C
Input Bias Current (doubles every 10°C)	I_{BIAS}	T_A = +25°C 0°C < T_A < +70°C −20°C < T_A < +85°C		1.5 35 100	10	pA
Input Offset Current	I_{OS}	T_A = 25°C		0.5		pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ	1×10^6	5×10^6		V/V
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ R_L = 100kΩ	±4.7	±4.85 ±4.95		V
Common Mode Voltage Range	CMVR		−5.0	−5.2 to +2.0	1.6	V
Common Mode Rejection Ratio	CMRR	CMVR = −5V to +1.6	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω 0 to 10Hz		2		μVp-p
Input Noise Current	I_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		2.5		V/μs
Rise Time	t_r			0.2		μs
Overshoot				20		%
Operating Supply Range	V+ to V−		4.5		16	V
Supply Current	I_{SUPP}	no load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	pins 12–14 open (DIP)	120	200	375	Hz
Clamp ON Current (note 2)		R_L = 100kΩ	25	70	200	μA
Clamp OFF Current (note 2)		−4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See OUTPUT CLAMP under detailed description.
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: $I_{OS} = 2 \bullet I_{BIAS}$

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Chopper Stabilized Operational Amplifier

- Lower Supply Current
- Key Parameters Guaranteed over Temperature
- Extended Common Mode Voltage Range
- Characterized over Military Temperature Range
- Significantly Enhanced "ESD" Protection (Note 6)
- Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

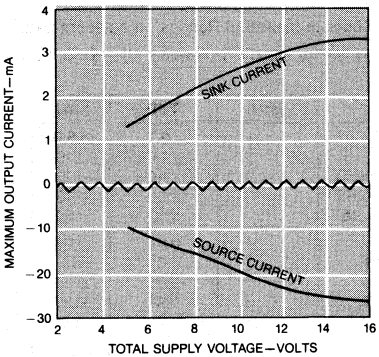
ELECTRICAL CHARACTERISTICS The ICL7650 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, T_A = 25°C, Test Circuit, unless Noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C, ICL7650		±0.7	±5.0	µV
		T_A = +25°C, ICL7650B		±1.0	±10	µV
		0°C ≤ T_A ≤ +70°C, ICL7650 (Note 7)		±1.0	±10	µV
		-20°C ≤ T_A ≤ +85°C, ICL7650 (Note 7)		±1.0	±10	µV
		-55°C ≤ T_A ≤ +125°C, ICL7650 (Note 7)		±10	±50	µV
Average Temperature Coefficient of Input Offset Voltage (Note 7)	$\frac{\Delta V_{OS}}{\Delta T}$	0°C ≤ T_A ≤ +70°C, ICL7650		0.01	0.05	µV/°C
		0°C ≤ T_A ≤ +70°C, ICL7650B		0.01	0.1	µV/°C
		-20°C ≤ T_A ≤ +85°C, ICL7650		0.01	0.05	µV/°C
		-55°C ≤ T_A ≤ +85°C, ICL7650		**0.01**	**0.05**	**µV/°C**
		+85°C ≤ T_A ≤ +125°C, ICL7650		**0.25**	**1.5**	**µV/°C**
Input Bias Current	I_B	T_A = +25°C, ICL7650		4	10	pA
		T_A = +25°C, ICL7650B		12	20	pA
		0°C ≤ T_A ≤ +70°C		**20**	**100**	**pA**
		-20°C ≤ T_A ≤ +85°C		**50**	**200**	**pA**
		-55°C ≤ T_A ≤ +125°C		**0.3**	**10**	**nA**
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ T_A = +25°C	1 x 10^6	5 x 10^6		V/V
		0°C ≤ T_A ≤ +70°C	**0.5 x 10^6**			**V/V**
		-20°C ≤ T_A ≤ +85°C	**0.5 x 10^6**			**V/V**
		-55°C ≤ T_A ≤ +125°C	**0.2 x 10^6**			**V/V**
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common Mode Voltage Range	CMVR	**0°C ≤ T_A ≤ +70°C**	**-5.0**	**-5.2 to 3.0**	**2.5**	**V**
		-20°C ≤ T_A ≤ +85°C	**-5.0**	**-5.2 to 3.0**	**2.5**	**V**
		-55°C ≤ T_A ≤ +125°C	**-4.5**	**-4.8 to 3.0**	**2.5**	**V**
Common Mode Rejection Ratio	CMRR	CMVR = -5V to +2.5V	120	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	120	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_s = 100Ω 0 to 10Hz		2		μV_{p-p}
Input Noise Current	i_n	f = 10Hz		0.01		pA/√Hz
Unity Gain Bandwidth	GBW			2.0		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		2.5		V/µs
Rise Time	t_r			0.2		µs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		4.5		16	V
Supply Current	I_{SUPP}	no load		1.2	2.0	mA
Internal Chopping Frequency	f_{CLKOUT}	pins 13 and 14 open (DIP)	120	200	375	Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	70	200	µA
Clamp OFF Current (Note 2)		-4.0V ≤ V_{OUT} ≤ +4.0V		1		pA
Offset Voltage vs Time				100		nV/√month

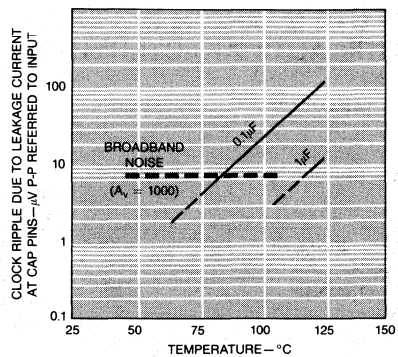
NOTE 1: Operating temperature range for M series parts is −55°C to +125°C, for I series is −20°C to +85°C, for C series is 0°C to +70°C
NOTE 2: See OUTPUT CLAMP under detailed description.
NOTE 3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.
NOTE 4: Limiting input current to 100µA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
NOTE 5: $I_{OS} \approx 2 \bullet I_{BIAS}$
NOTE 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883B Method 3015.1 Test Circuit)
NOTE 7: Sample tested. Limits are not used to calculate outgoing quality level.

Chopper Stabilized Operational Amplifier

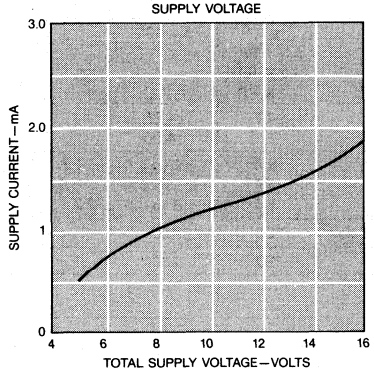
MAXIMUM OUTPUT CURRENT
vs. SUPPLY VOLTAGE



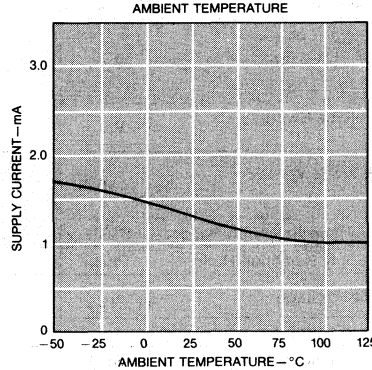
CLOCK RIPPLE REFERRED TO THE INPUT
vs. TEMPERATURE



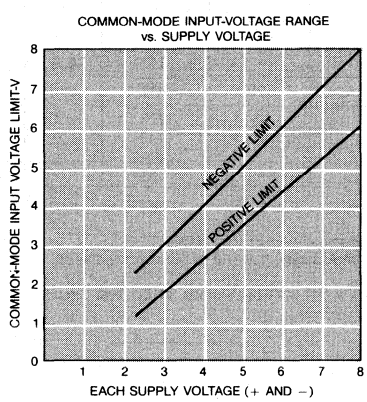
SUPPLY CURRENT vs.
SUPPLY VOLTAGE



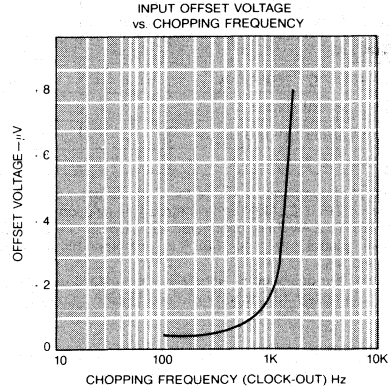
SUPPLY CURRENT vs.
AMBIENT TEMPERATURE



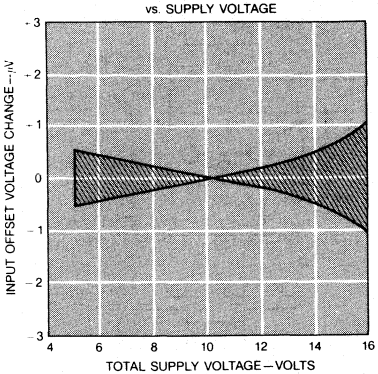
COMMON-MODE INPUT-VOLTAGE RANGE
vs. SUPPLY VOLTAGE



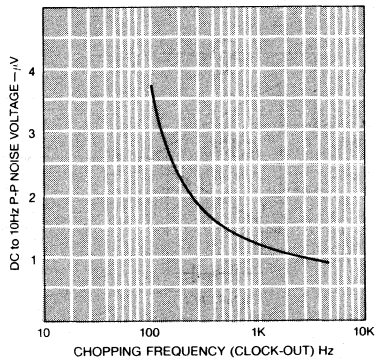
INPUT OFFSET VOLTAGE
vs. CHOPPING FREQUENCY



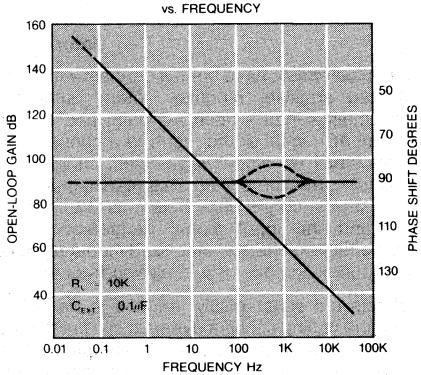
INPUT OFFSET VOLTAGE CHANGE vs. SUPPLY VOLTAGE



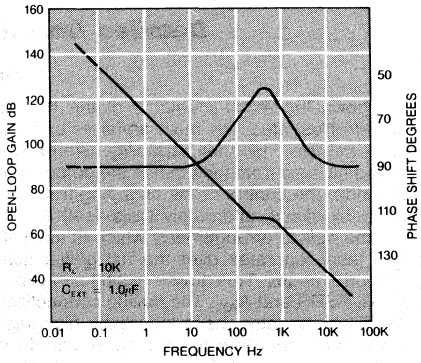
10Hz P-P NOISE VOLTAGE vs. CHOPPING FREQUENCY



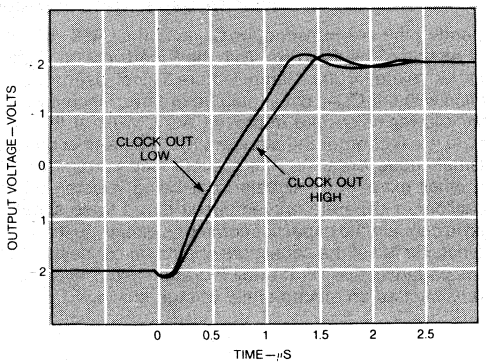
OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



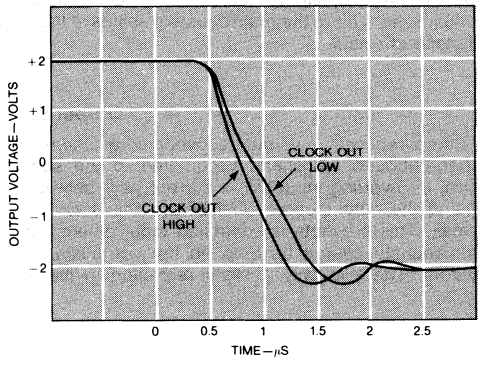
OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



Chopper Stabilized Operational Amplifier

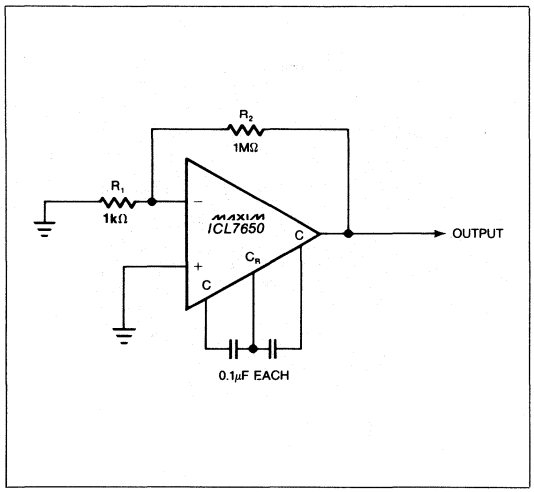


Figure 1. Maxim ICL7650 Test Circuit

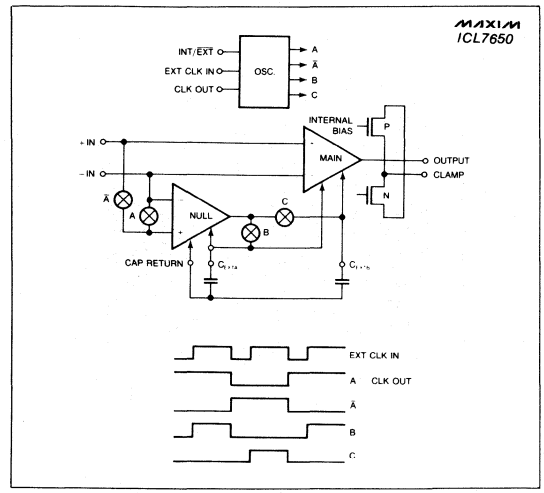


Figure 2. Block Diagram

Detailed Description

Amplifier

Figure 2 shows the major elements of the ICL7650. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling arrangement, which is independent of the output level, operates over the full power supply and common mode ranges. This device exhibits an exceptionally high CMRR, PSRR and A_{VOL}. The nulling connections, which are MOSFET back gates, have inherently high impedance. The two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants.

The chopper frequency charge injection at the input terminals is minimized by careful balance of the input switches. The feed forward-type injection into the compensation capacitor is also minimized. This is the main cause of spikes at the output in this type of circuit.

Output Clamp

The clamp reduces overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction, or inverting input pin, a current path between this point and the output occurs just before the output device saturates. This prevents uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors. There is only a slight reduction in the output swing.

Intermodulation

Intermodulation effects have been a problem with older chopper stabilized amplifier modules. Intermodulation occurs since the amplifier has a finite AC gain, and therefore will have a small AC signal at the input. In a chopper stabilized module this small AC signal is detected, chopped, and fed into the offset correction circuit. This results in spurious outputs at the sum and difference frequencies of the chopping frequency and the input signal frequency. Other intermodulation effects in chopper stabilized modules include gain and phase anomalies near the chopping frequency.

These effects are substantially reduced in the ICL7650 by adding into the nulling circuit a dynamic current that compensates for the AC on the inputs due to the amplifiers finite gain. Unlike the modules, the ICL7650 can precisely compensate for the finite AC gain since both the AC gain rolloff and the intermodulation compensation current are controlled by matched capacitors onboard the ICL7650.

Nulling Capacitor Connection

Separate pins are provided for C_{RETN} and CLAMP in the 14 lead version of the ICL7650. With the 8 lead version, a choice must be made. If the clamp feature is not used, the "-1" version with the C_{RETN} pin should be ordered since it will give slightly lower noise and improved AC CMRR. If the clamp feature is used, order the standard ICL7650 and connect the external capacitors to V^-. To prevent load current IR drops and other extraneous signals from being injected into the capacitors, a separate printed circuit board trace should be used to connect the capacitor commons directly to the V^- pin. The outside foil of the capacitors should be connected to the low impedance side of the null storage circuit, V^- or C_{RETN}. This will act as an electro-static voltage shield.

Clock Operation

A frequency of 200Hz is generated by the internal oscillator of the ICL7650. This is available at the CLK OUT pin on the 14-pin devices. The use of an external clock is also optional on these parts. The INT/$\overline{\text{EXT}}$ pin may be left open for normal operation due to the internal pull-up. However, the internal clock must be disabled and this pin must be tied to V− if an external clock is desired. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500 Hz, since the capacitors are charged only when EXT CLK IN is HIGH. This ensures that any transients have time to settle before the capacitors are turned OFF. The external clock should swing between GROUND and (V^+) for power supplies up to ±6 volts, and between (V^+) and (V^+ −6V) for higher supply voltages.

To avoid a capacitor imbalance during overload, a strobe signal may be used. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier. A typical amplifier will drift less than 10 μV/s since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications

Device Selection

In many applications Maxim's interchangeable ICL 7652 is preferred over the ICL 7650. The ICL7650 has a higher gain-bandwidth product and lower input bias currents, while the ICL7652 has less noise. The major change in the ICL7652 to reduce the noise is an increase in the size of the input FETs. This, however, increases the leakage at the ICL7652's external null pins. This means the ICL7650 can operate to a higher temperature with 0.1μF capacitors before the clock ripple (due to leakage at the null capacitor pins) becomes excessive and 1.0μF external capacitors are required.

Output Stage/Load Driving

The ICL7650 is in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high impedance stage (approximately 18KΩ for 1 output circuit. The open loop gain, for example, will be 17dB lower with a 1KΩ load than with a 10KΩ load. This lower gain is of little consequence if the amplifier is used strictly for DC, since the DC gain is typically greater than 120 dB even with a 1KΩ load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10kΩ or higher. The result will be a smooth 6dB/octave response from 0.1Hz to 2MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

C_{EXTA} and C_{EXTB}, the two required capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1μF for the preset internal clock. This component value should be scaled proportionally to the relationship between the chopping frequency and the nulling time constant if an external clock is used. A low leakage ceramic capacitor may prove suitable for many applications, however, a high-quality film-type capacitor such as mylar is preferred. Low dielectric absorption capacitors (such as polypropylene) should be used for lowest settling on initial turn-on. With low dielectric absorption capacitors, the ICL7650 will settle to 1μV offset in 100 ms, but several seconds may be required if ceramic capacitors are used.

Thermo-electric Effects

Thermo-electric effects developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc., ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages typically around 10μV/°C, but up to hundreds of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide it is essential to take special precautions to avoid temperature gradients. To eliminate air movement, all components should be enclosed (particularly those caused by power dissipating elements in the system). Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

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Input Guarding

Low leakage, high impedance, CMOS inputs allow the ICL7650 to make measurements of high impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. A significant reduction in leakage can be accomplished by using guarding to lower the voltage difference between inputs and adjacent metal runs. By using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board, input guarding of the 8-lead T0-99 package is accomplished. A conductive ring surrounding the inputs, the guard, is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high voltage pins. Typical guard connections are shown in Figure 3.

The 14-pin dip configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

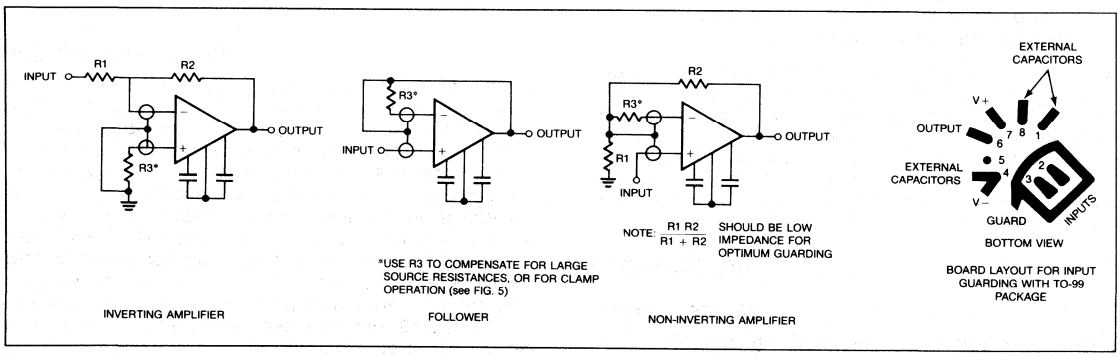


Figure 3. Input Guard Connection

Pin Compatibility

The 8-lead pin-out of the ICL7650 generally corresponds to that of the industry standard 8-pin devices, LM741, LM101, etc. However, the external null storage capacitors are connected to pins 1 and 8, whereas on most operational amplifiers these are left open or used for offset null or compensation capacitors.

The OP-05 and OP-07 operational amplifiers can be converted for ICL7650 operation. This can be accomplished by replacing the offset-null pot between pins 1 and 8, and V^+ by two capacitors from these pins to V^-. For LM 108 devices, the compensation capacitor is replaced by the external nulling capacitors.

Typical Applications

Figure 4 shows the ICL7650 automatically nulling the offset voltage of a high speed amplifier. The ICL7650 continuously monitors the voltage at the inverting input of the high speed amplifier, integrates the error, and drives the high speed amplifier's non-inverting input to correct for the offset voltage detected at the inverting input. The DC offset characteristics of the circuit are determined by the ICL7650, while the AC performance is determined by the high speed amplifier. While this circuit continuously and automatically adjusts the offset of the high speed amplifier to less than 5μV, it does not correct for errors caused by the input bias current, and R_F should be as low as is practical. This technique can be used with any operational amplifier that is configured as an inverting amplifier.

Figures 5 and 6 illustrate basic inverting and non-inverting amplifier circuits. An output clamping circuit is used in both circuits to enhance the overload recovery performance. The supply voltage (± 8V max) and the output drive capability (10KΩ load for full swing) are the only limitations on the replacement of other operational amplifiers by the ICL7650. By using a simple booster circuit, these limitations may be overcome (Figure 7). This enables the full output capabilities of the LM118 (or any other standard device) to be combined with the input capabilities of the ICL7650. The loop gain stability should be watched carefully when the feedback network is added, particularly when a slower amplifier such as the 741 is used.

A lower voltage supply is required when mixing the ICL7650 with circuits that operate at ±15V supplies. One approach is to use a highly-efficient voltage divider. This is illustrated in Figure 8 where the ICL7660 voltage converter is used to convert +15V to 7.5V.

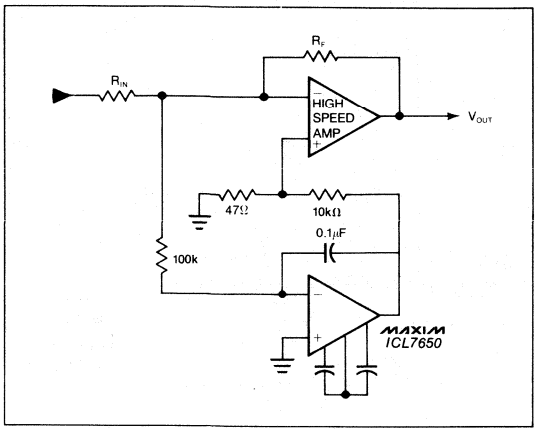


Figure 4. Nulling a High Speed Amplifier

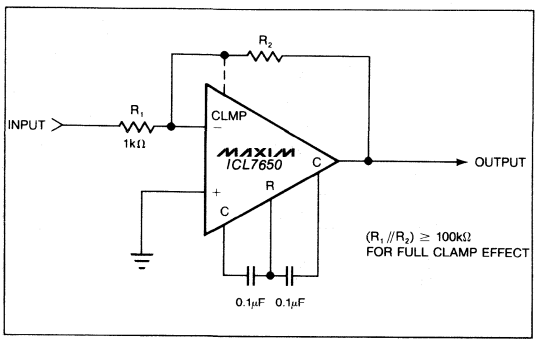


Figure 5. Inverting Amplifier with Optional Clamp

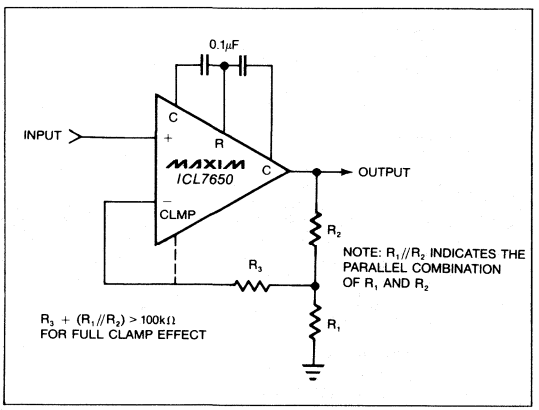


Figure 6. Non-Inverting Amplifier with Optional Clamp

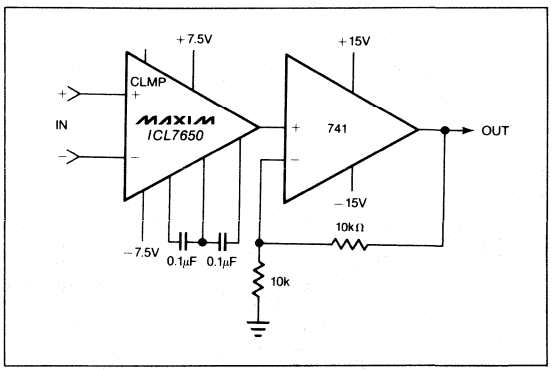


Figure 7. Using 741 to boost Output Drive Capability

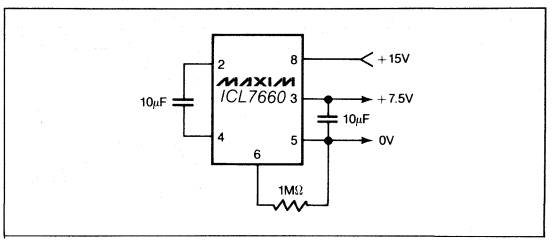
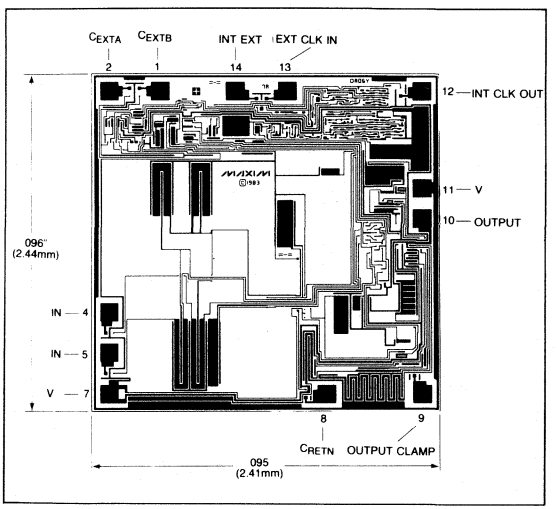


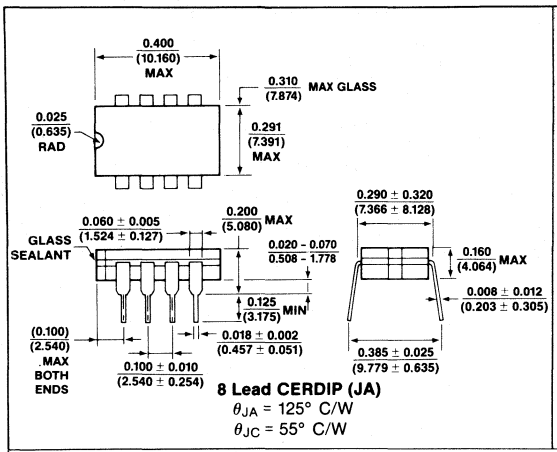
Figure 8. Splitting +15V with ICL7660 Same for −15V (95% Efficiency)

Chip Topography

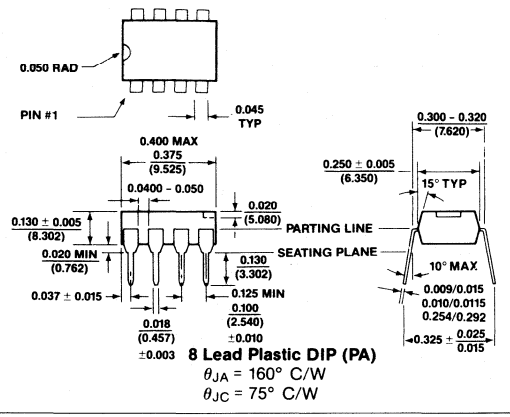


Chopper Stabilized Operational Amplifier

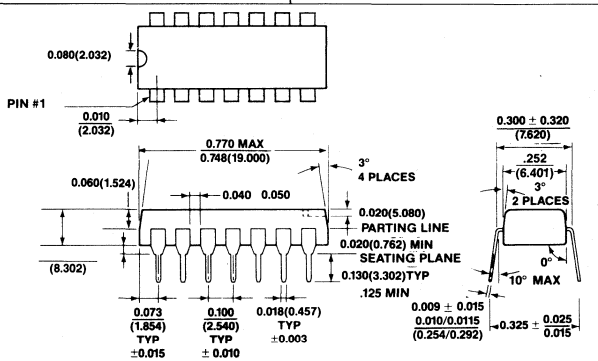
Package Information



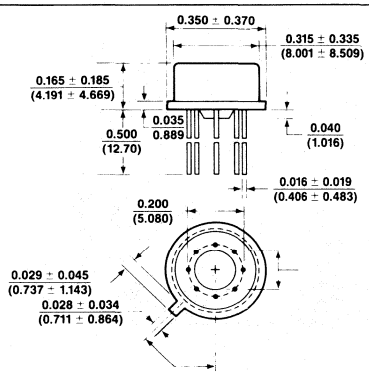
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



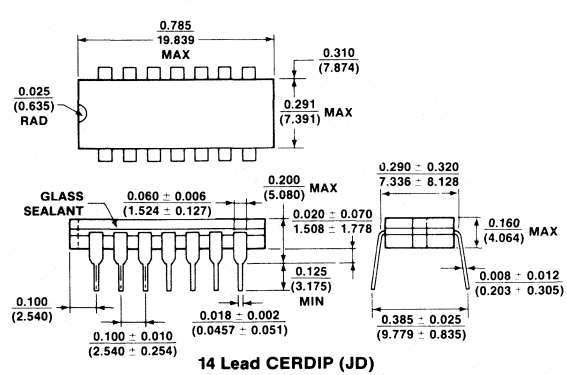
8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W



14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W

MAXIM
Chopper Stabilized Operational Amplifier

General Description

The Maxim ICL7652 is a chopper-stabilized amplifier, ideal for applications requiring low-level signal amplification and conditioning. This device offers distinct performance advantages over the ICL7650, including improved noise performance and a wider common-mode input voltage range. The bandwidth and slew rate are slightly reduced.

The ICL7652 virtually eliminates the V_{OS} error term in system error calculations, eliminating the reliability and cost problems associated with potentiometer adjustments. In addition, the 0.01μV/° C V_{OS} drift specification and the excellent long term offset stability eliminate the need for periodic V_{OS} trimming.

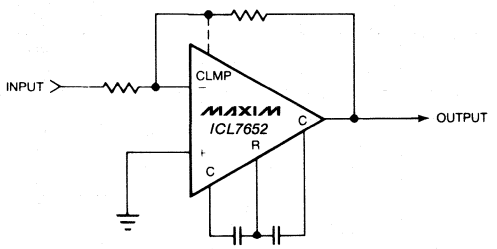
The offset nulling circuit for the 8-lead ICL7652 is controlled by an internal oscillator circuit. The 14-lead version offers the capability of connecting an external oscillator to control the V_{OS} nulling operation. The 14-lead device has an output voltage clamp circuit to minimize overload recovery time.

Applications

The ICL7652 is ideal for all preamplifier circuit applications where low offset voltage is critical and periodic adjustment of the offset is difficult or inaccessible.

Precision Amplifier
Instrumentation Amplifier
Thermocouple Amplifier
Thermistor Amplifier
Strain Gauge Amplifier

Typical Operating Circuit



Inverting Amplifier
with Optional Clamp

(Detailed Circuit Diagram — Figure 5)

Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Low Input Noise Voltage 0.2μV_{p-p}(DC-1Hz)**
- **Low Offset Voltage: 5μV Max.**
- **Low DC Input Bias Current: 30pA Max.**
- **High Gain, CMRR and PSRR (110dB Min.)**
- **Compensated for Unity Gain Operation**
- **Excellent Long Term Offset Stability (<100nV/$\sqrt{month}$)**
- **Monolithic, Low Power CMOS Design**

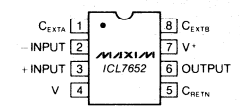
Ordering Information

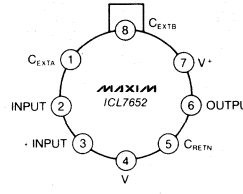
PART	TEMP. RANGE	PACKAGE
ICL7652CPA	0° C to +70° C	8 Lead Plastic DIP
ICL7652CPD	0° C to +70° C	14 Lead Plastic DIP
ICL7652CTV	0° C to +70° C	TO-99 Can
ICL7652IJA	-20° C to +85° C	8 Lead CERDIP
ICL7652IJD	-20° C to +85° C	14 Lead CERDIP
ICL7652ITV	-20° C to +85° C	TO-99 Can
ICL7652C/D	0° C to +70° C	Dice

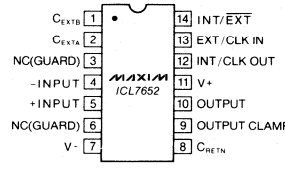
NOTE: All devices listed above are available in B versions. Order part number ICL7652B _ _ _.

Pin Configurations

Top View







NC = NO INTERNAL CONNECTION

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3) to (V^- – 0.3) V
Storage Temperature Range ..... –65°C to 160°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current into Any Pin 10mA
— while operating (Note 4) 100μA
Continuous Total Power Dissipation (T_A = +25°C)
CERDIP Package (Maxim) 500mW
Plastic Package 375mW
TO-99 ..... 250mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - ICL7652

(V^+ = +5V, V^- = –5V, T_A = +25°C, Test circuit unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{OS}	T_A = +25°C		±0.7	±5	μV
		Over Operating Temperature Range (Note 1)		±1.0		
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Operating Temperature Range (Note 1)		0.01	0.05	μV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_{BIAS}	T_A = +25°C		15	30	pA
		0°C ≤ T_A ≤ +70°C		35		
		–20°C < T_A < +85°C		100		
Input Offset Current	I_{OS}	T_A = +25°C		25	60	pA
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±4V,	120	150		dB
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common-Mode Voltage Range	CMVR		–4.3	–4.8 to +4.0	3.5	V
Common-Mode Rejection Ratio	CMRR	CMVR = –4.3V to +3.5V	110	130		dB
Power Supply Rejection Ratio	PSRR	±3V to ±8V	110	130		dB
Input Noise Voltage	$e_{n_{p-p}}$	R_S = 100Ω, DC to 1Hz		0.2		μV_{p-p}
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	I_{SUPP}	No Load		2.0	3.5	mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		–4.0V < V_{OUT} < +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

Note 1: Operating temperature range for I series parts is –20°C to +85°C, for C series is 0°C to +70°C.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this not guaranteed.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Chopper Stabilized Operational Amplifier

- **Key Parameters Guaranteed Over Temperature**
- **Lower Supply Current**
- **Improved ESD Protection (Note 5)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS This device conforms to the Absolute Maximum Ratings on adjacent page.

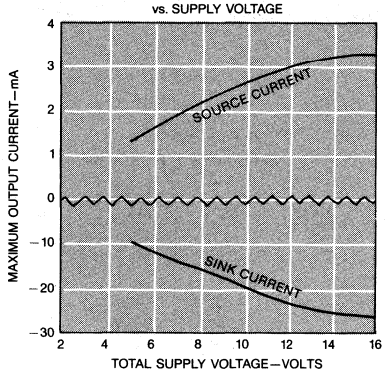
ELECTRICAL CHARACTERISTICS The ICL7652 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = +5V, V^- = -5V, T_A = +25°C, Test circuit, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	**V_{OS}**	T_A = +25°C		±0.7	±5.0	μV
		ICL7652 — Over Temperature Range		±1.0		
		ICL7652B (below)				
		-20°C ≤ T_A ≤ +40°C (Note 1)		**±1.0**	**±6.25**	
		-20°C ≤ T_A ≤ +70°C (Note 1, 7)		**±2.0**	**±7.25**	
		+70°C ≤ T_A ≤ +85°C (Note 1, 7)		**±5.0**	**±15**	
Average Temperature Coefficient of Input Offset Voltage (Note 1)	$\frac{\Delta V_{OS}}{\Delta T}$	ICL7652 — Over Temperature Range		0.01	0.05	μV/°C
		ICL7652B (below)				
		-20°C ≤ T_A ≤ +40°C		0.01	0.05	
		-20°C ≤ T_A ≤ +70°C (Note 1, 7)		0.01	0.1	
		+70°C ≤ T_A ≤ +85°C (Note 1, 7)		0.1	0.5	
Input Bias Current (Note 6) (Doubles every 10°C above approximately 60°C)	**I_{BIAS}**	T_A = +25°C		15	30	pA
		0°C ≤ T_A ≤ +70°C		**35**	**100**	
		-20°C ≤ T_A ≤ +85°C		**100**	**200**	
Input Resistance	R_{IN}			10^{12}		Ω
Large Signal Voltage Gain	**A_{VOL}**	R_L = 10kΩ, V_{OUT} = ±4V, T_A = +25°C	120	150		dB
		0°C ≤ T_A ≤ +70°C	**114**	**140**		
		-20°C ≤ T_A ≤ +85°C	**114**	**140**		
Output Voltage Swing (Note 3)	V_{OUT}	R_L = 10kΩ	±4.7	±4.85		V
		R_L = 100kΩ		±4.95		
Common-Mode Voltage Range	**CMVR**	**Over Temperature Range (Note 1)**	**-4.3**	**-4.8 to +4.0**	**3.5**	V
Common-Mode Rejection Ratio	**CMRR**	CMVR = -4.3V to +3.5V, T_A = +25°C	110	130		dB
		Over Temperature Range (Note 1)	**104**	**125**		
Power Supply Rejection Ratio	**PSRR**	±3V to ±8V, T_A = +25°C	110	130		dB
		Over Temperature Range (Note 1)	**104**	**125**		
Input Noise Voltage	en_{p-p}	R_S = 100Ω, DC to 1Hz		0.2		μV_{p-p}
		DC to 10Hz		0.7		
Input Noise Current	i_n	f = 10Hz		0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW			0.45		MHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ		0.5		V/μs
Rise Time	t_r			0.8		μs
Overshoot				20		%
Operating Supply Range	V^+ to V^-		5.0		16	V
Supply Current	**I_{SUPP}**	**No Load, T_A = +25°C**		**1.5**	**2.0**	mA
		Over Temperature Range (Note 1)		**2.0**	**3.5**	
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (DIP)		400		Hz
Clamp ON Current (Note 2)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 2)		-4.0V ≤ V_{OUT} ≤ +4.0V		1		pA
Offset Voltage vs Time				100		$nV/\sqrt{month}$

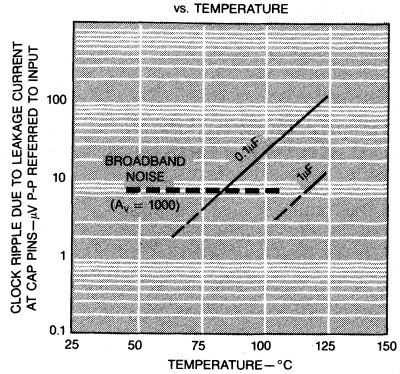
Note 1: Operating temperature range for "I" series parts is -20°C to +85°C, for C series is 0°C to +70°C. This parameter is guaranteed by test correlation.
Note 2: See OUTPUT CLAMP under detailed description.
Note 3: OUTPUT CLAMP not connected. See typical characteristics curves for output swing vs. clamp current characteristics.
Note 4: Limiting input current to 100μA is recommended to avoid latch-up problems. Typically 1mA is safe, however this is not guaranteed.
Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)
Note 6: $I_{OS} = 2 \cdot I_{BIAS}$.
Note 7: With $C_{EXTA} = C_{EXTB} = 1.0\mu F$

Chopper Stabilized Operational Amplifier

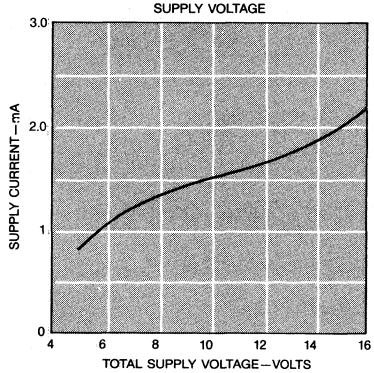
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



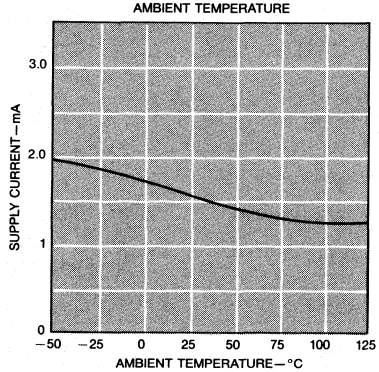
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



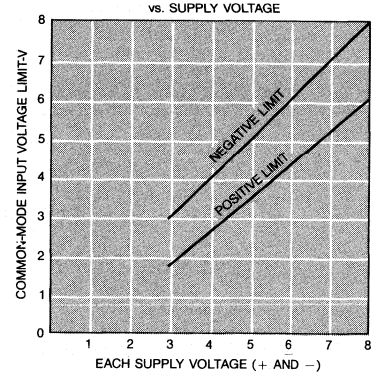
SUPPLY CURRENT vs. SUPPLY VOLTAGE



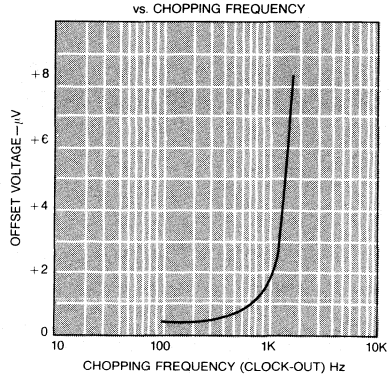
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



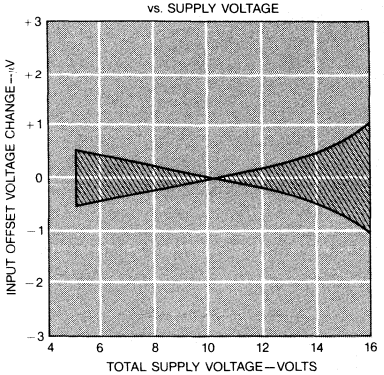
COMMON-MODE INPUT-VOLTAGE RANGE vs. SUPPLY VOLTAGE



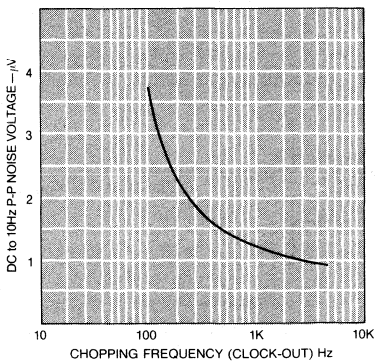
INPUT OFFSET VOLTAGE vs. CHOPPING FREQUENCY



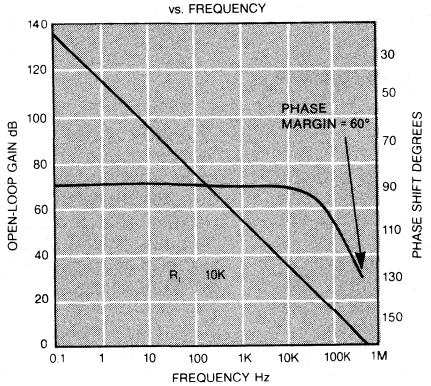
INPUT OFFSET VOLTAGE CHANGE
vs. SUPPLY VOLTAGE



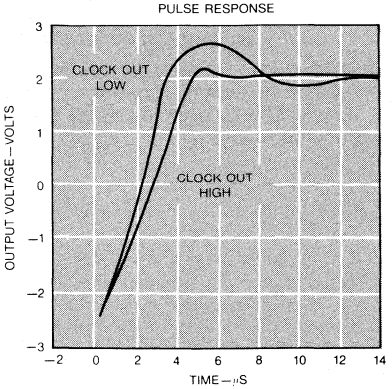
10Hz P-P NOISE VOLTAGE
vs. CHOPPING FREQUENCY



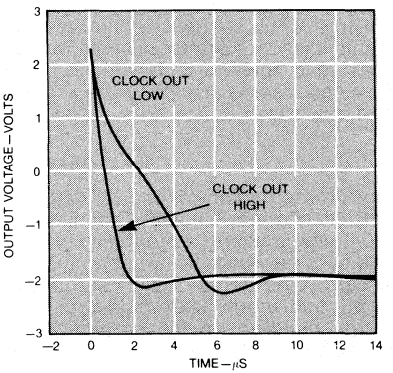
OPEN LOOP GAIN AND PHASE SHIFT
vs. FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



VOLTAGE FOLLOWER LARGE SIGNAL
PULSE RESPONSE



Chopper Stabilized Operational Amplifier

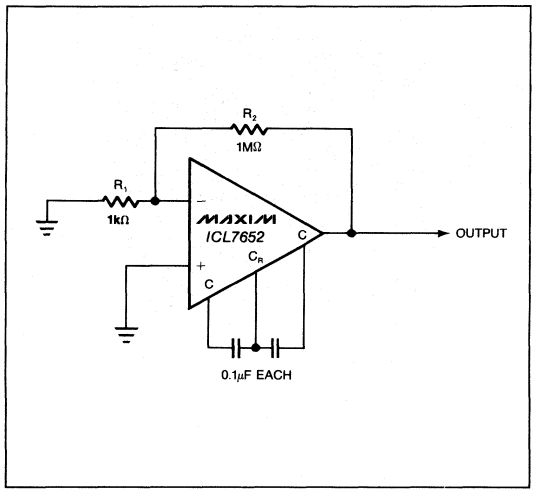


Figure 1. Maxim ICL7652 Test Circuit

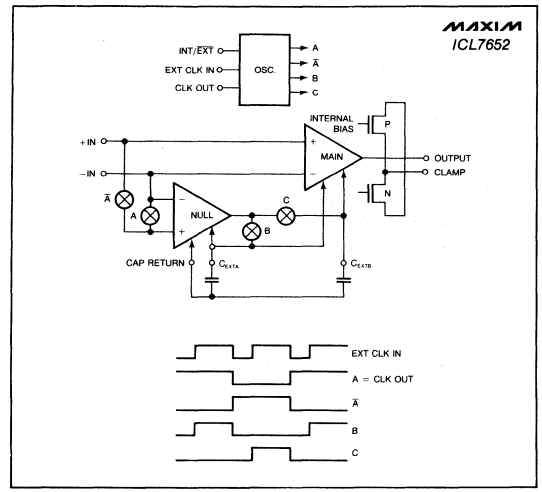


Figure 2. Maxim ICL7652 Block Diagram

Detailed Description

Amplifier

Figure 2 shows the major elements of the ICL7652. Two amplifiers are illustrated, the main amplifier and the nulling amplifier, both have offset-null capability. The main amplifier is connected full-time from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling arrangement, which is independent of the output level, operates over the full power supply and common mode ranges. This device exhibits exceptionally high CMRR, PSRR and A_{VOL}. The nulling connections, which are MOSFET back gates, have inherently high impedance. The two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants.

The chopper frequency charge injection at the input terminals is minimized by careful balance of the input switches. The feed forward-type injection into the compensation capacitor is also minimized. This is the main cause of spikes at the output in this type of circuit.

Output Clamp

This pin allows for reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the summing junction, or to the inverting input pin, a current path between this point and the output occurs just before the output device saturates. This avoids uncontrolled input differential and the consequent charge build-up on the correction-storage capacitors. There is only a slight reduction in the output swing.

Intermodulation

The effects of intermodulation between chopper frequency and input signals have been a problem with previous chopper stabilized amplifiers. These effects are present because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is detected by the zeroing circuit as an error signal. This signal is chopped and fed back, thus injecting sum and difference frequencies. This causes disturbances in the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652. This reduction is achieved by feeding the nulling circuit with a dynamic current which corresponds to the compensation capacitor current. The intermodulation and gain/phase disturbances in the ICL7652 are held to very low values, and generally can be ignored.

Nulling Capacitor Connection

The C_{EXTA} and C_{EXTB} pins should be connected to the null-storage capacitors, with the common connection made to the C_{RETN}. The outside foil of the capacitors should be connected to C_{RETN}.

Clock Operation

A frequency of 400Hz is generated by the internal oscillator of the ICL7652. This is available at the CLK OUT pin on the 14-lead device. The use of an external clock is also available on these parts. The INT/EXT pin may be left open for normal operation due to the internal pull-up. However, the internal clock must be disabled and this pin must be tied to V^- if an external clock is desired. An external clock signal may then be applied to the EXT CLK IN pin. The duty cycle of the external clock is not critical at low frequencies, since an internal divide by two provides the desired 50% switching duty cycle. However, a 50% to 80% positive duty cycle is preferred for frequencies above 500Hz, since the capacitors are charged only when EXT CLK IN is HIGH. This ensures that any transients have time to settle before the capacitors are turned OFF. The external clock can swing between V^+ and GROUND or V^+ and V^-, and has a logic threshold of about $V^+ - 2.5V$.

To avoid a capacitor imbalance during overload, a strobe signal may be used. Neither capacitor will be charged if a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier. A typical amplifier will drift less than $10\mu V/s$ since the leakage of the capacitor pins is quite low at room temperature. Relatively long measurements may be made with little change in offset.

Applications

Output Stage/Load Driving

The ICL7652 is in some ways like a transconductance amplifier whose open loop gain is proportional to load resistance. This behavior is apparent when loads are less than the high impedance stage of the output (approximately 18kΩ). The open loop gain, for example, will be 17dB lower with a 1kΩ load than with a 10kΩ load. This lower gain is of little consequence if the amplifier is used strictly for DC, since the DC gain is typically greater than 120dB even with a 1kΩ load. For wideband applications, however, the best frequency response will be achieved with a load resistor of 10kΩ or higher. The result will be a smooth 6dB/octave response from 0.1Hz to 0.5MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Component Selection

C_{EXTA} and C_{EXTB}, the two required external capacitors, have optimum values depending on the clock or chopping frequency. The correct value is 0.1 to 1μF for the preset internal clock frequency. The capacitor value should be scaled proportionally to the relationship between the chopping frequency and the nulling time constant if an external clock is used. A ceramic or other low grade capacitor may prove suitable for many applications, however, a high-quality film-type capacitor such as mylar is preferred. Low dielectric absorption capacitors (such as polypropylene) should be used for lowest settling on initial turn-on. Several seconds may be required to settle to 1μV with ceramic capacitors.

Static Protection

Input diodes provide static protection for all device pins. Strong static fields and discharges, however, should be avoided, as they can cause degraded diode junction characteristics which may result in increased input leakage currents.

Latch-up Avoidance

A parasitic four-layer (p-n-p-n) structure which has characteristics similar to an SCR is a characteristic of a junction-isolated CMOS circuit. This junction may be triggered into a low impedance state under certain circumstances which results in excessive supply current. In an effort to avoid this condition, no voltages greater than 0.3V beyond the supply rails should be applied to any pin. Generally the amplifier supplies should be established either at the same time or before any input signals are applied. However, if this is not possible, the drive circuits should limit the input current flow to under 1mA to avoid latch-up, even under fault conditions.

Thermo-electric Effects

Thermo-electric effects developed in thermocouple junctions of dissimilar metals, alloys, silicon, etc., ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/° C, but up to tens of μV/° C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide it is essential to take special precautions to avoid temperature gradients. All components should be shielded from air movement, especially that caused by power dissipating elements. Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

Chopper Stabilized Operational Amplifier

Input Guarding

Low leakage, high impedance, CMOS inputs allow the ICL7652 to make measurements of high impedance sources. Stray leakage paths can decrease input resistance and increase input currents unless inputs are guarded. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. The board should be coated with epoxy or silicone rubber after cleaning to prevent contamination.

Leakage currents may cause trouble even with properly cleaned and coated boards, particularly since the input pins are adjacent to pins that are at supply potentials. A significant reduction in leakage can be accomplished by using guarding to lower the voltage difference between the inputs and adjacent metal runs. By using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board, input guarding of the 8-lead TO-99 package is accomplished. A conductive ring surrounding the inputs, forming a guard, is connected to a low-impedance point that is approximately the same voltage as the inputs. The guard then absorbs the leakage current from the high voltage pins. Typical guard connections are shown in Figure 3.

The 14-lead DIP configuration has been specifically designed to ease input guarding. The pins adjacent to the inputs are not used.

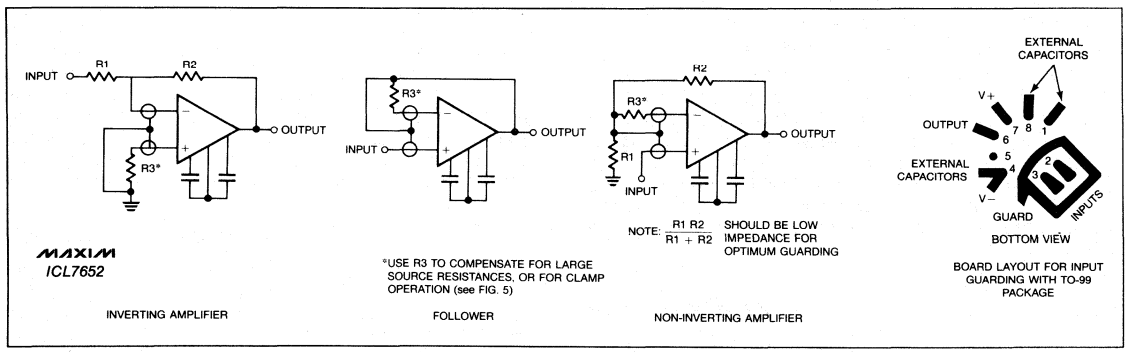


Figure 3. Input Guard Connection

Pin Compatibility

The 8-pin dip of the ICL7652 generally corresponds to that of the industry standard 8-pin devices, μA741, LM101, etc. However, the external null storage capacitors are connected to pins 1 and 8, whereas on most operational amplifiers these are left open or used for offset null or compensation capacitors.

The OP-05 and OP-07 operational amplifiers can also be converted for ICL7652 operation. This can be accomplished by replacing the offset-null potentiometer between pins 1 and 8, and V^+ by two capacitors from those pins to V^-. For LM108 pinout devices, the compensation capacitor is replaced by the external nulling capacitors.

Typical Applications

The ICL7652 is the optimal circuit solution whenever the performance of the system requires significant improvements in the reduction of the input offset voltage and bias currents. Figure 6 illustrates the use of a clamp circuit in a non-inverting amplifier. Since the clamp circuit forces the inverting input to follow the input signal, the usual problems in using a chopper-stabilized amplifier in this application are avoided.

Figures 5 and 6 illustrate basic inverting and non-inverting amplifier circuits. An output clamping circuit is used in both circuits to enhance the overload recovery performance. The supply voltage (± 8V max) and the output drive capability (10kΩ load for full swing) are the only limitations on the replacement of other operational amplifiers by the ICL7652. By using a simple booster circuit, these limitations may be overcome (Figure 7). This enables the full output capabilities of the μA741 (or any other standard device) to be combined with the input capabilities of the ICL7652. Because these devices form a composite amplifier, the loop gain stability should be watched carefully when the feedback network is added.

The provision for lower supply voltages is required when interfacing the ICL7652 with circuits that operate at ± 15V supplies. One approach is to use a highly-efficient voltage divider. This is illustrated in Figure 8 where Maxim's ICL7660 voltage converter is utilized in a backwards fashion.

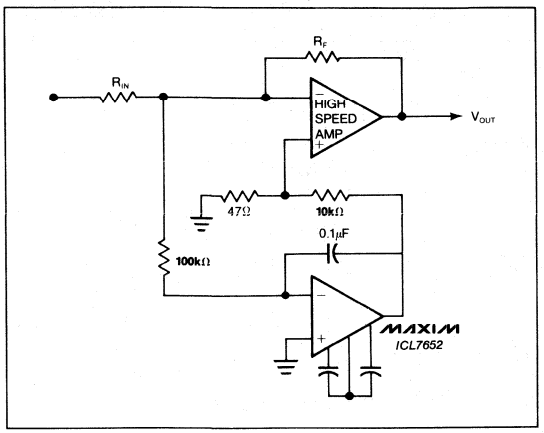


Figure 4. Nulling a High Speed Amplifier

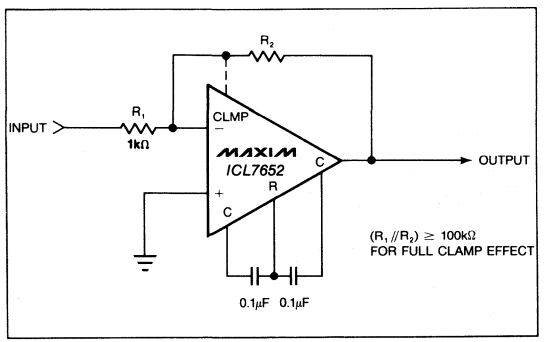


Figure 5. Inverting Amplifier with Optional Clamp

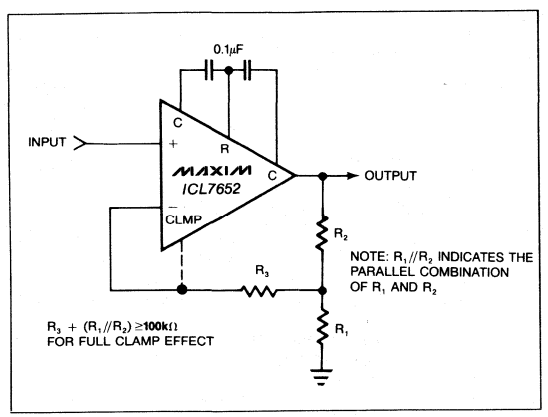


Figure 6. Non-Inverting Amplifier with Optional Clamp

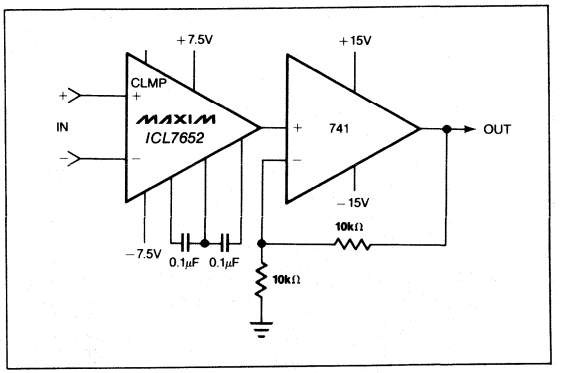


Figure 7. Using 741 to boost Output Drive Capability

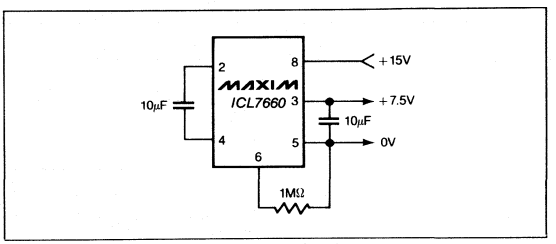
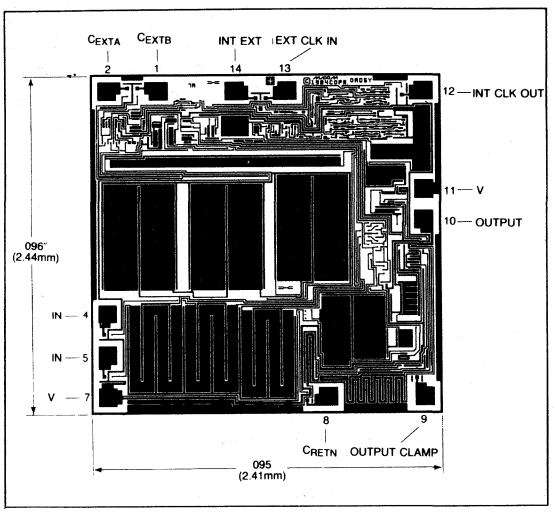


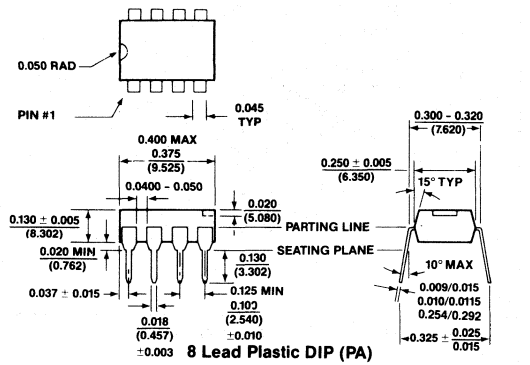
Figure 8. Splitting +15V with ICL7660 Same for −15V (95% Efficiency)

Chip Topography

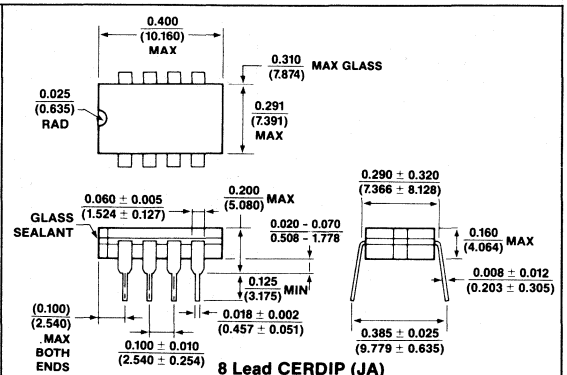


Chopper Stabilized Operational Amplifier

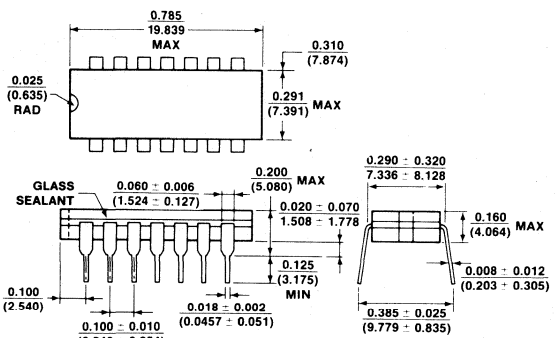
Package Information



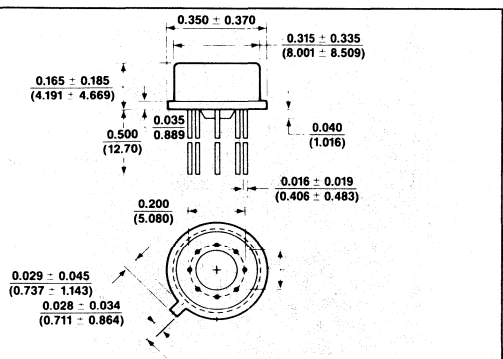
8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



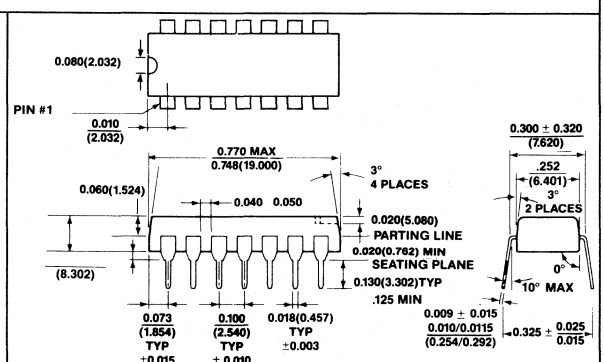
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W



14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W

Fast Buffer Amplifier

General Description

The LH0033A and LH0033 are high speed JFET input voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. With a slew rate of 1500 V/μsec when driving 1kΩ loads, the LH0033 will provide 100 mA output drive (250 mA peak), and can drive loads as low as 50Ω. In addition, phase linearity is characterized up to 20 MHz for video applications. Specifications are included for driving heavy coaxial cable loads not only at the normal 15 volt supplies, but also for 5V supplies.

The LH0033 family is intended to fulfill a wide range of buffer applications such as high-speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, operational amplifier isolation buffers for driving reactive loads and high input impedance buffers for high-speed analog to digital converters and comparators.

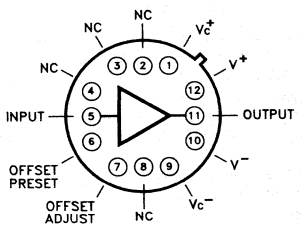
Guaranteed operation over temperature of the LH0033 family is achieved by using specially selected junction field effect transistors along with state-of-the art active laser trim techniques. They are available in the industry standard hermetic 12 Lead TO-8 metal Can.

Applications

Fast Sample/Hold Amplifiers
Flash A/D Input Buffering
Video Distribution
CRT Drive
Coaxial Line Driver

Pin Configuration

Top View



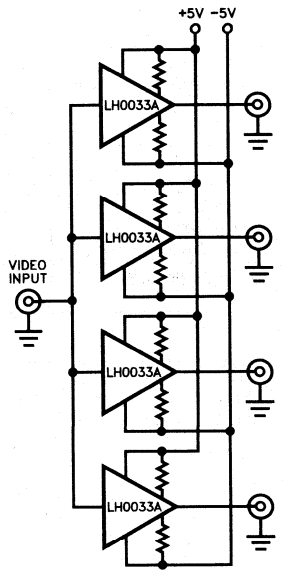
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Guaranteed operation at ±5V supplies**
- **1500 V/μs Slew Rate**
- **100 MHz Bandwidth**
- **2.9 ns Rise and Fall Times**
- **10^{11}Ω Input Impedance**
- **±5V to ±18V Supply Operation**

Ordering Information

PART	TEMP. RANGE	PACKAGE
LH0033AG	−55°C to +125°C	12 Lead TO-8
LH0033ACG	−25°C to + 85°C	12 Lead TO-8
LH0033G	−55°C to +125°C	12 Lead TO-8
LH0033CG	−25°C to + 85°C	12 Lead TO-8

Typical Operating Circuit



Low Loss 75Ω video distribution amplifier

(Detailed Circuit Diagram—Figure 7)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fast Buffer Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$) 40V
Maximum Power Dissipation (See Curves)
LH0033A/LH0033AC/LH0033/LH0033C 1.5W
Maximum Junction Temperature 175°C
Input Voltage $\pm V_S$
Continuous Output Current
LH0033A/LH0033AC/LH0033/LH0033C ±100 mA
Peak Output Current
LH0033A/LH0033AC/LH0033/LH0033C ±250 mA
Operating Temperature Range
LH0033A/LH0033 −55°C to +125°C
LH0033AC/LH0033C −25°C to +85°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) +300°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage	$R_S = 100\Omega$, $T_J = 25°C$, $V_{IN} = 0V$ (Note 2)		1	5		6	15		5.0	10		12	20	mV
	$R_S = 100\Omega$			10			20			15			25	mV
Offset Tempco	$R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	$V_{IN} = 0V$													
	$T_J = 25°C$ (Note 2)			100			250			250			500	pA
	$T_A = 25°C$ (Note 4)			1.5			2.5			2.5			5.0	nA
	$T_J = T_A = T_{MAX}$			7.5			10			10			20	nA
Voltage Gain	$V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0\ k\Omega$	0.97	0.98	1.00	0.96	0.98	1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V
Input Impedance	$R_L = 1.0\ k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	$V_{IN} = \pm 1.0V$, $R_L = 1.0k\Omega$		6.0	10		6.0	10		6.0	10		6.0	10	Ω
Output Voltage Swing	$V_I = \pm 14V$, $R_L = 1.0k\Omega$	±12			±12			±12			±12			V
	$V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25°C$	±9.0			±9.0			±9.0			±9.0			V
Supply Current	$V_{IN} = 0V$ (Note 5)		20	22		21	24		20	22		21	24	mA
Power Consumption	$V_{IN} = 0V$		600	660		630	720		600	660		630	720	mW

Note 1: LH0033A and the LH0033 are 100% production tested as specified at 25°C, 125°C, and −55°C. LH0033AC and LH0033C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033A and LH0033 are 100% production tested for this parameter. LH0033AC and LH0033C are sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25°C$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Fast Buffer Amplifier

- ◆ Full DC specifications at ±5V supplies
- ◆ Low Input Capacitance
- ◆ Guaranteed Offset Adjust Range
- ◆ 75Ω load specifications
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

DC ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Note 1)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage (Note 2)	R_S = 100Ω, T_J = 25°C, V_{IN} = 0V R_S = 100Ω, V_{IN} = 0V		1 	5 10		6 	15 20		5 	10 15		12 	20 25	mV mV
Offset Tempco	R_S = 100Ω, V_{IN} = 0V (Note 3)		50	100		50	100		50	100		50	100	µV/°C
Input Bias Current	V_{IN} = 0V, T_J = 25°C (Note 2) T_A = 25°C (Note 4) T_J = T_A = T_{MAX}			100 1.5 7.5			250 2.5 10			250 2.5 10			500 5.0 20	pA nA nA
Voltage Gain	V_O = ±10V, R_S = 100Ω, R_L = 1 kΩ V_{IN} = ±10.5V, R_S = 100Ω, R_L = 100Ω V_{IN} = ±2V, R_S = 100Ω, R_L = 75Ω	0.97 0.86 0.84	0.98 0.95 0.95	1.00 1.00 1.00	0.96 0.86 0.84	0.98 0.95 0.95	1.00 1.00 1.00	0.97	0.98	1.00	0.96	0.98	1.00	V/V V/V V/V
Input Impedance	V_{IN} = ±1V, R_L = 1 kΩ, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	V_{IN} = ±1V, R_L = 1 kΩ		6	10		6	10		6	10		6	10	Ω
Output Voltage Swing	V_{IN} = ±14V, R_L = 1 kΩ V_{IN} = ±10.5V, R_L = 100Ω, T_A = 25°C	±12 ±9			±12 ±9			±12 ±9			±12 ±9			V V
External Offset Resistance	V_{OS} = 0 mV, T_A = 25°C (Note 7)	0	75	200	0	75	200							Ω
Supply Current (Note 5)	V_{IN} = 0V		20	22		21	24		20	22		21	24	mA
Power Consumption	V_{IN} = 0V		600	660		630	720		600	660		630	720	mW

DC ELECTRICAL CHARACTERISTICS

V_S = ±5V, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified.

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Offset Voltage (Note 2)	R_S = 100Ω, T_J = 25°C, V_{IN} = 0V		10	15		12	20							mV
Input Bias Current	V_{IN} = 0V, T_J = 25°C (Note 2) V_{IN} = 0V, T_A = 25°C (Note 4)			100 300			250 750							pA pA
Voltage Gain	V_O = ±1V, R_S = 100Ω, R_L = 1kΩ V_O = ±1V, R_S = 100Ω, R_L = 75kΩ	0.92 0.84	0.96 0.91	1.00 1.00	0.92 0.84	0.96 0.91	1.00 1.00							V/V V/V
Input Impedance	V_{IN} = ± 1V, R_L = 1kΩ, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}								Ω
Output Impedance	V_{IN} = ±1V, R_L = 1kΩ		6	10		6	10							Ω
Output Voltage Swing	V_{IN} = ±4V, R_L = 75Ω, T_A = 25°C	±2	±3.4		±2	±3.4								V
Supply Current	V_{IN} = 0V		16	20		16	20							mA
Power Consumption	V_{IN} = 0V		160	200		160	200							mW

Refer to notes 1-6 on adjacent page.

Note 7: Offset adjust resistor connects between device pin 7 and V — as shown in Figure 2.

Fast Buffer Amplifier

AC ELECTRICAL CHARACTERISTICS

T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1.0 kΩ (Note 6)

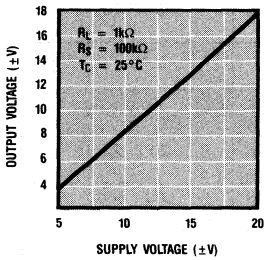
Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1.0 Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2			2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f > 1 kHz		<0.1			<0.1			<0.1			<0.1		%

Refer to notes 1-7 on second and third page of this data sheet.

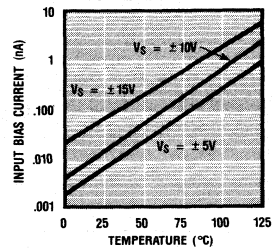
The electrical characteristics above are a reproduction of a portion of National Semiconductor Corporation's copyrighted (1984) Linear data book supplement. This information does not constitute any representation by Maxim that NSC's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Typical Operating Characteristics

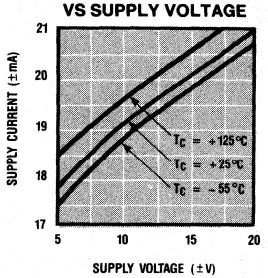
LH0033 OUTPUT VOLTAGE VS SUPPLY VOLTAGE



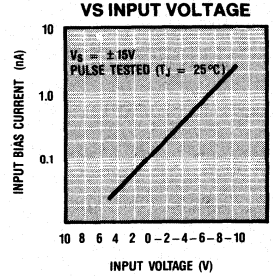
LH0033 INPUT BIAS CURRENT VS TEMPERATURE



LH0033 SUPPLY CURRENT VS SUPPLY VOLTAGE



LH0033 INPUT BIAS CURRENT VS INPUT VOLTAGE



AC ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

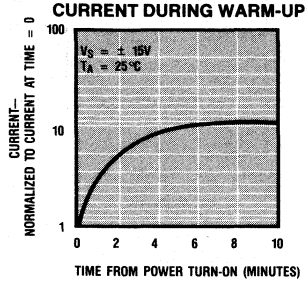
T_C = 25°C, V_S = ±15V, R_S = 50Ω, R_L = 1.0 kΩ (Note 6)

Parameter	Conditions	LH0033A			LH0033AC			LH0033			LH0033C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Slew Rate	V_{IN} = ±10V	1000	1500		1000	1400		1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1.0 Vrms		100			100			100			100		MHz
Phase Non-Linearity	BW = 1.0 Hz to 20 MHz		2.0			2.0			2.0			2.0		degrees
Rise Time	ΔV_{IN} = 0.5V		2.9			3.2			2.9			3.2		ns
Propagation Delay	ΔV_{IN} = 0.5V		1.2			1.5			1.2			1.5		ns
Harmonic Distortion	f = 1kHz		<0.1			<0.1			<0.1			<0.1		%

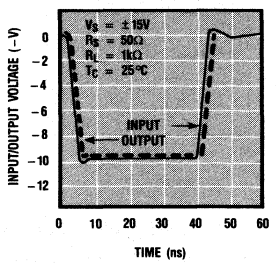
Refer to notes 1-7 on second and third page of this data sheet.

Typical Operating Characteristics

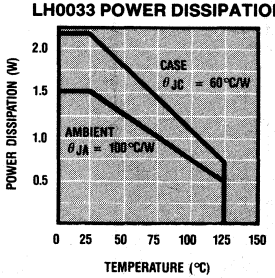
LH0033 NORMALIZED INPUT BIAS CURRENT DURING WARM-UP



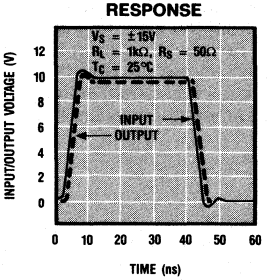
LH0033 NEGATIVE PULSE RESPONSE



LH0033 POWER DISSIPATION



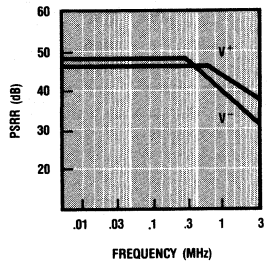
LH0033 POSITIVE PULSE RESPONSE



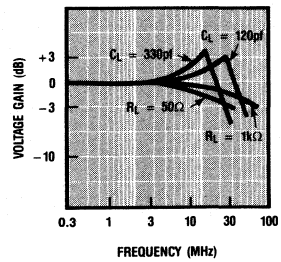
Fast Buffer Amplifier

Typical Operating Characteristics

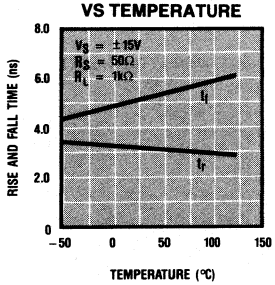
LH0033 POWER SUPPLY REJECTION RATIO



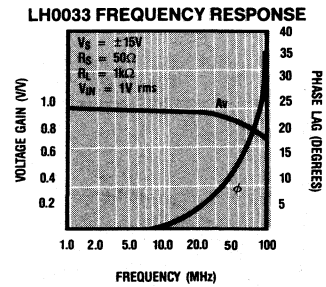
LH0033 FREQUENCY RESPONSE FOR VARIOUS LOADS



LH0033 RISE AND FALL TIME VS TEMPERATURE



LH0033 FREQUENCY RESPONSE



Detailed Description

The LH0033 combines a JFET input stage with a high current bipolar output stage. Also included is the biasing network and laser trimmed resistors for supply current and offset voltage adjustments.

The n-channel JFET Q1 has very low input current, less than 10 nA at V_{IN} = 0V and T_J = 125°C. The source of Q1 will be offset from the input voltage by the V_{GS} voltage of Q1. The output is offset from the Q1 source voltage by the IR drop across R1 and the V_{BE} of Q5. The output offset voltage has been actively laser trimmed during assembly to meet the guaranteed maximum offset specification.

Transistors Q2 and Q3 provide a two V_{BE} voltage difference between the bases of the two output transistors, setting the quiescent current through Q5 and Q6. Resistors R3 and R4 provide a small amount of degeneration to stabilize the quiescent current over temperature. Q4 is another n-channel JFET, similar to Q1. Q4 acts as a current sink for the current flowing through the input stage (Q1, R1, Q2, and Q3). The voltage drop across diode D1 and resistor R2 is equal to the drop across R1 and the base-emitter junction of Q5.

LH0033/LH0033C

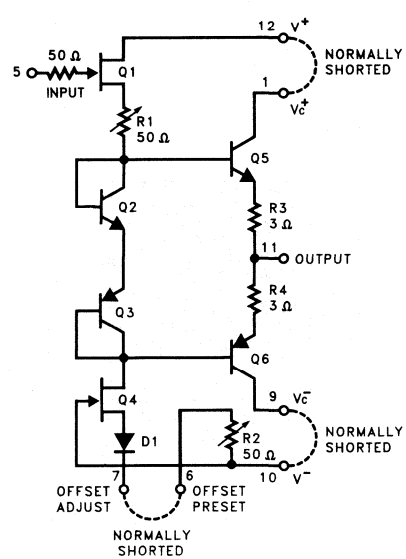


Figure 1. Internal Schematic Diagram

Since Q2 is matched to Q5 and Q3 is matched to Q6, approximately one-half of the quiescent current flows in the input stage, with the remaining quiescent current flowing through the output transistors. This means that the output stage will be operating as a class A amplifier with output currents less than 10 mA. Above this current, the output stage operates in a class B mode, with slightly increased nonlinearity.

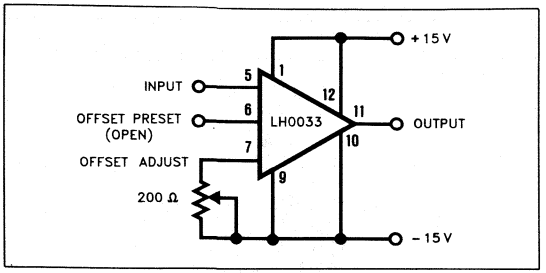


Figure 2. Offset Zero Adjust for LH0033

Applications

Layout Precautions

The LH0033 should be treated as a high frequency amplifier when designing a printed circuit layout. Power supply bypassing to a ground plane with low inductance capacitors should be within a half inch of the device. For applications where the input capacitance is critical, connect the case of the device to the output so that the case capacitance is bootstrapped. For most applications, the case may be left unconnected or grounded. There is no internal connection to the case.

Offset Voltage Adjustment

For most applications, connect pin 6 to pin 7, and the offset voltage will be guaranteed to within the actively trimmed specification. When this is not sufficient, or there is a system offset to be absorbed, an external 200Ω trim pot may be connected from pin 7 to V^-, as illustrated in Figure 2.

Operation Within an Op Amp Loop

The LH0033 may be used as a current booster within the feedback loop of almost any operational amplifier with only a few cautions: remember that the output is not internally short circuit protected, and many applications will require one of the short circuit protection circuits discussed below.

Short Circuit Protection

The LH0033 is not internally short circuit protected as most of the possibilities involve some compromise in output swing or transient response. The output stage collectors are available separately, however, so there are several options open to the user. The simplest and most commonly used is the simple resistor in each output stage collector (Figure 3). For worst case protection these resistors may be calculated by:

$$R_{LIM} = V^+/100\ mA = V^-/100\ mA$$
$$= 150\Omega \text{ for } \pm 15V \text{ supplies}$$

Unfortunately, a resistor that large severely restricts the voltage swing into a heavy load and the slew rate into a capacitive load. Decoupling the V_{C+} and V_{C-} pins with capacitors will retain full output swing for transient pulses, but if the capacitors are made too large, (to hold up long pulses) the protection is lost.

An alternative active current limit circuit is shown in Figure 4. This technique retains full DC output swing. The current sources are set to a safe limit and are normally saturated, thus applying full supply voltage to the V_C pins. In the event of a short on the output, the current source comes into operation and reduces the output stage collector voltage as required to keep the current to a safe level. The output stage collectors may be bypassed with a small capacitor to give additional current capacity for short times, as would be required in driving a capacitive load.

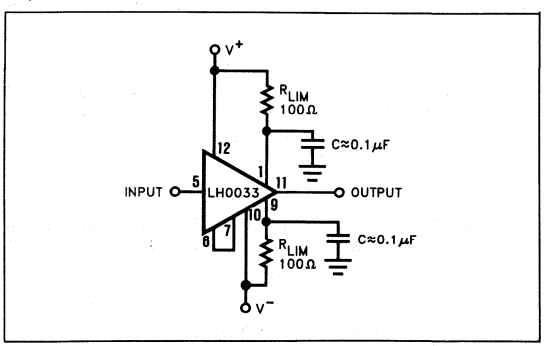


Figure 3. LH0033 Using Resistor Current Limiting

Operation from Single or Asymmetrical Power Supplies

Since the LH0033 has no ground pin, an asymmetrical power supply is indistinguishable from a symmetrical supply with a DC level on the input. (The single supply case is simply the asymmetrical case taken to the extreme of one of the supplies being zero.) In either case, an offset error will be generated corresponding directly to the gain of the circuit times the apparent DC level with respect to a pseudo ground point half-way between the supplies.

$$\text{Offset Voltage} = 0.5(1 - \text{gain})(|V^+| - |V^-|)$$

For example, a device operating on supplies of +5V and −12V would have an apparent offset error due to the gain of about −35 mV. This could be easily corrected with an offset adjust potentiometer connected from pin 6 to V^- as discussed in the offset voltage adjustment section.

Fast Buffer Amplifier

Operation from ±5V Power Supplies

The original LH0033 was characterized and guaranteed to operate at ±15 volt power supplies only, but many applications can save substantial power by operating the device from reduced supplies. The Maxim LH0033A and LH0033AC are specified and tested for gain, swing, offset voltage, bias current and supply current at ±5V power supplies as well as the standard ±15V.

Capacitive Loading

The LH0033 is designed to drive heavy capacitive loads without susceptibility to oscillation. Note that the absolute maximum current rating must still be observed, thus the output slew rate times the load capacitance must be less than 250 mA. For example, a 1000 V/μs slew rate with a 250 pF load would fall just within the absolute maximum peak current specification. If a heavier capacitive load needs to be driven, the slew rate must be externally limited.

$$\text{Slew Rate} \leq I_{OUT(MAX)}/C_{LOAD} \leq \pm 250\ \text{mA}$$

Power dissipation resulting from capacitive load currents must be considered independently. The real power dissipated in a circuit driving a sine wave into a pure capacitive load is:

$$P_{AC} = (V_{P-P})^2 \times \text{Frequency} \times C_1$$

This dissipation adds directly to the devices quiescent power and any DC load power that might be present. The sum of all these terms must be less than the absolute maximum power rating at the temperature of operation.

$$P_{DC} + P_{AC} \leq P_{DISS(PKG)}$$

For example, a 250 pF load driven to 20V peak to peak at 1 MHz adds a reactive power dissipation in the LH0033 of:

$$P_{AC} = (20)^2 \times 10^6 \times 250 \times 10^{-12} = 100\ \text{mW}$$

This term is not often a severe application problem with the LH0033.

Power Dissipation Considerations

The LH0033 package is rated for 0.5W in still air at 125°C and 0.75W with an infinite heat sink. Since the quiescent power is in the neighborhood of 600 mW, a heat sink is needed for most 125°C applications and some heavy load applications at lower temperatures. Several suitable commercial heat sinks are available including the Thermalloy 2241, the Wakefield 215CB and the IERC UP-TO8-48CB. Please note that the can diameter is 0.55 inches nominal as opposed to the JEDEC TO-8 which is 0.45 inches nominal. (See the outline drawing for detailed dimensions)

Typical Applications

Output Buffer within an Op Amp Loop

The low output impedance, high slew rate, wide power bandwidth, and low phase shift of the LH0033 make it ideally suited for use as an output buffer for operational amplifiers. When using the LH0033 as an op amp buffer, the total phase shift of both the op amp and the LH0033 buffer must be considered when checking for loop stability. With typically only 10 degrees of phase shift at 50 MHz, the LH0033 can be used with all but the very fastest op amps. With an output impedance of less than 10Ω, the LH0033 can drive large inductive or capacitive loads with little additional phase shift.

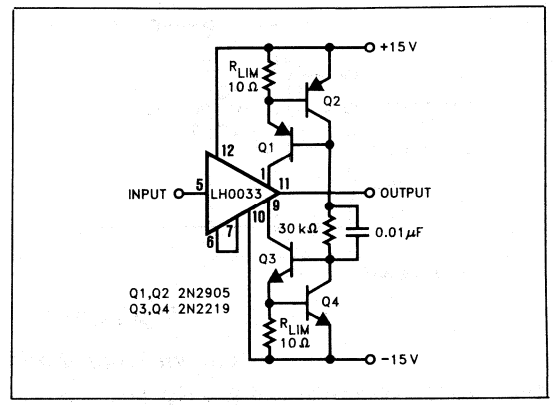


Figure 4. LH0033 Current Limiting Using Current Sources

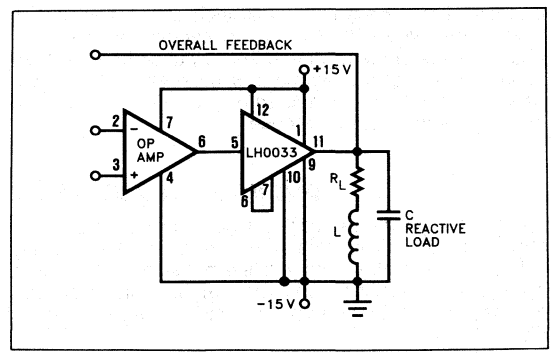


Figure 5. Isolation Buffer

Coaxial Cable Driver

With an input resistance of $10^{11}\Omega$ and input capacitance of 4 pF, the LH0033 places negligible load on a 50 or 75Ω video source. The Maxim LH0033A is guaranteed for operation with ±5V power supplies common in video systems, and is also specified for a minimum ±2V swing into a 75Ω load. The LH0033 typically has only 2 degrees of phase non-linearity over the frequency range of 1 to 20 MHz. The 68Ω resistor on the output can be shorted out if a higher output voltage is required, but this causes a misermination of the 75Ω cable, and reflections will not be absorbed by the coaxial driver output.

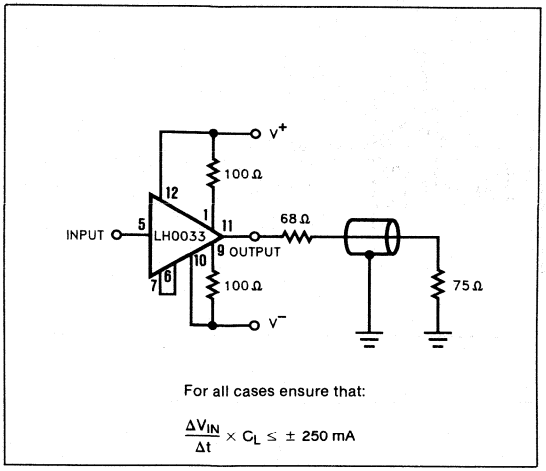


Figure 6. Coaxial Cable Driver

Video Distribution Amplifier

Figure 7 and the front page of this data sheet show a video distribution amplifier capable of driving a number of 75Ω output lines from a single source with very low signal loss. The entire amplifier operates from ±5V supplies with a total power dissipation of 640 mW plus the output power. The input resistance will be in the thousands of megohms and will be negligible in most situations. The input capacitance, however, should be considered as it may result in high frequency misterminations at the input. The voltage gain of the LH0033A and the LH0033AC is specified at 0.91 typ, 0.84 min (±5V supplies and 75Ω load), so the worst case insertion loss of the distribution amplifier is 1.5 dB with a typical under 1dB. Protection resistors are included in series with pins 10 and 12 of each device so that the distribution amplifier will be able to tolerate momentary overloads on the outputs.

Figure 8 is a similar video distribution amplifier which has output resistance of 75Ω to back terminate the outputs. The back termination resistor is selected to be 68Ω to account for the typical 6Ω output resistance of the LH0033. Because each 75Ω load is isolated from the buffer amplifier, each device is able to drive two loads. The voltage loss through this amplifier will be approximately 6 dB. Note that protection resistors are unnecessary in the back terminated configuration, as the LH0033 can safely drive the 68Ω termination resistor even if the cable is shorted.

High Speed Sample/Hold

In Figure 9, the first LH0033 buffers the input and drives the sample capacitor through the FET, Q1, whenever the Sample/Hold logic input is in the sample mode. When the logic input changes to the hold mode, Q1 opens up, isolating the hold capacitor from the input LH0033, and the output voltage no longer follows the input. The second LH0033 buffers and isolates the sample capacitor voltage from the load. Since the input bias current of the LH0033 is typically less than 1 nanoamp, the droop rate of this sample and hold will be less than 1 mV/ms.

Since the LH0033 has a slew rate of 1500 V/μs and a 100 MHz bandwidth, this LH0033-based sample and hold is well suited for use with video speed flash A/D converters.

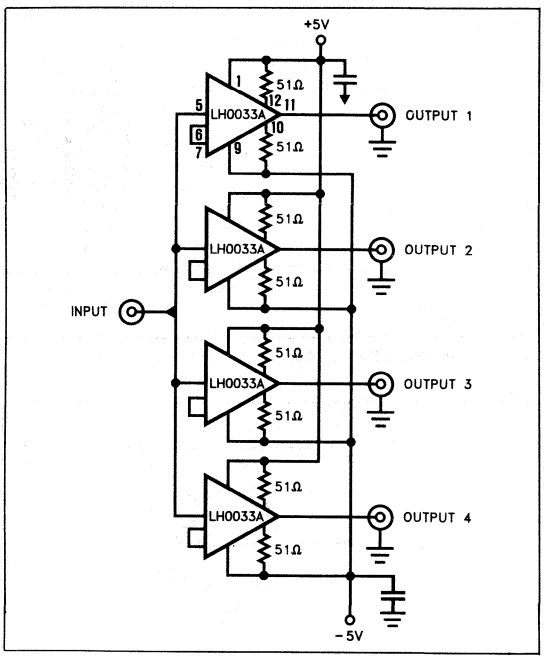


Figure 7. Low Loss 75Ω Video Distribution Amplifier

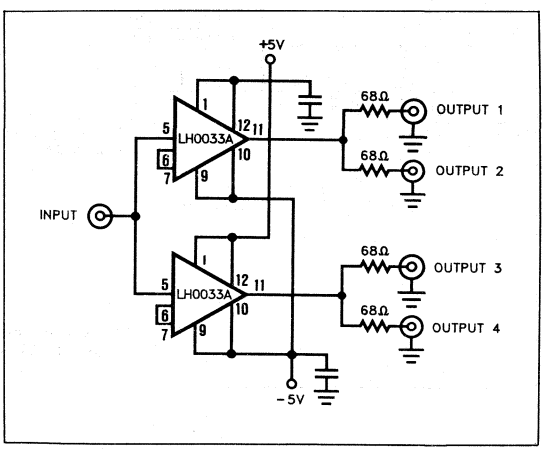


Figure 8. Back Terminated 75Ω Video Distribution Amplifier

Fast Buffer Amplifier

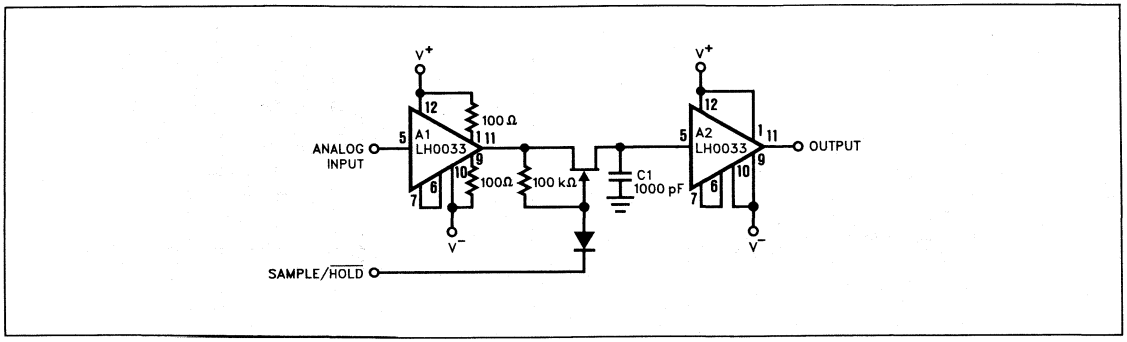


Figure 9. High Speed Sample/Hold

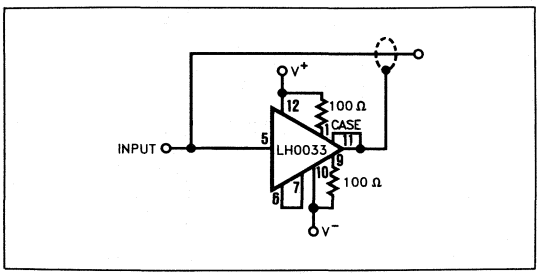


Figure 10. Instrumentation Shield/Line Driver

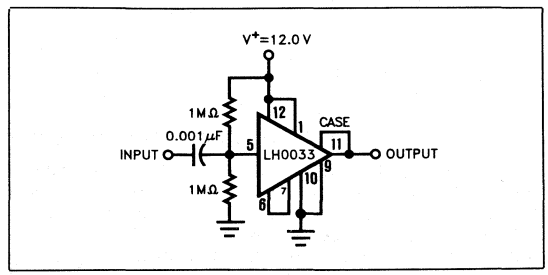
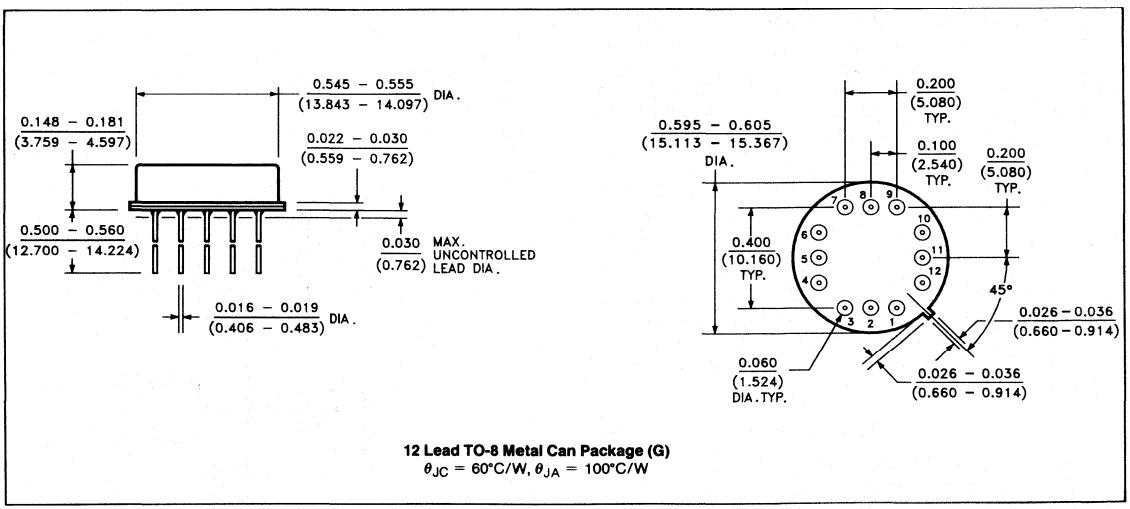


Figure 11. Single Supply AC Amplifier

Package Information



12 Lead TO-8 Metal Can Package (G)
θ_{JC} = 60°C/W, θ_{JA} = 100°C/W

MAXIM
Power Operational Amplifier

General Description

The Maxim LH0101 Power Operational Amplifier delivers up to 5A peak output current. Packaged in a rugged TO-3 case, the LH0101 combines the ease of use and performance of a FET input op amp with the power handling capabilities of a 5A output stage. The short circuit output current limit protection feature makes this device ideal for driving AC and DC motors, large capacitive loads, and electromagnetic actuators. The output stage virtually eliminates crossover distortion while using very little quiescent power.

The LH0101 is a wideband amplifier, with a full power bandwidth of 300kHz and a gain bandwidth of 5MHz.

Features

- **Pin for Pin 2nd Source!**
- **5 Amp Peak, 2 Amp Continuous Output Current**
- **Virtually No Crossover Distortion**
- **300 kHz Power Bandwidth**
- **850 mW Standby Power (±15V supplies)**
- **300 pA Input Bias Current**
- **10 V/μs Slew Rate**
- **5 MHz Gain Bandwidth**
- **2 μs Settling Time to 0.01%**

Applications

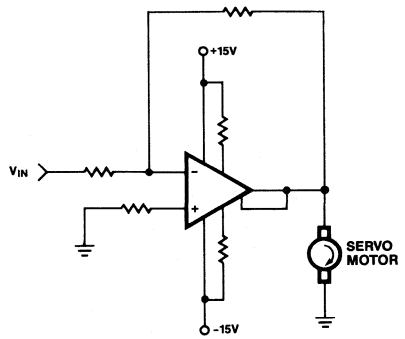
The LH0101 is well suited for applications requiring both standard op amp performance and high current output capability:

DC Motors
AC Motors
Actuators
Coaxial Cable Drivers
Programmable Power Supplies

Ordering Information

PART	TEMP. RANGE	PACKAGE
LH0101CK	-25°C to +85°C	TO-3 Can
LH0101K	-55°C to +125°C	TO-3 Can
LH0101ACK	-25°C to +85°C	TO-3 Can
LH0101AK	-55°C to +125°C	TO-3 Can

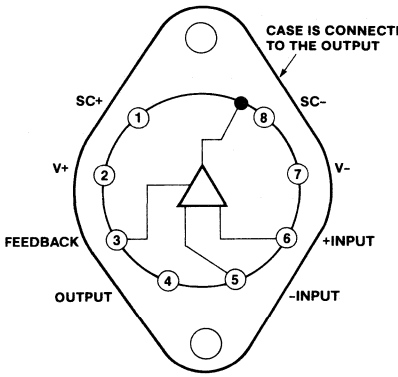
Typical Operating Circuit



DC Servo Motor Driver

Pin Configuration

Top View



Display Drivers/Counters

MAXIM

Four Digit Display Decoder/Drivers

General Description

The Maxim ICM7211 (LCD) and ICM7212 (LED) four digit, seven segment display drivers include input data latches, BCD to segment decoders, and all level translation and timing circuits needed to drive non-multiplexed displays.

Both the ICM7211 and ICM7212 are available in two data input configurations: a multiplexed BCD interface version and a microprocessor interface version. The multiplexed BCD interface version has four BCD data inputs and four separate digit strobes. The microprocessor interface versions, designated by an "M" suffix, have four BCD data inputs, two digit address lines, and two chip selects or WRITE inputs.

The ICM7211 and ICM7212 decode the BCD data via an onboard character font ROM. There are two different character fonts available, hexadecimal and Code B.

Applications

The low power consumption of the ICM7211 LCD driver makes it ideal for battery powered and portable applications. The ICM7212 LED display driver reduces system cost by eliminating external level translators, external segment drivers, and segment current limiting resistors.

Digital Panel Displays
Intelligent Instruments
Remote Display Units
Microprocessor-to-Visual Communication

Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Directly drives Four Digit, 7 Segment Displays**
  ICM7211 - Non-multiplexed Liquid Crystal Display (LCD)
  ICM7212 - Non-multiplexed Common Anode LED

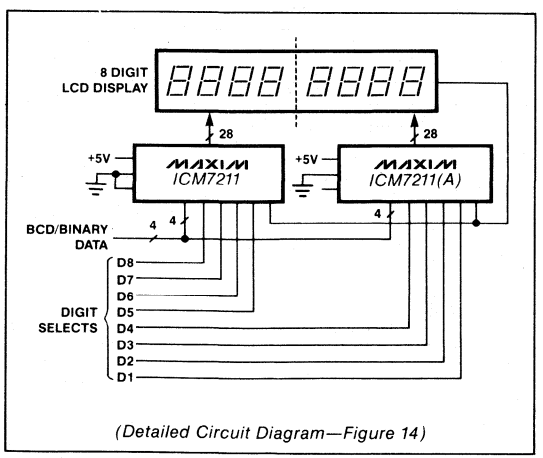
  Multiplexed BCD Interface and μP Interface Versions
- **No external components needed**
- **Low Power CMOS - 25μW typ. (display blanked)**

Ordering Information

DEVICE TYPE	OUTPUT CODE	INPUT CONFIGURATION
ICM7211 (LCD)	Hexadecimal	Multiplexed 4-Bit
ICM7211A (LCD)	Code B	
ICM7211M (LCD)	Hexadecimal	μP Interface
ICM7211AM (LCD)	Code B	
ICM7212 (LED)	Hexadecimal	Multiplexed 4-Bit
ICM 7212A (LED)	Code B	
ICM7212M (LED)	Hexadecimal	μP Interface
ICM7212AM (LED)	Code B	

(Ordering information continued).

Typical Operating Circuit

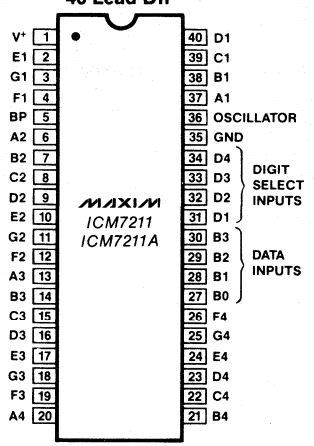


(Detailed Circuit Diagram—Figure 14)

Pin Configurations

Top View

40 Lead DIP



(Pin Configurations continued)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Four Digit Display Decoder/Drivers

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W@ 70°C
Supply Voltage 6.5V
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, GROUND -0.3V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V; T_A = 25°C, Test circuit unless noted)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	I_{OP}	Test circuit, Display blank		10	50	µA
Oscillator Input Current	I_{OSCI}	Pin 36		±2	±10	
Segment Rise/Fall Time	t_{RFS}	C_L - 200pF		0.6		µs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{BP}	Pin 36 Floating		125		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pin 27-34 - GROUND		10	50	µA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment On Current	I_{SEG}	Segment On, V_O = +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}		3			V
Logical "0" input voltage	V_{IL}				1	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	µA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	µA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			µs
Data Setup Time	t_{DS}		500			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			µs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1981) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Four Digit Display Decoder/Drivers

- ♦ Key Parameters Guaranteed Over Temperature
- ♦ Low Power (Typically 25μW)
- ♦ Increased Segment-On Current
- ♦ Maxim Quality and Reliability
- ♦ Improved ESD Protection (Note 3)

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = +5V; T_A = 25°C, Test circuit unless noted.)

ICM7211 CHARACTERISTICS (LCD)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		3	5	6	V
Operating Current	**I_{OP}**	**Test circuit, Display blank**		**5**	**25**	**μA**
Oscillator Input Current	I_{OSCI}	Pin 36, V_{OSC} = 2.5V		±2	±10	μA
Segment Rise/Fall Time	t_{RFS}	C_L = 200pF		0.5		μs
Backplane Rise/Fall Time	t_{RFB}	C_L = 5000pF		1.5		
Oscillator Frequency	f_{OSC}	Pin 36 Floating		19		kHz
Backplane Frequency	f_{BP}	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{SUPP}		4	5	6	V
Operating Current Display Off	I_{OP}	Pin 5 (Brightness), Pin 27-34 - GROUND		5	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment On Current	**I_{SEG}**	**Segment On, V_O = +3V; T_A = 25°C 0°C ≤ T_A ≤ +70°C**	**6 5**	**9**		**mA**

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" input voltage	**V_{IH}**	**Pins 27-34, 0°C ≤ T_A ≤ +70°C**	**3**			**V**
Logical "0" input voltage	**V_{IL}**	**Pins 27-34, 0°C ≤ T_A ≤ +70°C**			**1**	
Input leakage current	I_{ILK}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{IN}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{BPLK}	Measured at Pin 5 with Pin 36 at GND		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{SA}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{DS}		-100			ns
Data Hold Time	t_{DH}		200			
Inter-Digit Select Time	t_{IDS}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{CSA}	Other chip select either held active, or both driven together		200		ns
Data Setup Time	t_{DS}		100			
Data Hold Time	t_{DH}		10	0		
Inter-Chip Select Time	t_{ICS}		2			μs

Note 1: This limit refers to that of the package and will not be realized during normal operation.

Note 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

Note 3: All pins except pin 29 are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883B Method 3015.1 Test Circuit). Due to the special test functions associated with pin 29, this pin is designed to withstand up to 1500V (same test circuit).

Four Digit Display Decoder/Drivers

Ordering Information (Cont.)

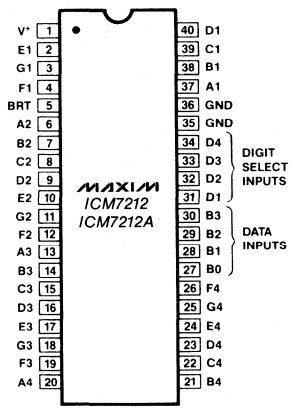
PART	TEMP. RANGE	PACKAGE
ICM7211IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7211AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212IQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212MIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
ICM7212AMIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

PART	TEMP. RANGE	PACKAGE
ICM7211IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7211AMIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212MIPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7212AMIPL	-20°C to +85°C	40 Lead Plastic DIP

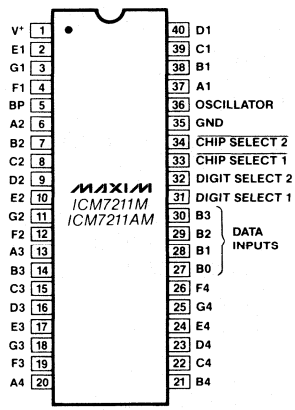
Each device type listed is available in dice form;
Order basic part number followed by C/D;
(i.e. ICM7211C/D).

Pin Configurations (Cont.)

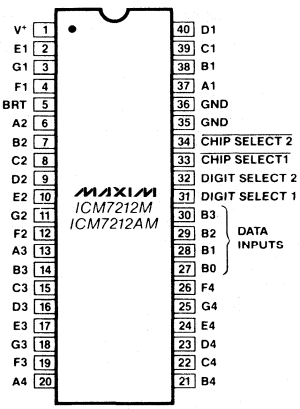
Top View **40 Lead DIP**



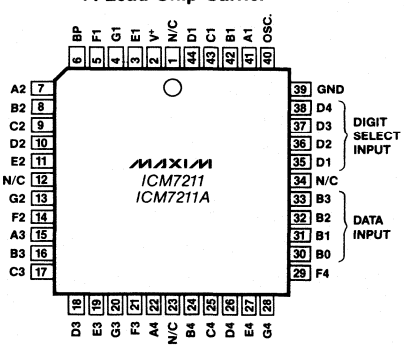
40 Pin DIP



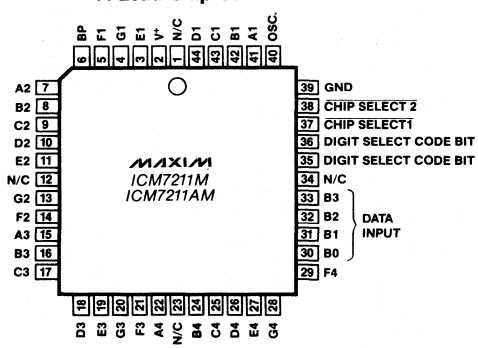
40 Lead DIP



44 Lead Chip Carrier



44 Lead Chip Carrier

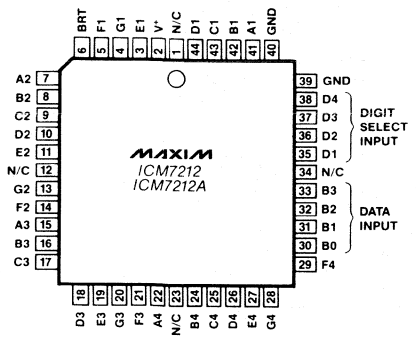


Four Digit Display Decoder/Drivers

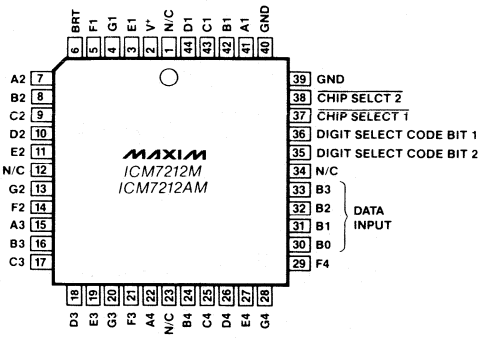
Pin Configurations (Cont.)

Top View

44 Lead Chip Carrier

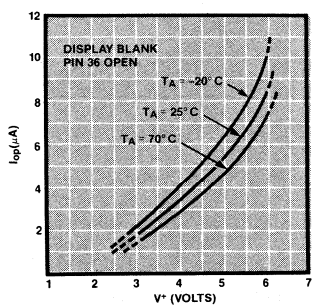


44 Lead Chip Carrier

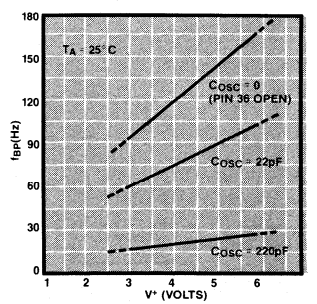


Typical Operating Characteristics

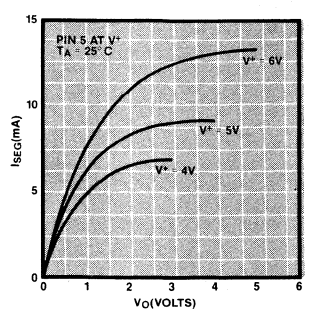
ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



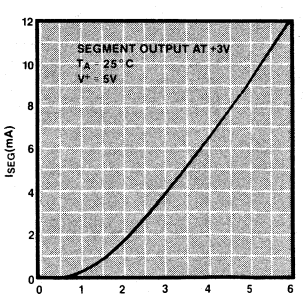
ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



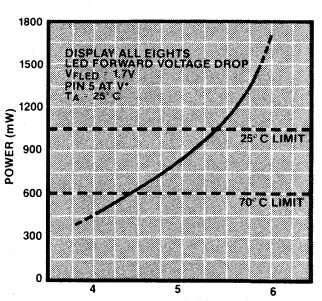
ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



Four Digit Display Decoder/Drivers

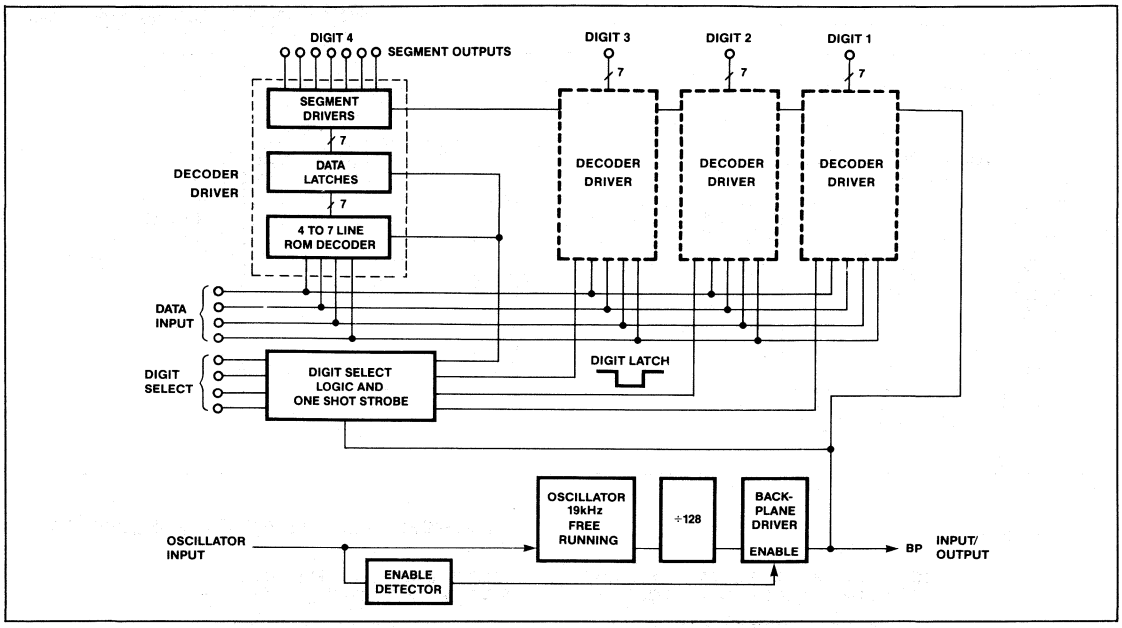


Figure 1. Block diagram of ICM7211 and ICM7211A.

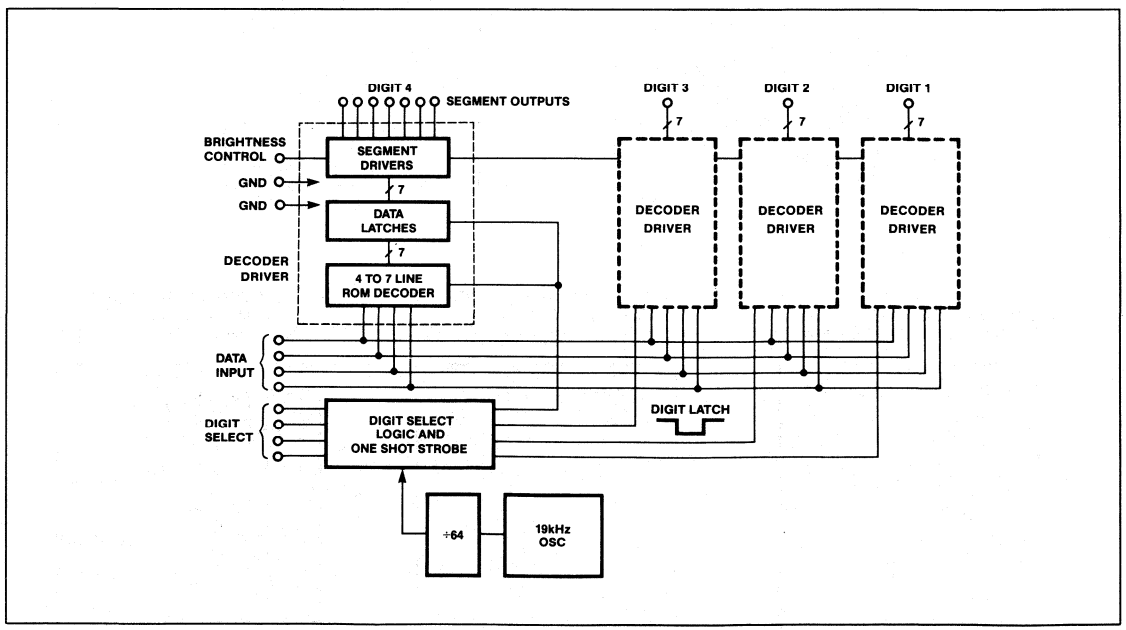


Figure 2. Block diagram of ICM7212 and ICM7212A.

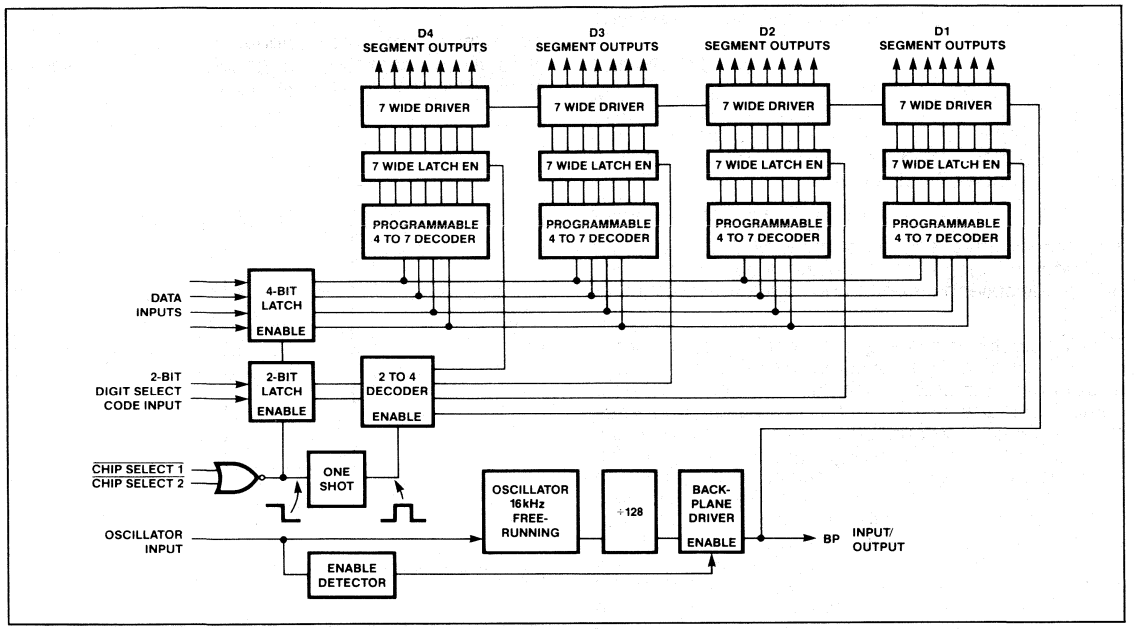


Figure 3. Block diagram of ICM7211M and ICM7211AM.

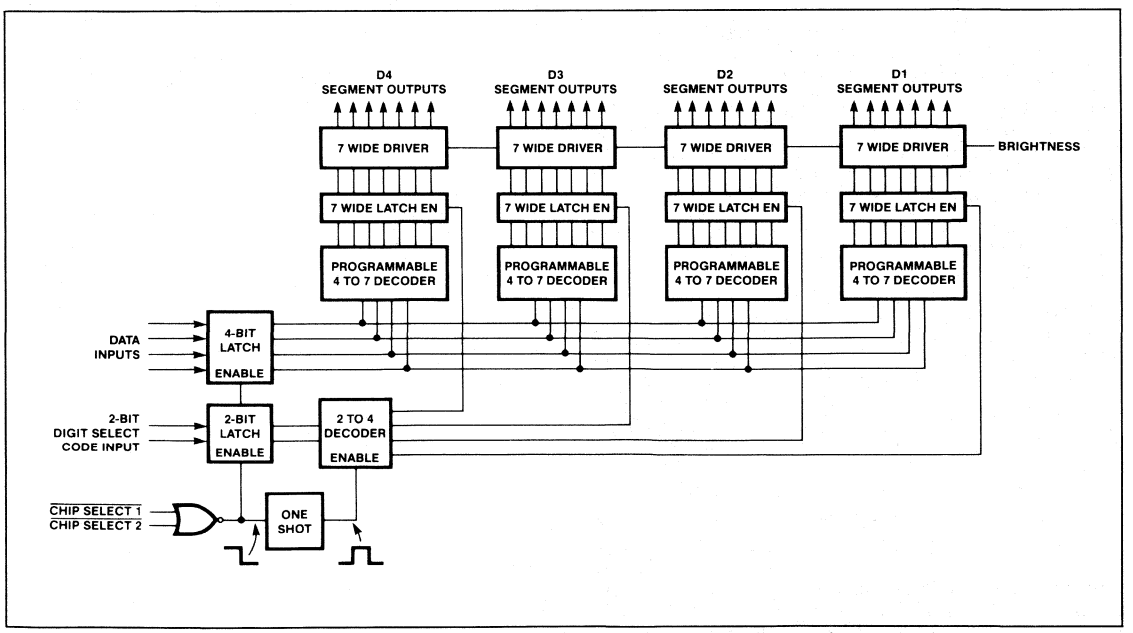


Figure 4. Block diagram of ICM7212M and ICM7212AM.

Four Digit Display Decoder/Drivers

Detailed Description

Display Interface

The ICM7211 and ICM7212 differ only in the type of display interface. The ICM7211 is designed to drive non-multiplexed liquid crystal displays (LCDs), while the ICM7212 is designed to drive non-multiplexed, common anode LED displays.

ICM7211 LCD Display Driver

The display driver section of the ICM7211 includes an oscillator, a 7 stage binary divider, a backplane driver, backplane slaving detector and logic, and 28 segment drivers.

The RC oscillator has a nominal oscillation frequency of 19kHz with no external components. Ordinarily this frequency is suitable and no external oscillator components are needed, but if desired, the frequency may be lowered by connecting a capacitor between pin 36 (Oscillator) and either ground or V^+. A graph showing the relationship between capacitor value and oscillator frequency is shown in the Typical Characteristics section. The oscillator may also be overdriven by an external clock source with a frequency of 128 times the desired backplane frequency. The external clock source should swing from approximately 1.5V to 5V when V^+ is 5V. The external clock signal must not go below 1V for more than one microsecond, or the backplane disable circuitry may be activated (see below). Figure 7 shows an external clock drive circuit that meets the above requirements.

The 19kHz nominal output of the onboard oscillator is divided by a 7 stage binary divider (÷128) to generate the backplane frequency of 150Hz.

The backplane drive is simply an inverter whose input is the output of the last divider. The backplane output swings from ground to V^+ with a 50% duty cycle. The backplane has a low (200 ohm typical) output resistance so that it can drive the capacitance of large displays.

The backplane output driver can be disabled by tying pin 36 (Oscillator) to ground. The Backplane Input/Output (pin 5) then becomes an input which can be driven by the backplane output of another ICM7211 (see Figures 14, 18 and 19). Each backplane is a load of about 200 pF when driven, and no more than 4 ICM7211's (16 digits total) should be slaved together using one "master" ICM7211 as the backplane source, since power dissipation and the DC offset increase when the ICM7211 backplane output drives very large capacitive loads. For more than 16 digits on a common backplane, a separate, external driver with a low impedance should be used to drive all ICM7211s.

The segment drivers are CMOS inverters that swing between ground and V^+ with an output resistance of about 2 kΩ. The input to the inverter is switched between two signals, so that the segment driver output is the same as the backplane when LCD segment is to be turned OFF, and is $\overline{\text{BACKPLANE}}$ when the LCD segment is to be turned ON. The segment and backplane drivers are designed to have equal rise and fall times, so that the average DC component across the LCD is less than 25 millivolts.

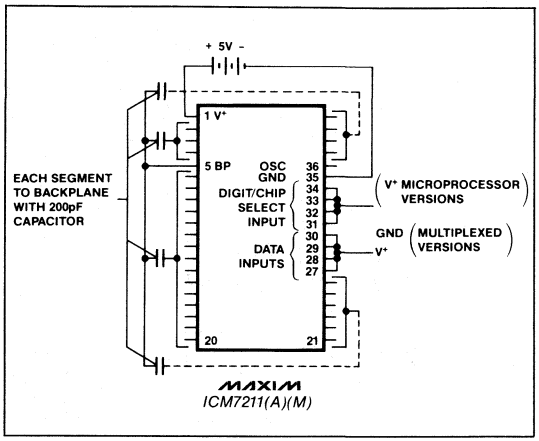


Figure 5. ICM7211 Test Circuit (all versions).

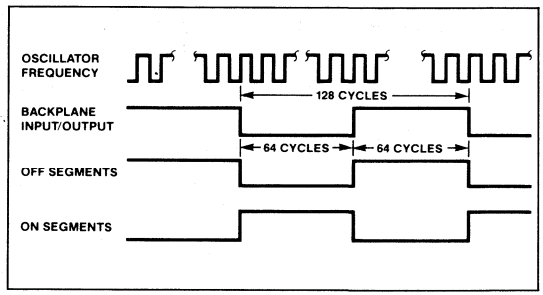


Figure 6. Display Waveforms.

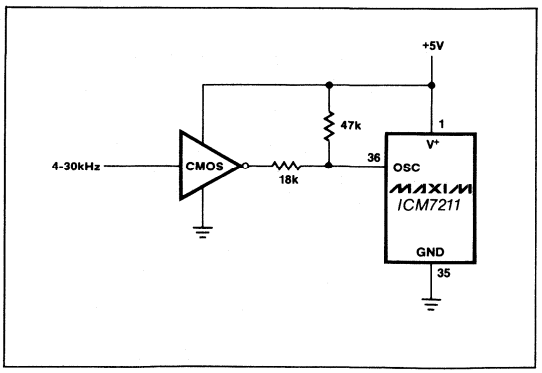


Figure 7. External Clock Drive.

ICM7212 LED Drivers

The ICM7212 has 28 open drain constant current n-channel outputs, which eliminate the need for external segment resistors. The LED current vs. output voltage of a typical segment driver is shown in the Typical Characteristics section. The Brightness input (pin 5) supplies the segment driver gate voltage, and it can be used to either control the brightness of the LED display or to completely blank the display. Two methods of controlling display brightness are shown in Figure 8. The first method simply controls the voltage on the brightness pin by means of a potentiometer. The Brightness input draws negligible current and the potentiometer is normally in the range of 100 kilohms to 1 megohm. By replacing the potentiometer with a resistor and a photoresistor, the display brightness can be automatically adjusted in response to changes in the ambient lighting. A second method of display brightness control is to duty-cycle modulate the Brightness input between "full on" and "blanked" states. As with the simple potentiometer method, the display brightness can be automatically adjusted for ambient lighting conditions by replacing one of the timing resistors with a photoresistor.

The ICM7212 has two ground pins to support the high total display current that flows into the segment outputs and then is returned to ground through the ICM7212 ground pins.

Since the ICM7212 will drive the LED display at high total display current, care must be taken not to exceed the absolute maximum power dissipation limit of the ICM7212 at high ambient temperatures. For example, at 70°C, the absoulute maximum power dissipation specification is 500 mW. If all 28 segments are turned on (a display of 8888), and each segment is drawing 8 mA, the total power dissipation in the ICM7212 would be

$Pd = 28 \text{ segments}.(8mA).(V_{seg})$
Where $V_{seg} = V^+ - V_{led} = 5V - 1.6V = 3.4V$
Therefore $Pd = 28.(8).(3.4) = 760$ mW; greater than the absolute maximum limit.

There are two ways to keep the power dissipation below the ICM7212 power dissipation limits: reduce the LED current, or reduce the voltage across the ICM7212 segment drivers. The LED current can be reduced by the display brightness control circuits shown in figure 8. The other alternative, reducing the voltage across the segment drivers can be accomplished by either reducing the V^+ supply to the entire system, or by reducing the V^+ supply to just the LED display by placing diodes in series with the LED display (see Figure 9). Two silicon diodes in series with the anode of the LED display will reduce the voltage across the segment drivers from 3.4V to 2.2V, resulting in a power reduction of approximately 35%, while only slightly reducing the LED current and brightness. A third diode in series with the LED display would further reduce the power dissipation, but the segment current would also be reduced since there would be only about 1.6V across the n-channel segment driver.

Digital Interface

There are two different types of digital interfaces available for the ICM7211 and ICM7212, a multiplexed BCD interface and a microprocessor interface.

Multiplexed BCD Data Interface

On the multiplexed BCD data entry versions of ICM7211 and ICM7212 there are 8 lines used for entering data: 4 BCD data lines and 4 digit strobes. The multiplexed BCD input timing and truth table is shown in Figure 10. When one of the four digit strobes is taken high, a short internal pulse is generated which latches the decoded segment data in the 7 bit latch associated with that digit. If the digit strobe is continuously held high, each transition of the backplane will cause another internal latch pulse to be generated, latching new segment data if the BCD data has changed. When the digit strobe goes low the data in the latch is held constant with no further updates until the digit strobe is again taken high. As shown in the electrical specifications table, the data setup time is is a negative 100ns, which means that the digit strobe can be taken high as much as 100ns before the BCD data is valid.

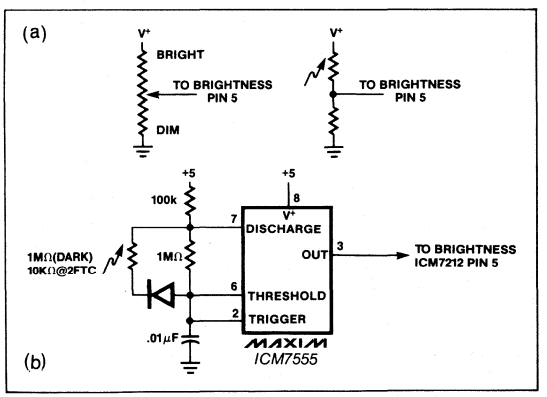


Figure 8A & 8B. Brightness Control

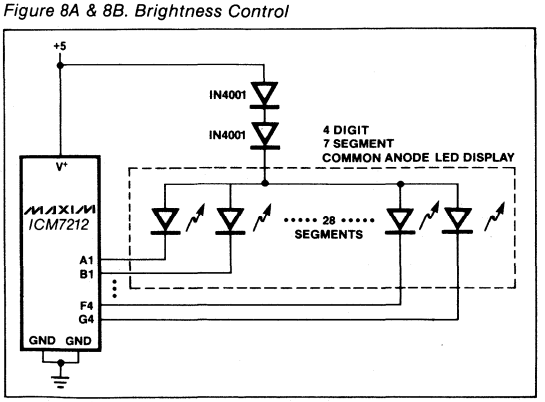


Figure 9. Reducing ICM7212 Power Dissipation.

Four Digit Display Decoder/Drivers

Character Fonts

Table 1 shows the two different output codes or fonts available. Both versions have the same display for 0-9 and differ only in the display of the last 6 input codes. The Code B versions have the suffix "A" in their part number.

Table 1: Output Codes

BINARY				HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

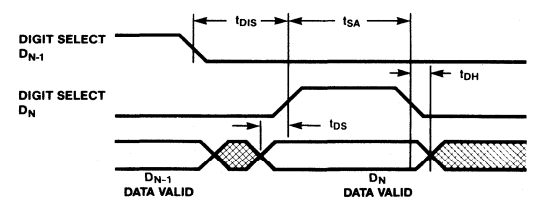
Microprocessor or Data Interface

The microprocessor data interface versions of the ICM7211 and ICM7212 are denoted by an "M" suffix in their part number. The microprocessor data interface also uses 8 lines for the data interface: 4 BCD data lines, 2 digit address lines, and 2 active low chip select lines. A typical data write cycle and the truth table are shown in Figure 11. Data is entered into the input latches whenever both CS (chip select) lines are low. When either CS line goes high an internal one shot is activated, transferring the decoded 7-segment data to the appropriate digit latch. One CS line is ordinarily driven by an address decoder and the other CS line is driven by the microprocessor WR (write) line (see Figure 15). In this type of application, the ICM7211/12 is accessed as 4 "write only" memory locations.

Application Notes

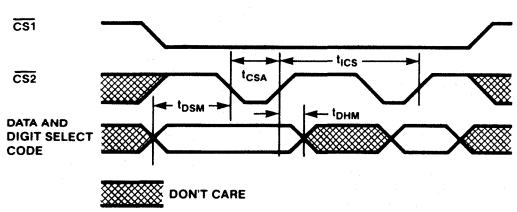
Backplane Frequency

The ICM7211 onboard oscillator generates a backplane frequency of approximately 150Hz with no external components. This is suitable for most displays, but



TRUTH TABLE				
D1	D2	D3	D4	Function
0	0	0	0	No change
0	0	0	1	Store Data in D4 Latch
0	0	1	0	Store Data in D3 Latch
0	1	0	0	Store Data in D2 Latch
1	0	0	0	Store Data in D1 Latch
1	1	1	1	Store Data in All Data Latches

Figure 10. Multiplexed input timing diagram and truth table.



TRUTH TABLE				
DS2	DS1	$\overline{CS2}$	$\overline{CS1}$	Function
X	X	X	1	No change
X	X	1	X	
0	0	0	↑	Store D4 Data
0	0	↑	0	
0	1	0	↑	Store D3 Data
0	0	↑	0	
1	0	0	↑	Store D2 Data
1	0	↑	0	
1	1	0	↑	Store D1 Data
1	1	↑	0	

Figure 11. Microprocessor Interface input timing diagram and truth table.

150Hz is too high a frequency when driving very large displays or low threshold displays with high segment trace resistance. When driving very large displays (>1" height), the very large capacitance of the display will significantly slow the rise and fall times of the backplane and segment drivers. These drivers are designed to have matching rise and fall times, but any residual mismatch will result in a DC offset across the LCD. This DC offset is directly proportional to the backplane frequency, so the lowest acceptable backplane frequency (usually 30Hz) should be used when driving very large LCDs. A simple way of lowering the backplane frequency is to connect an external capacitor from the OSCillator (pin 36) to either ground or V^+. The graph in the Typical Characteristics curves shows the relationship between the value of this external capacitor and the backplane frequency. The backplane frequency can also be controlled by externally driving the OSCillator pin. Figure 12 shows a method of setting the backplane frequency to precisely 32Hz.

If the indium traces on the LCD glass itself are very long and they have high sheet resistance, the resistance of the trace will form an RC delay with the capacitance of the LCD. The phase shift caused by this RC delay causes a small voltage to appear across the LCD segments that are supposed to be in the off state. This may cause "ghosting" or a slight turn-on of segments that are supposed to be off. Reducing the backplane frequency or using LCDs that have a higher threshold will eliminate this problem.

Annunciators or Flags

Many LCD displays have annunciators or flags in addition to the 7 segment digits. Figure 13 shows several different methods of driving LCD segments used as annuciators or flags. Output A of Figure 13 is driven by a CMOS exclusive OR (XOR) gate. The XOR's output is either the same as the backplane or the complement of the backplane, depending on the logic level on the input. With a "1" at the logic input the XOR output is the complement of the backplane and the LCD segment is turned on. Output B is connected to the backplane through a 1 MΩ resistor. When the analog switch is open, output B will be the backplane signal and the segment will be off. When the analog switch is closed, output B will be the complement of the backplane signal and the segment will be on. Output C is simply the complement of the backplane signal, and any segment (such as a decimal point) connected to output C will always be turned on. Output D is another way of turning on a decimal point, but since the voltage at D is simply the average DC voltage of the backplane signal, the total applied voltage across a segment connected to D is only 5 Vpk-pk (assuming 5V V^+) rather than the 10Vpk-pk drive received by a segment connected to output C. The resistor-capacitor drive method of output D should be used only with low threshold LCDs. Unused LCD segments should be tied to the backplane, NOT allowed to float. A floating segment, while usually remaining off, may be driven by leakage currents or capacitive coupling with other segments and become a "ghost" or slightly turned on.

If one or more of the ICM7211 digits are not used, they can be used to drive annunciator segments without using any external logic. If only two annunciator segments need to be driven, connect the annunciators to segments B and D of the unused digit. That digit is then loaded with the data $\overline{A2}$, $\overline{A1}$ 11, where A1 and A2 are the data for the two annunciators.

Three annunciators can be driven from one unused digit, but the input data to select all 8 possible combinations of annunciator states must be obtained from a look-up table. Two possible arrangements are shown in Table 2.

Driving an 8 Digit LCD with Common Backplane

In order to drive 8 LCD digits that have a common backplane, the backplanes of two ICM7211s must be synchronized. In figure 14 the left hand ICM7211's Backplane pin is turned into an input by grounding its oscillator pin. The right hand ICM7211 then drives both the LCD backplane and the Backplane pin of the left hand ICM7211.

Memory Mapped 8048 Microprocessor Interface

In figure 15 the digit select lines DS1 and DS2 are driven by the address latched from the 8048's multiplexed data and address bus. The data is then written into the selected digit by the $\overline{WR}$ line. The 74LS138 is used to decode eight blocks, each four bytes long, starting at address 32 (decimal). The ICM7211s are addressed by MOVX instructions to these external ram locations. The extra decoded outputs of the 74LS138 can be used as chip selects for other I/O devices.

Microprocessor Interface via I/O Port

Figure 16 shows one 8 bit I/O port driving two ICM7211s or ICM7212s. The data and digit selects are controlled by the lower 6 bits, while the upper two bits control which display driver receives the data.

Remote Display via UART

The serial input stream is assembled into an 8 bit parallel output by the UART, then the UART brings the DR (data ready) line high (See Figure 17). The schmitt trigger and RC delay drive both the $\overline{CS}$ inputs of the ICM7211s and the $\overline{DRR}$ (data ready reset) pin of the UART. When the schmitt trigger drives the $\overline{DRR}$ low, the DR pin goes low, and after a short delay, the output of the schmitt trigger output goes back high. This low-going pulse on the schmitt trigger output latches the data into the ICM7211s.

Display Interface for ICL7135 A/D

Figure 18 shows an ICM7212 interfaced to the 4½ digit A/D, ICL7135. The polarity and ½ digit segments are driven by D flip-flops that latch polarity and ½ digit data at the end of each measurement. The ICL7135

Four Digit Display Decoder/Drivers

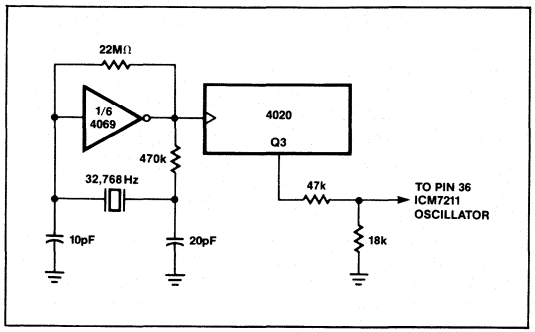


Figure 12. Crystal Controlled Backplane Frequency.

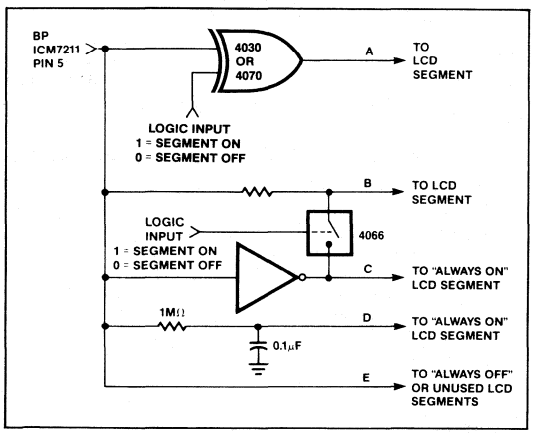


Figure 13. Driving Annunciators, Flags and Decimal Points.

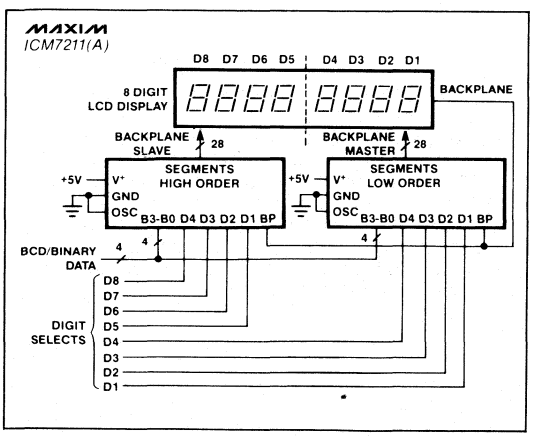


Figure 14. Two ICM7211's Driving 8-Digit LCD Display.

Overrange output drives the ICM7212 Brightness input, blanking the four least significant digits when the input voltage is greater than full-scale.

Similar to the LED display system, Figure 19 uses Maxim's ICM7211 LCD display driver to drive 4 digits of LCD display. The backplane signal of the ICM7211 and the CMOS exclusive OR gates are used to drive the 1/2 digit and the polarity sign. The 4 AND gates combine the ICM7135's digit outputs with its Strobe output to generate the digit select signals that latch data into the ICL7211. Since the Strobe occurs in the middle of each digit's data there is more than enough data setup and hold time to ensure that valid data is latched. The OR gates will force the BCD data to all ones when overrange goes high. The ICM7211A will blank the display when all ones (hex F) is loaded.

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	1	1	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	0	1	1
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2A: Using Segments to Drive Annunciators, ICM7211

SEGMENT			INPUT DATA FOR ICM7211			
F	E	A	B3	B2	B1	B0
0	0	0	1	1	1	1
0	0	1	0	1	0	1
0	1	0	0	0	0	1
0	1	1	0	0	1	1
1	0	0	1	1	0	1
1	0	1	0	1	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	0

0 = OFF
1 = ON

Table 2B: Using Segments to Drive Annunciators, ICM7211A

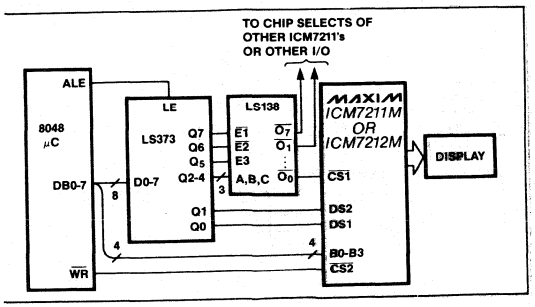


Figure 15. 8048 Memory Mapped Interface

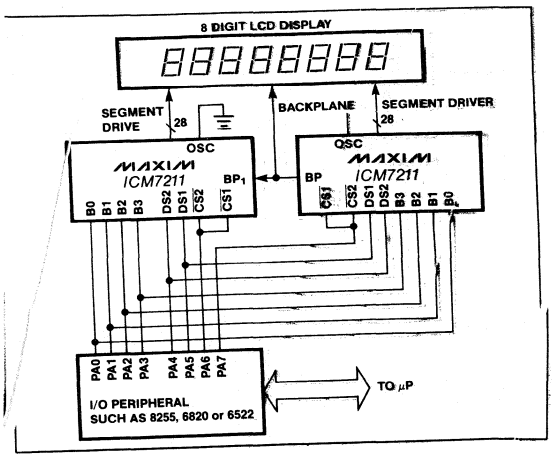
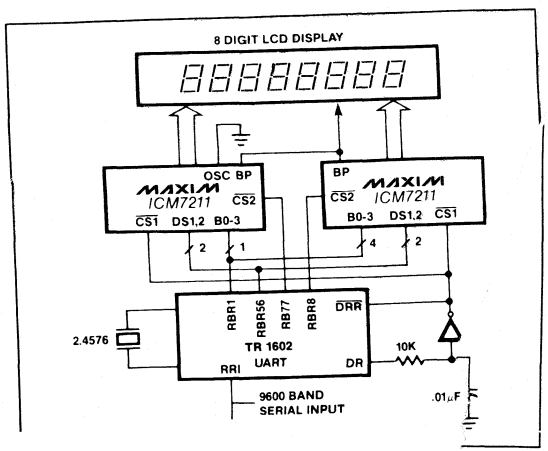


Figure 16. uP Interface via I/O Port



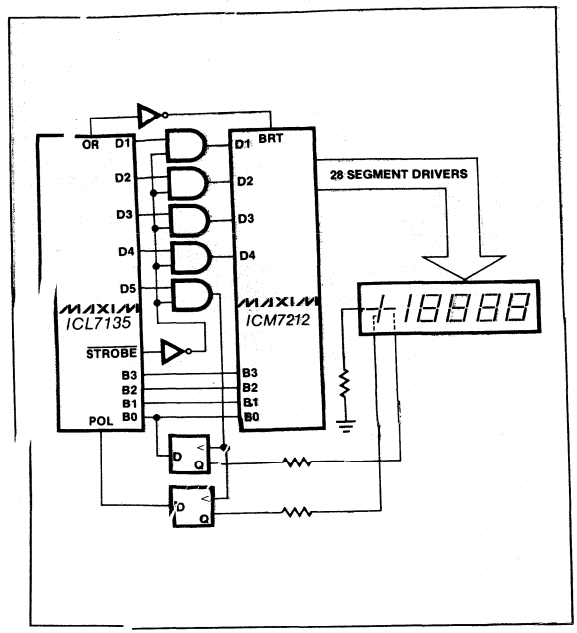


Figure 18 . LED Display Interface for ICL7135 A/D

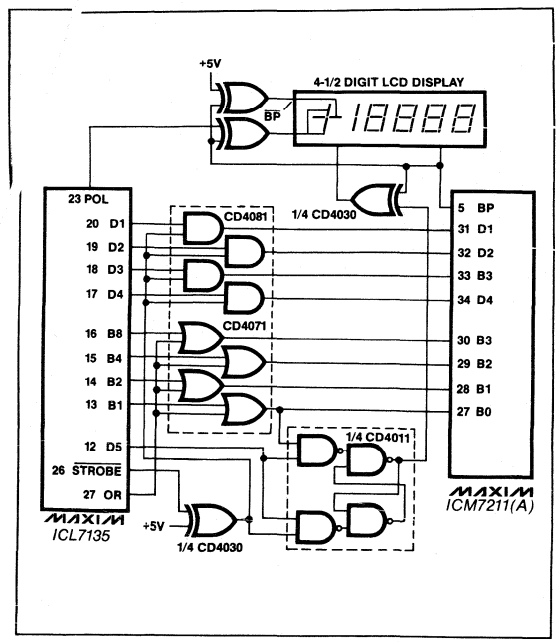


Figure 19. LCD Display for ICL7135 A/D

Four Digit Display Decoder/Drivers

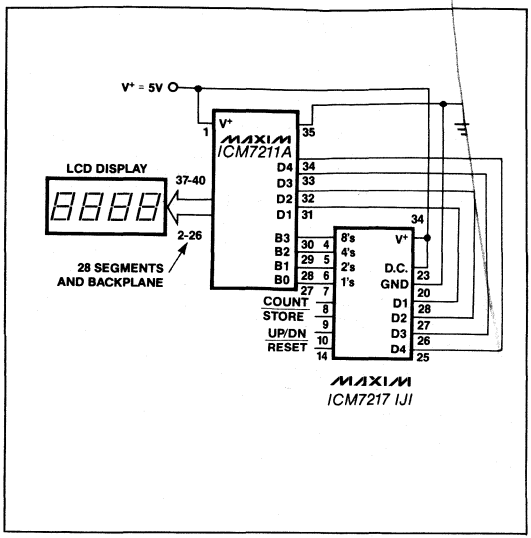


Figure 20. ICM7217 to LCD Interface.

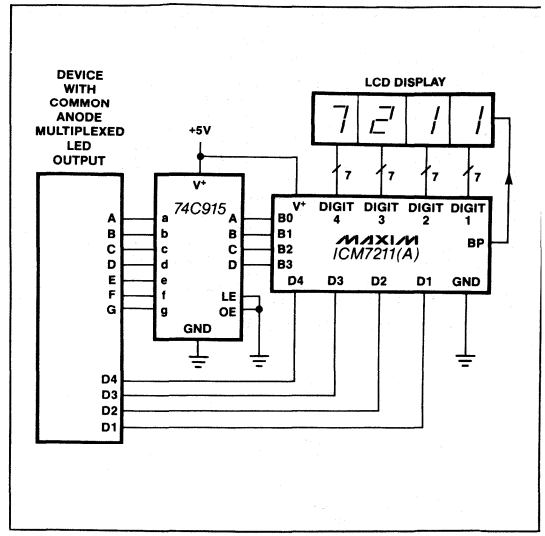
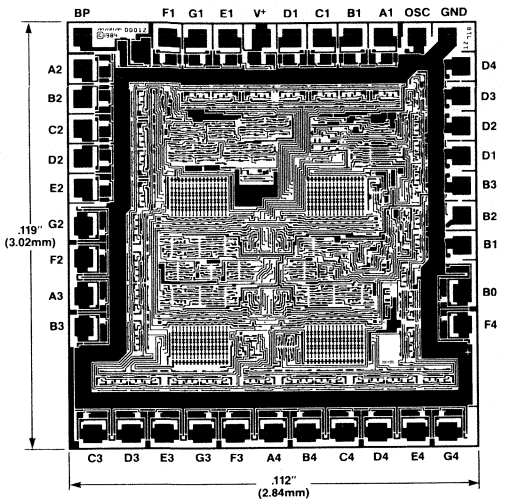


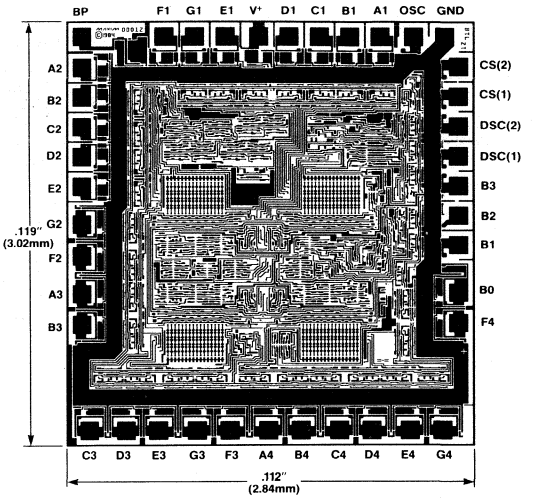
Figure 21. Multiplexed LED Driver to LCD Interface.

Chip Topography

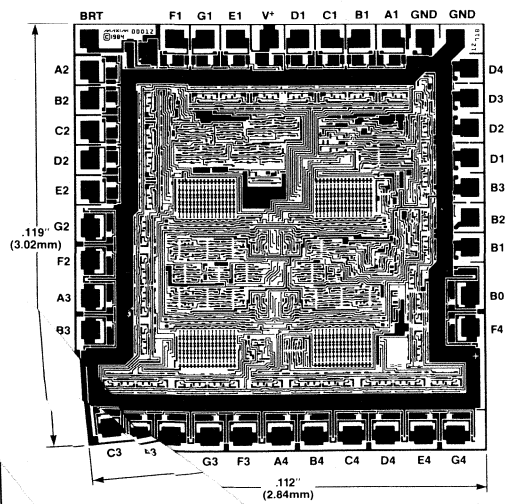
ICM7211, 7211A



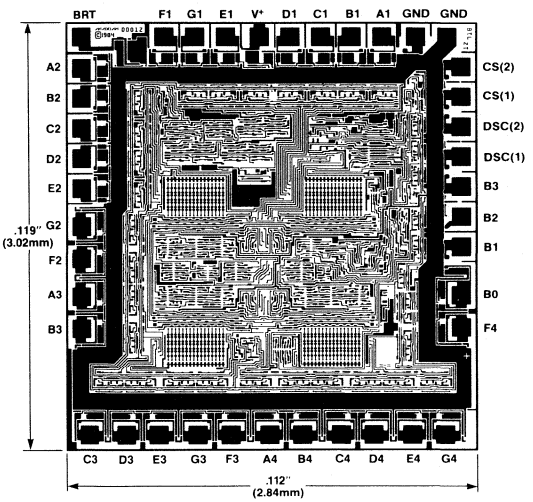
ICM7211M, 7211AM



ICM7212, 12A

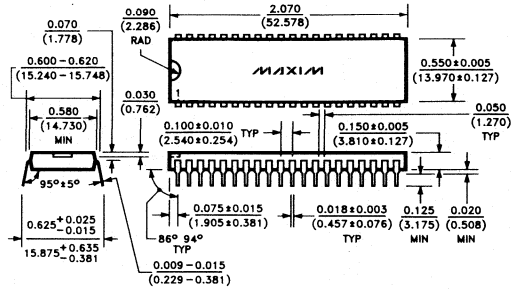


ICM7212M, 7212AM

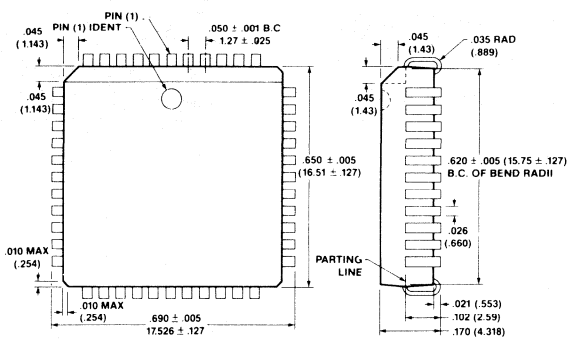


Four Digit Display Decoder/Drivers

Package Information



40 Lead Plastic (PL)
θ_{JA} = 100°C/W
θ_{JC} = 45°C/W



44 Lead Plastic Chip Carrier (Quad Pack) (Q)

MAXIM
8 Digit LED Display Driver

General Description

The Maxim ICM7218 display driver interfaces microprocessors to an 8 digit, 7 segment, numeric LED display. Included on chip are two types of 7 segment decoders, multiplex scan circuitry, segment and digit drivers, and an 8×8 static memory.

The ICM7218A and ICM7218B accept data in a serial format and drive common anode (ICM7218A) or common cathode (ICM7218B) displays. The ICM7218C and ICM7218D accept data in a parallel format and drive common anode (ICM7218C) or common cathode (ICM7218D) displays. All four versions can display the data in either hexadecimal or code B format. The ICM7218A and ICM7218B also feature a No Decode mode where each individual segment can be independently controlled. This is particularly useful in driving bar graphs.

Applications

Instrumentation
Test Equipment
Hand Held Instruments
Telecommunication Displays
Panel Meters

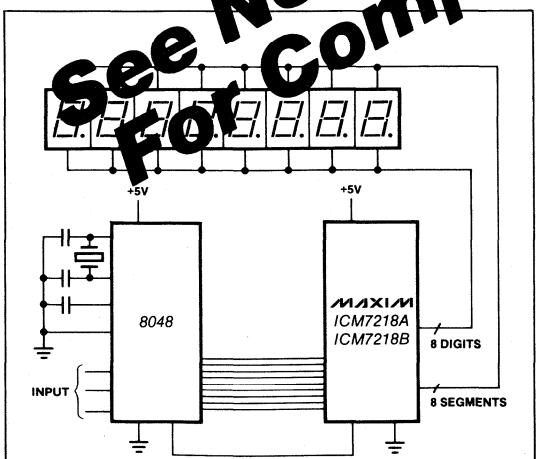
Features

- **Improved 2nd Source! See 3rd page of this data sheet for our "Maxim Advantage™"**
- **Faster Access Time: 200ns Write Pulse Width**
- **Microprocessor Compatible**
- **Hexadecimal and Code B Decoders**
- **Individual Segment Control with "No Decode" Feature**
- **Digit and Segment Drivers On-Chip**
- **Common Anode and Common Cathode LED versions available**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7218AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218CIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218DIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218DIJI	-20°C to +85°C	28 Lead CERDIP

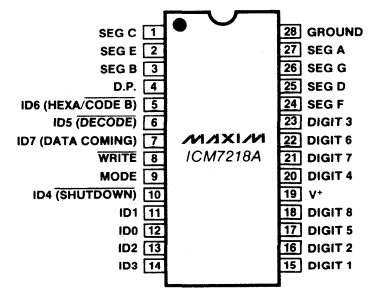
Typical Operating Circuit



8 Digit Microprocessor Display

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

MAXIM

Triplexed LCD Decoder/Drivers

General Description

The MAX7231/32/33/34 family of integrated circuits is a complete line of triplexed liquid crystal display (LCD) drivers. These devices interface microprocessors (or digital systems) to multiplexed numeric and alphanumeric displays. The MAX7231 drives 8 digits and accepts data in a parallel format. The MAX7232 drives 10 digits and accepts data in a serial format. Both devices feature two independent annunciators per digit. The MAX7233 drives 4 alphanumeric 18 segment characters. The MAX7234 drives 5 alphanumeric 18 segment characters.

Each device includes an input buffer, digit address decoding circuitry and mask-programmed ROM allowing six bits of input data to be decoded into 64 independent combinations of the output segments of each digit. This offloads the microprocessor system, reducing the ROM space and CPU time needed to service a display.

Applications

These low-power LCD drivers are ideal for microprocessor-based portable applications where power consumption is a primary concern. Many applications also take advantage of the annunciator drive capability, which allows unlimited variations of display layout.

Portable instrumentation
Industrial equipment
Telecommunications
Medical equipment
Panel Meters
Machine control

Features

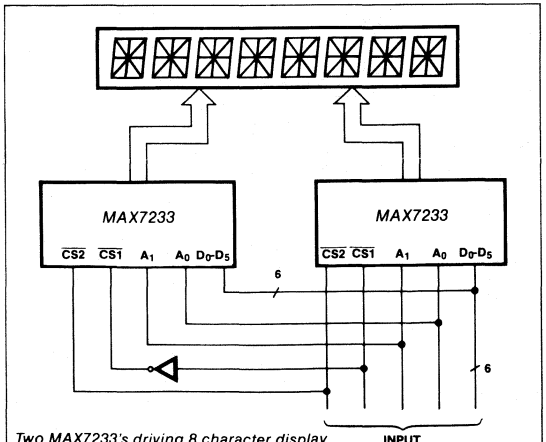
- **MAX7231 drives 8 digits/7 segments; parallel input format; 2 annunciators per digit**
- **MAX7232 drives 10 digits/7 segments; serial input format; 2 annunciators per digit**
- **MAX7233 drives 4 alphanumeric characters/ 18 segments; parallel input format**
- **MAX7234 drives 5 alphanumeric characters/ 18 segments; serial input format**
- **On-chip oscillator**
- **Direct interface to microprocessors**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7231AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7231CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7232CFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7233BFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234AFIPL	-20°C to +85°C	40 Lead Plastic DIP
MAX7234BFIPL	-20°C to +85°C	40 Lead Plastic DIP

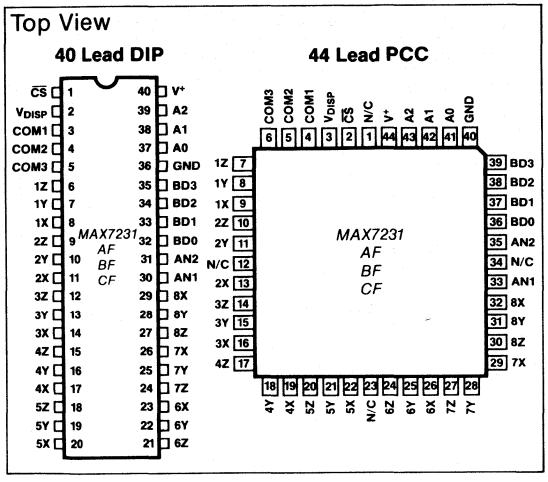
Ordering information continued on next page

Typical Operating Circuit



Two MAX7233's driving 8 character display (Detailed Circuit Diagram — Figure 21)

Pin Configuration



Triplexed LCD Decoder/Drivers

OPTION TABLE

DEVICE	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231AF ICM7231BF ICM7231CF	Hexdecimal Code B Code B	Both Annunicators on COM3 1 Annunciator COM1 1 Annunciator COM3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7232AF ICM7232BF ICM7232CF	Hexadecimal Code B Code B	Both Annunciators on COM3 1 Annunciator COM1 1 Annunciator COM3	Serial Entry 4 bit Data 2 Bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7233AF	64 Character (ASCII) 18 Segment (Half width numbers)	No independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7233BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Parallel Entry 6 bit (ASCII) Data 2 bit Address	Four Characters
ICM7234AF	64 Character (ASCII) 18 Segment (Half width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters
ICM7234BF	64 Character (ASCII) 18 Segment (Full width numbers)	No Independent Annunciators	Serial Entry 6 bit (ASCII) Data 3 bit Address	Five Characters

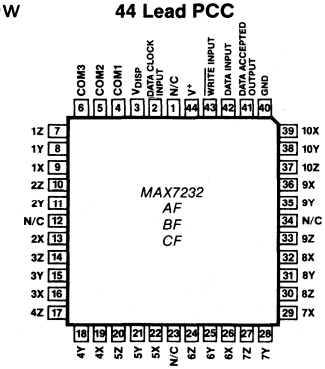
Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX7231AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7231CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7232CFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7233BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234AFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier
MAX7234BFIQ	-20°C to +85°C	44 Lead Plastic Chip Carrier

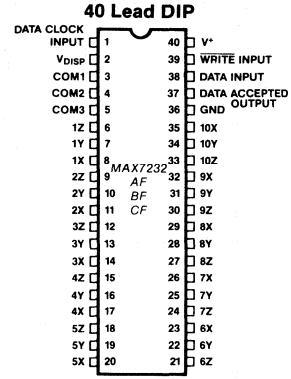
Pin Configuration

Top View

44 Lead PCC



40 Lead DIP



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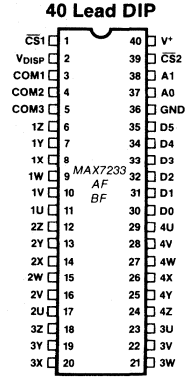

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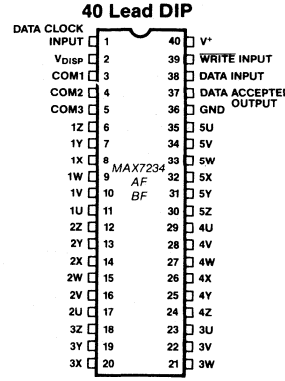


Continued on last page of data sheet.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 W @ 85°C
Supply Voltage (V^+) 6.5V
Input Voltage (Note 2) ..... $-0.3V \le V_{IN} \le 6.5V$
Display Voltage (Note 2) ..... -0.3V to V^+ + 0.3V
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Soldering Temperature (10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not limited. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +5V ±10%, T_A = -20°C to +85°C unless noted)

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION		MIN	TYP	MAX	UNITS
Power Supply Voltage	V^+			4.5		5.5	V
Data Retention Supply Voltage	V^+	Guaranteed Retention at 2V		2	1.6		V
Logic Supply Current	I^+	Current from V^+ to Ground excluding Display, V_{DISP} = 2V			30	100	µA
Shutdown Total Current	I_S	V_{DISP} Pin 2 Open			1	10	µA
Display Voltage Range	V_{DISP}	Ground ≤ V_{DISP} ≤ V^+		0		V^+	V
Display Voltage Setup Current	I_{DISP}	V_{DISP} = 2V, Current from V^+ to V_{DISP} On-Chip (Note 3)			15	25	µA
Display Voltage Setup Resistor Value	R_{DISP}	One of Three Identical Resistors in String (Note 3)		40	75		kΩ
DC Component of Display Signals		Sample Test only, V_{DISP} = 0V			1/4	1	% (V^+-V_{DISP})
Display Frame Rate	f_{DISP}	See Figure 2		60	90	120	Hz
Input Low Level (Note 3)	V_{IL}	MAX7231, MAX7233	MAX7232, MAX7234			0.8	V
Input High Level (Note 3)	V_{IH}	Pins 1, 30-35, 37-39	Pins 1, 38, 39	2.0			V
Input Leakage	I_{ILK}	MAX7231, MAX7233	MAX7232, MAX7234		0.1	1	µA
Input Capacitance	C_{IN}	Pins 1, 30-35, 37-39	Pins 1, 38, 39		5		pF
Output Low Level	V_{OL}	Pin 37, MAX7232, MAX7234, I_{OL} = 1mA,				0.4	V
Output High Level	V_{OH}	V^+ = 4.5V, I_{OH} = -500µA		4.1			V

AC CHARACTERISTICS V^+ = 5V, T_A = 25°C, 0-3V INPUT SWINGS **PARALLEL INPUT (MAX7231, MAX7233) See Figure 5**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Chip Select Pulse Width	t_{cs}		500	350		ns
Address/Data Setup Time	t_{ds}		200			ns
Address/Data Hold Time	t_{dh}		0	-20		ns
Inter-Chip Select Time	t_{ics}		3			µs

AC CHARACTERISTICS V^+ = 5V, T_A = 25°C, 0-3V INPUT SWINGS **SERIAL INPUT (MAX7232, MAX7234) See Figures 6, 7, 8**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN	TYP	MAX	UNITS
Data Clock Low Time	t_{cl}		350			ns
Data Clock Period	t_{cl}		1			µs
Data Setup Time	t_{ds}		200			ns
Data Hold Time	t_{dh}		0	-20		ns
Write Pulse Width	t_{wp}		500	350		ns
Write Pulse to Clock at Initialization	t_{wll}		4			µs
Data Accepted Low Output Delay	t_{odl}				1	µs
Data Accepted High Output Delay	t_{odh}			1.5	3	µs
Write Delay After Last Clock	t_{cws}		350			ns

Note 1: This limit refers to that of the package and will not be obtained during normal operation.
Note 2: Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3 volts below ground, but may be connected to voltages above V^+ but not more than 6.5 volts above GND.
Note 3: V^+ = 5V, T_A = +25°C.

Triplexed LCD Decoder/Drivers

TERMINAL DEFINITIONS

MAX7231 PARALLEL INPUT NUMERIC DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF — See Table 1
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant } 4 Bit Binary Data Inputs	Input Data (See Table 2) — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant } 3 Bit Digit Address Inputs	Input Address (See Table 4)
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit

Note 3: CS has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, and driving it with fast rise and fall times.

MAX7233 PARALLEL INPUT ALPHA DISPLAY

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
D0 D1 D2 D3 D4 D5	30 31 32 33 34 35	Least Significant Most Significant } 6 Bit (ASCII) Data Inputs	Input Data (See Table 3) — HIGH = Logical One (1), LOW = Logical Zero (0)
A0 A1	37 3	Least Significant Most Significant } Address Inputs	Input Add. (See Table 5)
$\overline{CS1}$ $\overline{CS2}$	39 1	Chip Select Inputs (Note 3)	Both Inputs LOW, load data into input latches. Rising edge of either input causes data to be latched, decoded and sent out to addressed character.

MAX7232 and MAX7234 SERIAL DATA AND ADDRESS INPUT

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic is reset. When DATA ACCEPTED Output is HIGH, positive going edge of WRITE triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. MAX7232: Eleventh edge resets shift register and control logic. MAX7234: Tenth edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; MAX7232: 8, 9 or 10 bits. MAX7234: 9 bits.

ALL DEVICES

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V^+) chip is shutdown; oscillator stops, all display pins to V^+.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6-29 6-35	(On MAX7231/33) (On MAX7232/34)	Drive display segments, or columns.
V^+	40	Positive Supply	
GND	36	Ground	

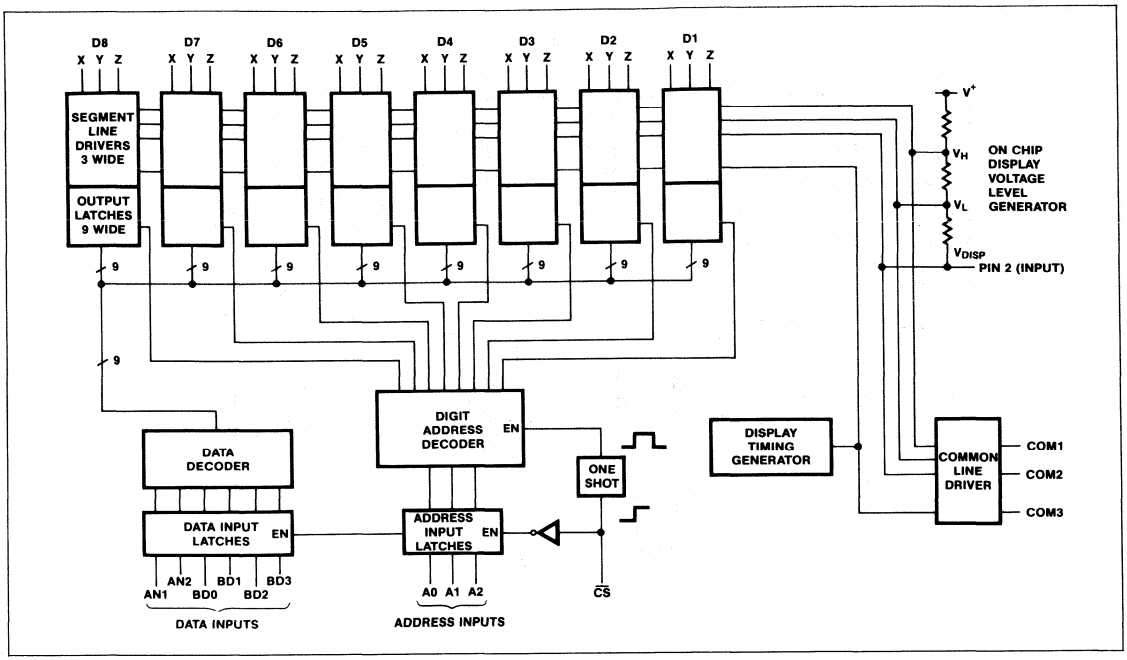


Figure 1. Block Diagram of MAX7231.

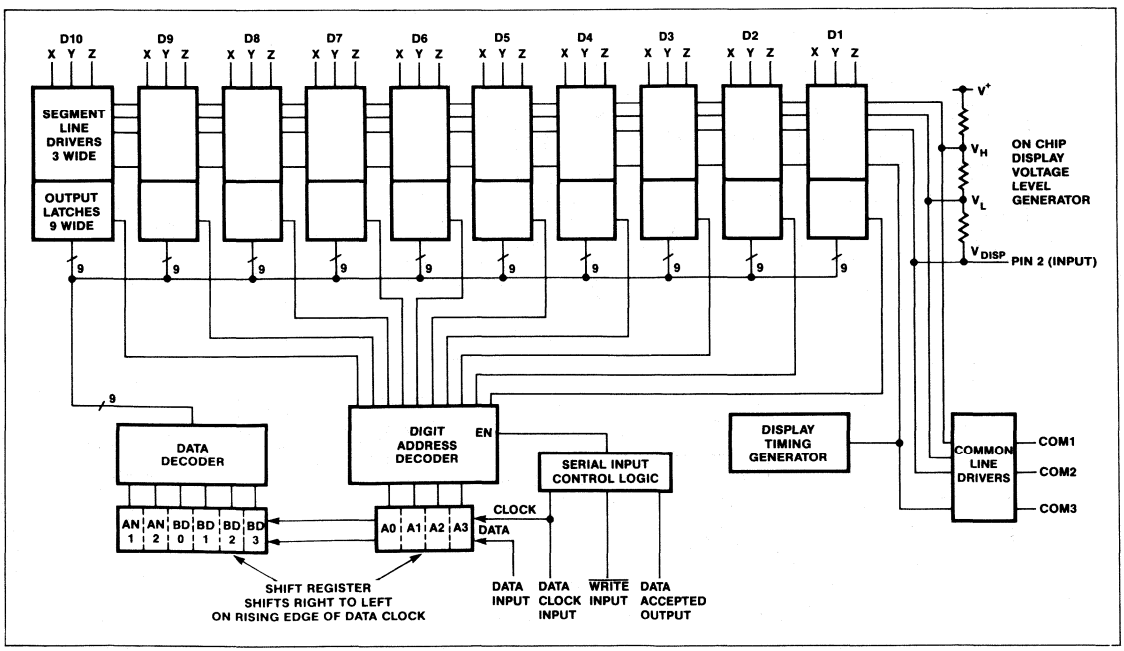


Figure 2. Block Diagram of MAX7232

Triplexed LCD Decoder/Drivers

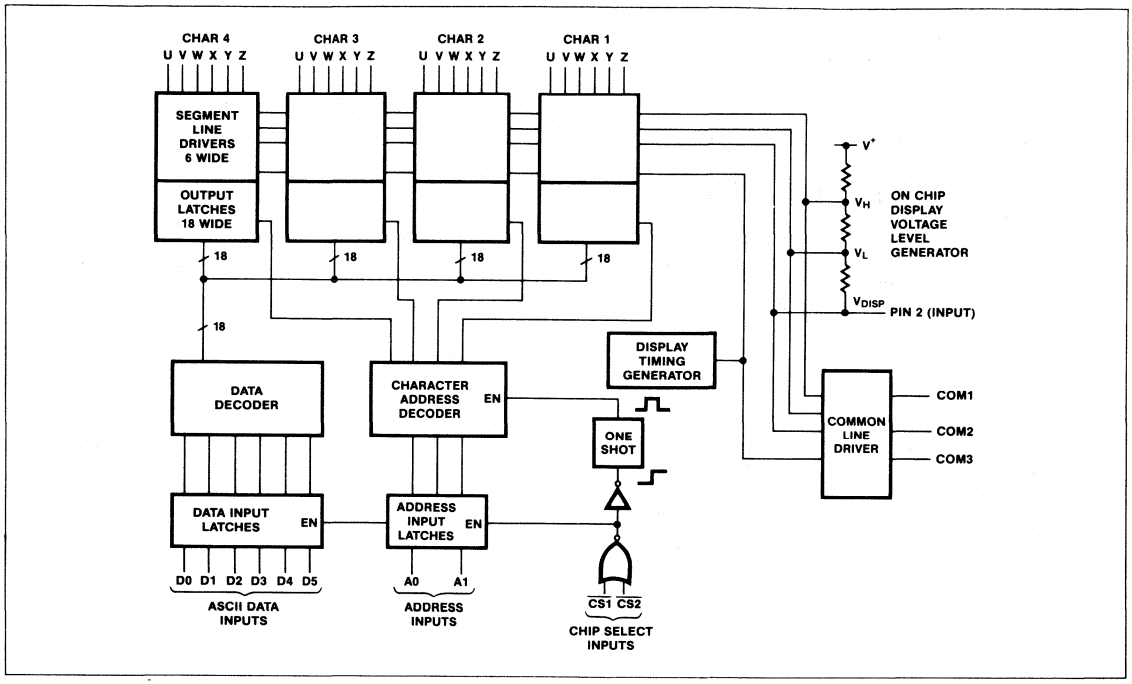


Figure 3. Block Diagram of MAX7233

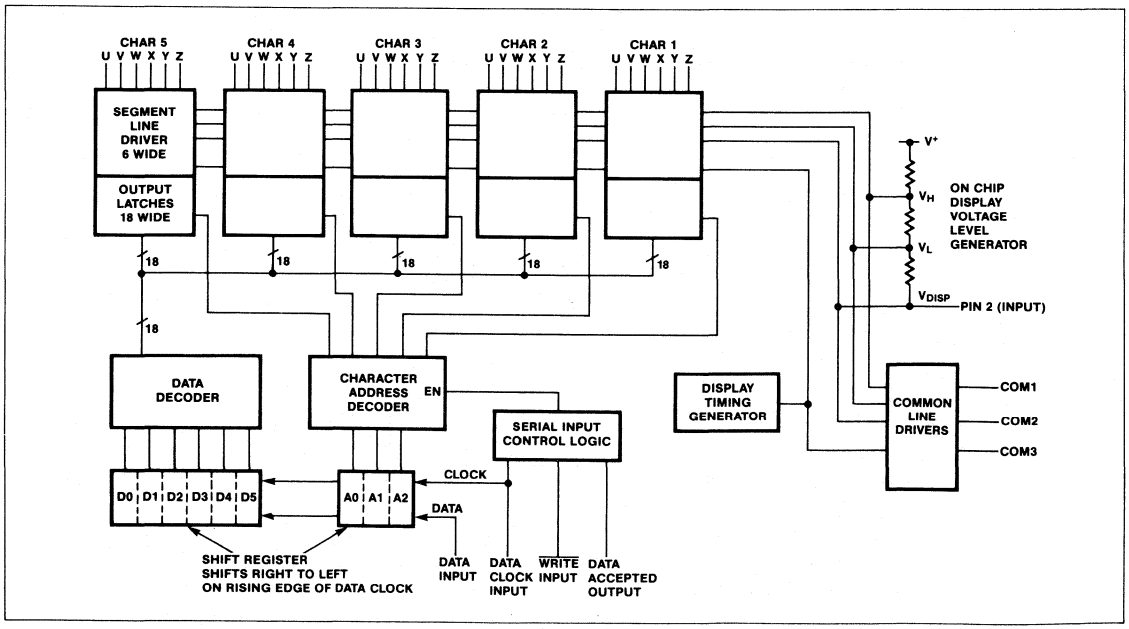


Figure 4. Block Diagram of MAX7234

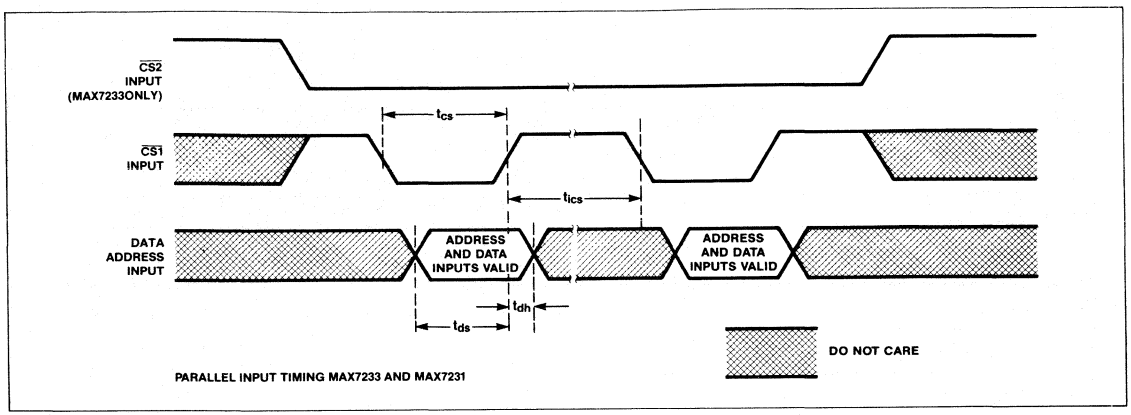


Figure 5. Parallel Input Timing

Detailed Description

Parallel Input Interface

The MAX7231 and MAX7233 have a parallel interface allowing direct parallel connection to microprocessors. The address and data bits are latched on the positive going edge of the Chip Select. The positive going edge of Chip Select also triggers an internal monostable that enables the address decoder and latches the decoded data into the digit/character output latches.

Figure 5 shows the timing requirements for the parallel input devices (7231 and 7233). To ensure that the new data does not appear at the decoder inputs before the previous decoded data is written to the outputs, there is a minimum time required between CHIP SELECT pulses.

Serial Input Interface

A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is high will reset the serial input control logic, but will not latch any data. A $\overline{\text{WRITE}}$ pulse while Data Accepted Output is low will cause the MAX7232 and MAX7234 to decode the data, latch the data into the output latches and then reset the serial input control logic.

This assures that each data bit will be entered into the correct position in the shift register, depending on the subsequent data clock inputs. The MAX7232's Data Accepted Output goes low after 8 Data Clock pulses, whereas the MAX7234's Data Accepted Output goes low after 9 Data Clock Inpulses. Further Data Clock pulses occuring before a $\overline{\text{WRITE}}$ pulse will cause the Data Accepted Output to go high after 11 Data Clock pulses in the MAX7232 and the 10 Data Clock pulses in the MAX7234. In both cases, the serial input control logic is also reset when Data Accepted goes high.

The serial input timing diagram shown in Figure 6 illustrates the recommended procedure for entering data.

Note that the eleventh clock resets the shift register and control logic for the MAX7232, but the Data Accepted Output goes low after the eighth clock. As Figure 7 illustrates, this allows the user to reduce the data to eight bits. The MAX7232 then writes to the 7 segment display, but leaves the annunciators off. Nine Bits are clocked in if only AN2 is turned on.

The control logic of the MAX7234 is similar to the MAX7232, but nine bits are always required. As illustrated in Figure 8, the data bits are only latched if the $\overline{\text{WRITE}}$ input occurs after the ninth data bit has been entered and Data Accepted Output is low.

Triplexed LCD Decoder/Drivers

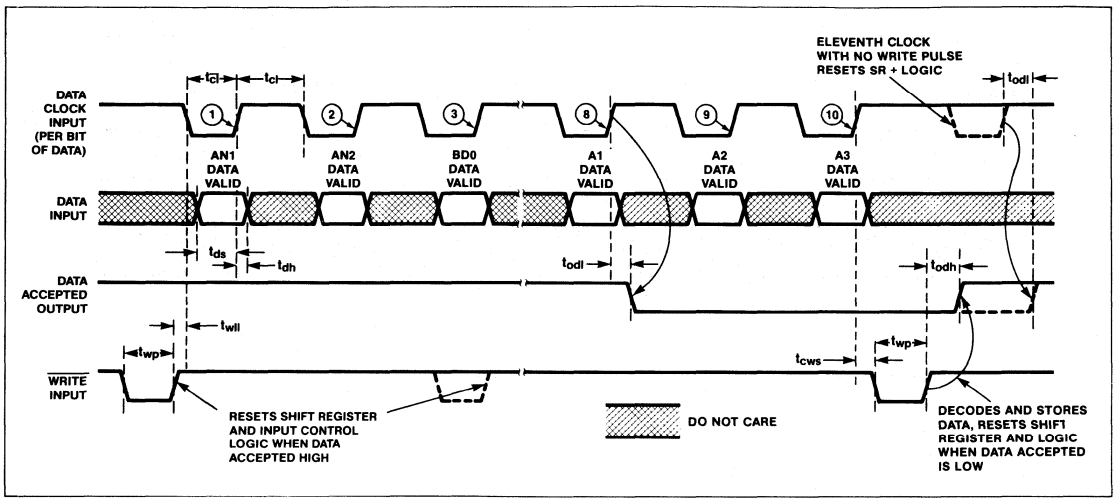


Figure 6. One Digit Timing Diagram for the MAX7232, Writing Both Annunciators.

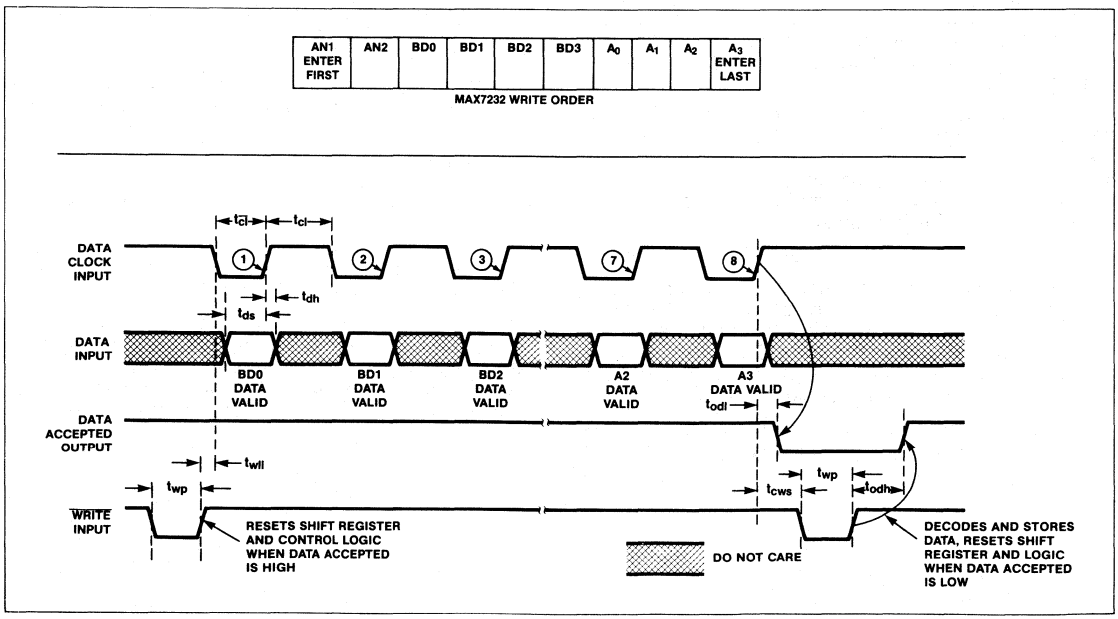


Figure 7. Input Timing Diagram of the MAX7232. Both Annunciators OFF.

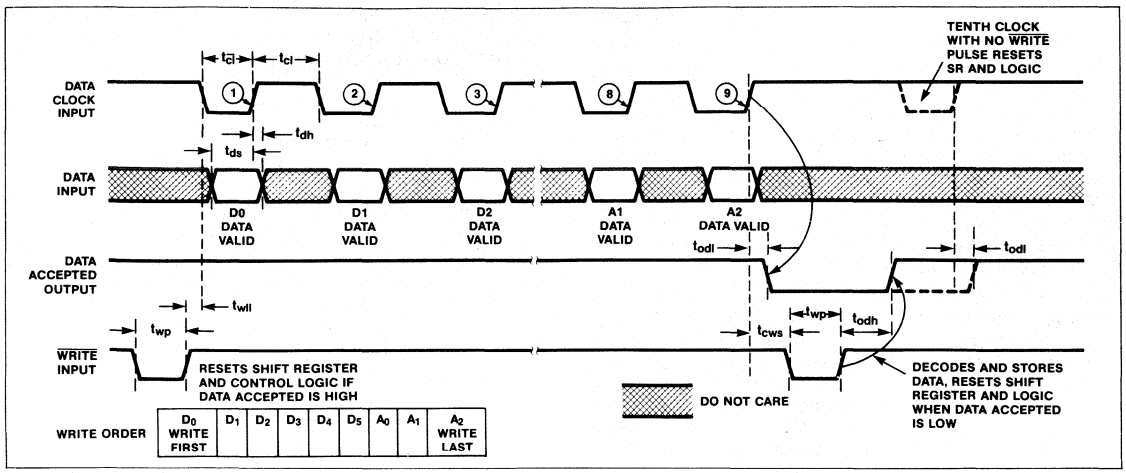


Figure 8. One Character Input Timing Diagram of the MAX7234.

Temperature Compensation

Temperature Effects

Temperature affects the performance of liquid crystal displays (LCD's) in two ways. As the display temperature drops, the response time of the display becomes longer. At very low temperatures, some displays may take several seconds to change to a new character. However, high-speed liquid crystal materials are available for low temperature environments.

Temperature has a significant effect on the variation of liquid crystal threshold voltage. The peak voltage (V_P) required to turn on the display has a temperature coefficient of -7 to -14 mV/°C for typical liquid crystal materials used in multiplexed LCD's. This means that as the temperature increases, the threshold voltage decreases. Figure 9 illustrates the dependence of peak voltage (V_P) on temperature for the same liquid crystal material described in Figure 10. Assuming a fixed value for V_P, OFF segments begin to be visible when the threshold voltage drops below $V_P/3$. To avoid this problem at high temperature, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This is appropriate where display temperatures do not vary widely.

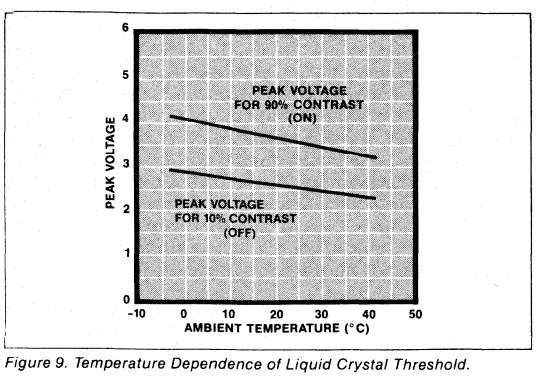


Figure 9. Temperature Dependence of Liquid Crystal Threshold.

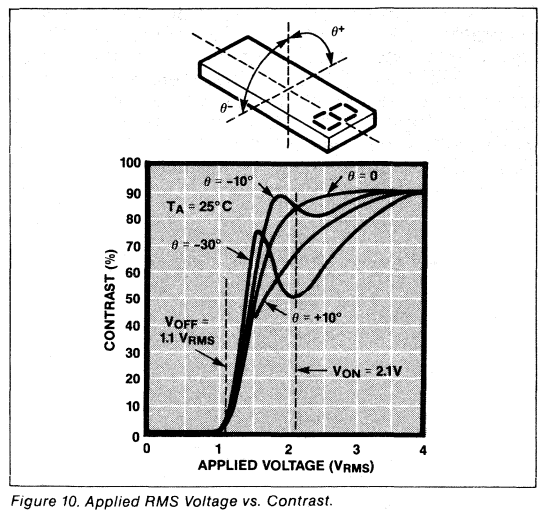


Figure 10. Applied RMS Voltage vs. Contrast.

Triplexed LCD Decoder/Drivers

Display Voltage

An internal resistor string of three equal value resistors is used to generate the display drive voltages. One end of the string is available at Pin 2 (V_{DISP}) and the other end is connected to V^+ on the chip. Pin 2, the user's input, allows the display voltage to be optimized for a particular liquid crystal material. Note that V_P should be three times the threshold voltage for the liquid crystal material used ($V_P = V^+ - V_{DISP}$). To avoid device latchup and possible destruction of the chip, never drive Pin 2 below Ground or above V^+.

Figure 11 illustrates a simple method of generating a display voltage suitable for a particular display. A potentiometer with a maximum value of 200kΩ connected from Pin 2 to Ground gives sufficient range adjustment to suit most displays. Due to the positive temperature coefficient of the resistors on-chip, this method for generating display voltage should be used only in applications where the temperature variation of the chip and display will not vary more than ±5°C (15°F). The power supply voltage also effects the display voltage.

The chip may be operated at the display voltage with V_{DISP} connected to Ground in battery powered applications where the display voltage is the same as the battery voltage (typically 3 to 4.5 volts). The inputs of the chip are designed such that they may be driven above V^+ without damage. This allows the chip and display to operate at a regulated 3V while its inputs are driven by a microprocessor that is operating at a less well controlled 5V supply. Under no circumstances should the inputs be driven more than 6.5V above Ground. Independent adjustment of both voltage and temperature compensation is illustrated in Figure 12. Temperature compensation is performed by the ICL7663.

Another method of setting up a display voltage is illustrated in Figure 13. The five diodes (1N914 or equivalent), each have a forward drop of approximately 0.65V, with 20 (μA) at room temperature. This configuration is suitable for the 3V display using the material properties as shown in Figures 9 and 10. More diodes may be added for higher voltage displays. Each diode has a negative temperature coefficient of -2mV/°C (5 in series gives -10mV/°C). Consequently, this circuit will provide reasonable temperature compensation.

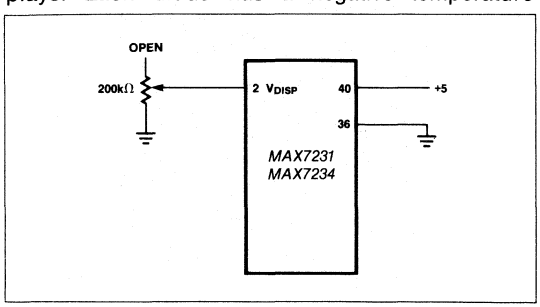


Figure 11. Simple Display Voltage Adjustment.

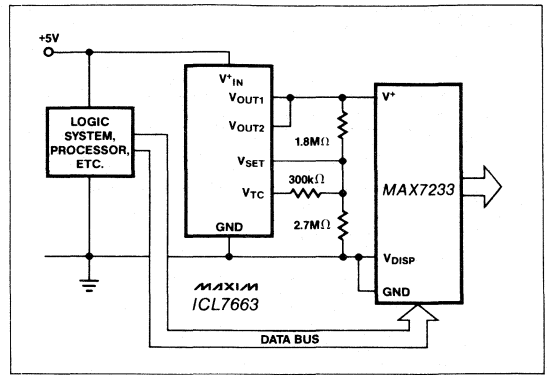


Figure 12. Flexible Temperature Compensation.

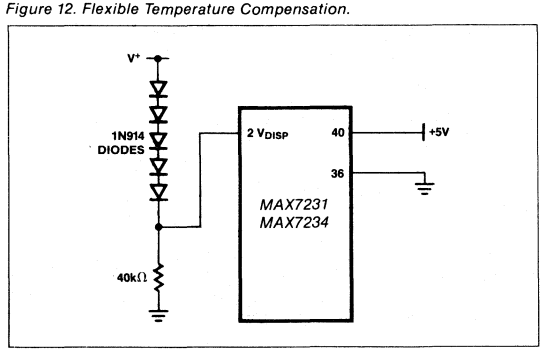


Figure 13. Diode String VDISP Generator.

Triplexing

The connection diagram for a typical 7-segment display font with 2 annunciators is illustrated in Figure 15. The MAX7231 and MAX7232 (A and B suffix versions) numeric display drivers use this configuration. The voltage waveforms of the common lines and one segment line are illustrated in Figure 14. The "Y" segment line has been chosen as an example. This line intersects with COM1 to form the "A" segment, COM2 to form the "G" segment, and COM3 to form the "D" segment. Four different ON/OFF combinations of the "A", "G" and "D" segments and their corresponding waveforms of the "Y" segment line are illustrated in Figure 14. The schematic diagram in Figure 16 shows that each intersection acts as a capacitance from segment line to common line. Figure 17 illustrates the voltage across the "G" segment for the same four combinations of ON/OFF segments shown in Figure 14.

The RMS voltage across the segment determines the degree of polarization for the liquid crystal material and thus the contrast of the segment. The

RMS OFF voltage is always $V_P/3$, whereas the RMS ON voltage is always 1.92 $V_P/3$. This is illustrated in Figure 17. The ratio of RMS ON to OFF voltage is fixed at 1.92 for a triplexed liquid crystal display.

Contrast vs. applied RMS voltage is shown in Figure 10. With a V_P of 3.1V, the RMS ON voltage is 2.1V and the RMS OFF voltage is 1.1V. The OFF segment will have a contrast of less than 5%, while the ON segments will have greater than 85% contrast.

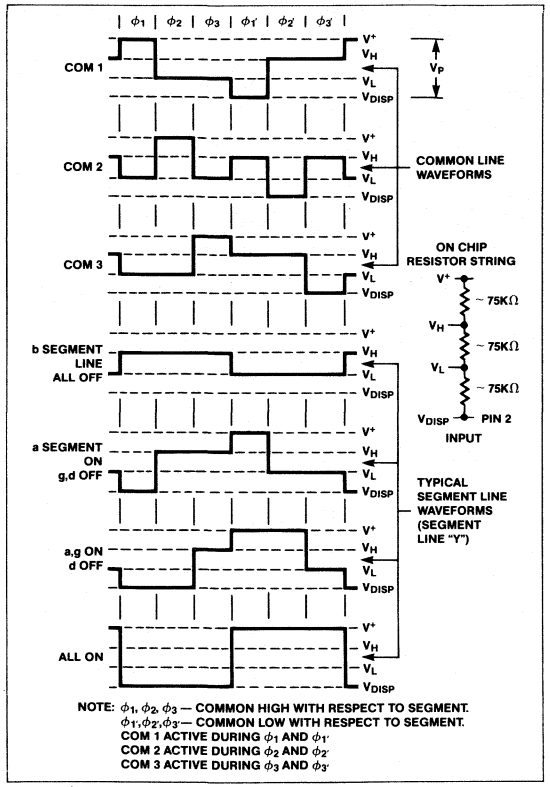


Figure 14. Display Voltage Waveforms.

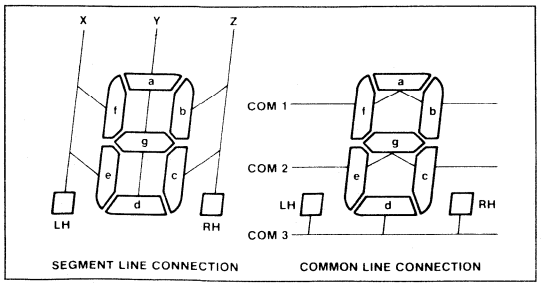


Figure 15. Connection Diagrams for Typical 7-Segment Displays.

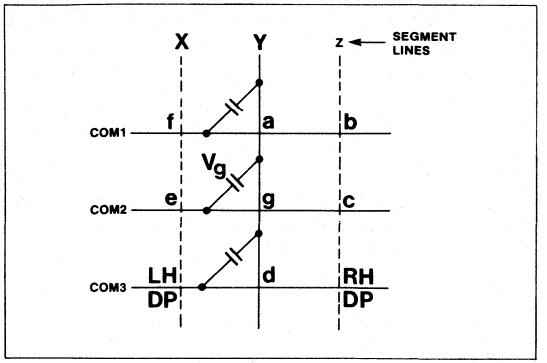


Figure 16. Schematic of Display.

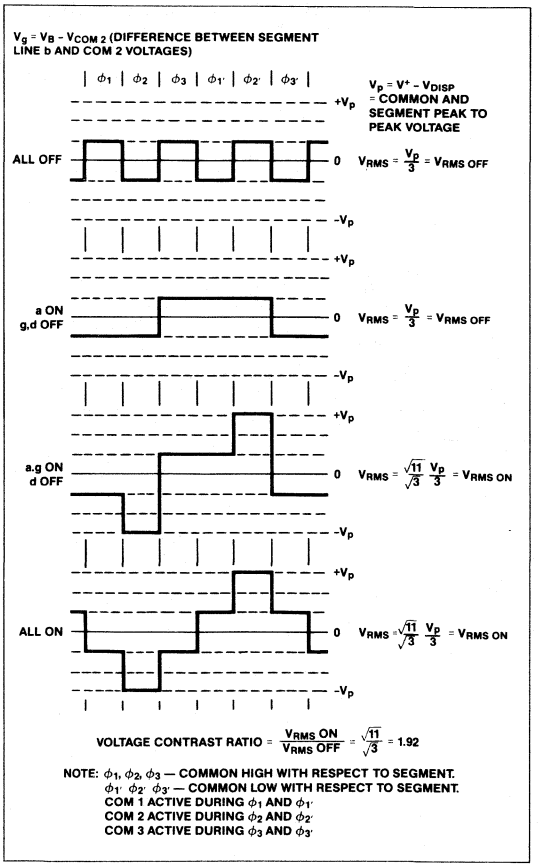


Figure 17. Voltage Waveforms on Segment g (Vg).

Triplexed LCD Decoder/Drivers

Output Codes and Display Fonts

The MAX7231 and MAX7232 numeric display drivers are programmed to drive 7-segment displays plus 2 annunciators per digit. Refer to Table 1 for annunciator input controls. The display connections for one digit are shown in Figure 18. Both annunciators are placed on COM3 on the "A" and "B" suffix devices. The "A" devices offer a "hexadecimal" 7-segment output, while the "B" devices offer "Code B" outputs. This is illustrated in Table 2. Figure 19 illustrates the "C" device configuration. The Left hand annunciator is placed on COM1 (AN2) and the right hand annunciator (usually a decimal point) is placed on COM3 (AN1). Only a "Code B" output is offered for the "C" devices.

Both the MAX7233 and MAX7234 are supplied in "A" and "B" versions, decoding an ASCII 6-bit subset to an 18-segment display, with 16 "flag" segments and 2 "dots". Figure 20 illustrates the layout for a single character. The "A" devices have numbers which are half-width and the "B" devices have full-width numbers. Refer to Table 3 for output decoding.

Table 1: Annunciator Decoding

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	MAX7231 A/B MAX7232 A/B BOTH ANNUNCIATORS ON COM 3	MAX7231C MAX7232C LH ANNUNCIATOR COM 1 RH ANNUNCIATOR COM 3
0	0	8	8
0	1	.8	8.
1	0	8.	.8
1	1	.8.	.8.

Table 2: Binary Data Decoding (MAX7231/MAX7232)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

Table 3: Data Decoding — 18 Segment (MAX7233/MAX7234)

CODE INPUT				DISPLAY OUTPUT				
				D5	D4		A VERSION	B VERSION
D3	D2	D1	D0	0,0	0,1	1,0	1,1	
0	0	0	0	@	P		0	0
0	0	0	1	A	Q	!	1	1
0	0	1	0	B	R	"	2	2
0	0	1	1	C	S	#	3	3
0	1	0	0	D	T	$	4	4
0	1	0	1	E	U	%	5	5
0	1	1	0	F	V	&	6	6
0	1	1	1	G	W	'	7	7
1	0	0	0	H	X	(	8	8
1	0	0	1	I	Y	)	9	9
1	0	1	0	J	Z	*	:	
1	0	1	1	K	[	+	;	
1	1	0	0	L	\	,	<	
1	1	0	1	M	]	-	=	
1	1	1	0	N	^	.	>	
1	1	1	1	O	_	/	?	

Table 4: Address Decoding (MAX7231/7232)

CODE INPUT				DISPLAY OUTPUT
MAX 7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

Table 5: Address Decoding (MAX7233/7234)

CODE INPUT			DIGIT SELECTED
MAX 7234 ONLY A2	A1	A0	
0	0	0	D1
0	0	1	D2
0	1	0	D3
0	1	1	D4
1	0	0	D5
1	0	1	NONE
1	1	0	NONE
1	1	1	NONE

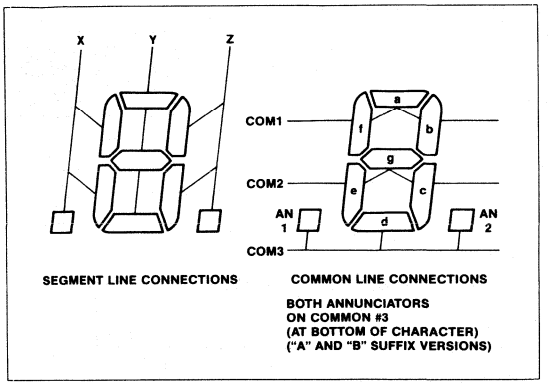


Figure 18. Display Fonts for MAX7231 and 7232. (Suffix Versions "A" and "B").

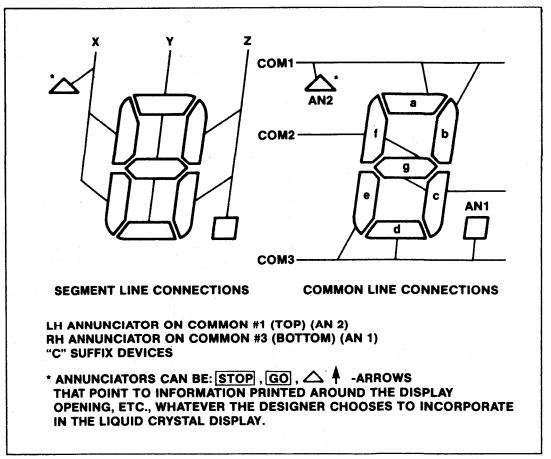


Figure 19. Display Fonts for MAX7231 and 7232. (Suffix Version "C").

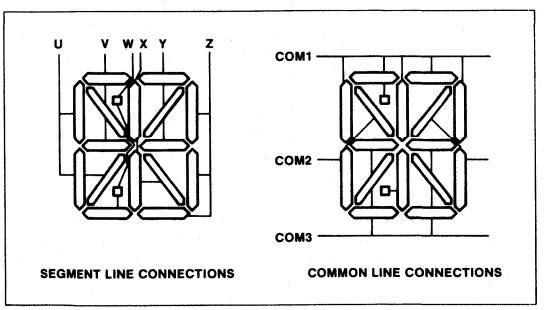


Figure 20. Display Fonts for MAX7233 and 7234. (18-Segment Alphanumeric).

Triplexed LCD Decoder/Drivers

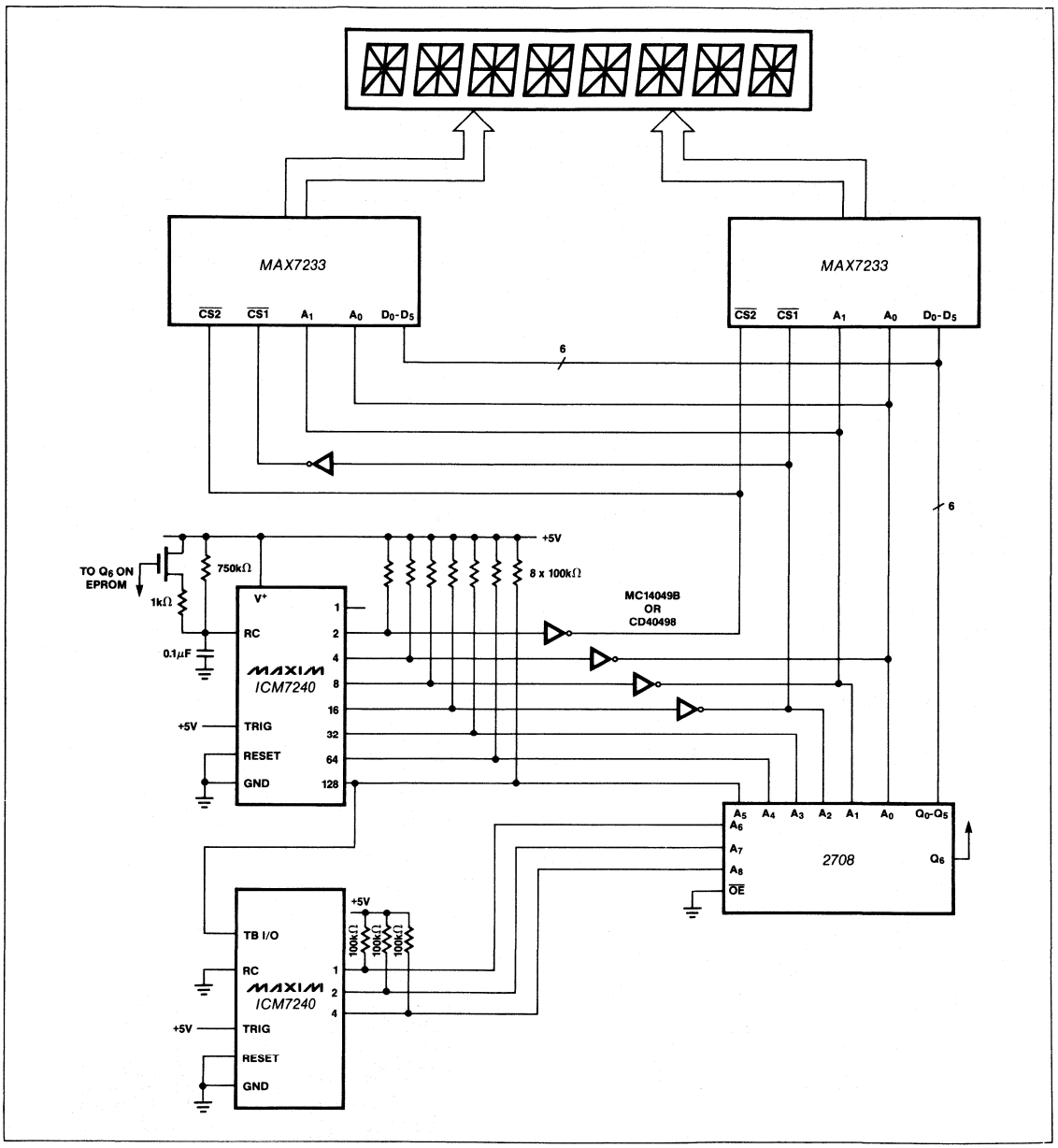


Figure 21. EPROM-Coded Message System. This circuit cycles through a message coded in the EPROM, pausing at the end of each line, or whenever coded on Q_6.

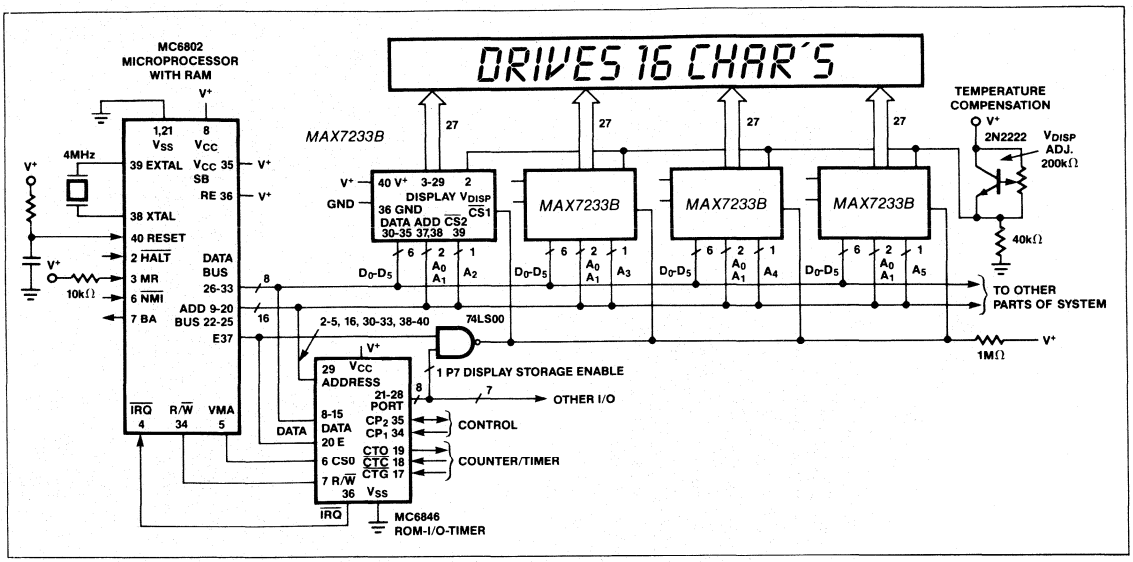
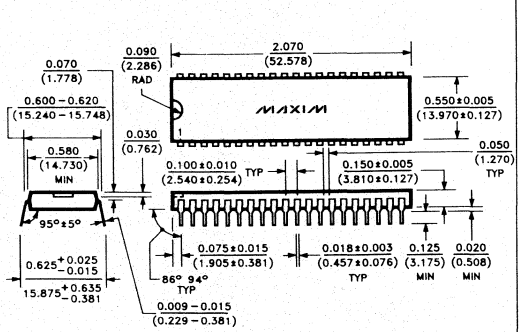
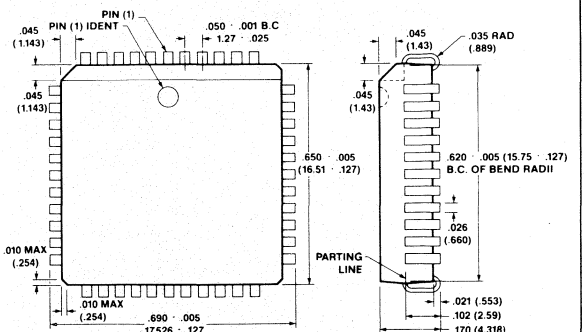


Figure 22. MC6802 Microprocessor with 16 Character 16 Segment ASCII Liquid Crystal Display.

Package Information



40 Lead Plastic (PL)
θ_{JA} = 100°C/W, θ_{JC} = 45°C/W

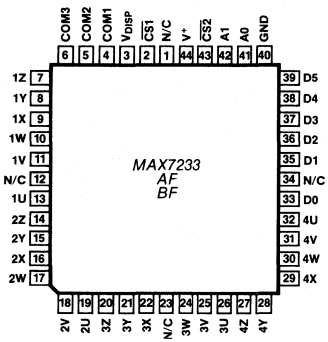


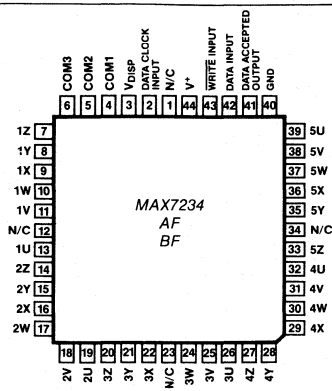
44 Lead Plastic Chip Carrier (Quad Pack) (Q)

Triplexed LCD Decoder/Drivers

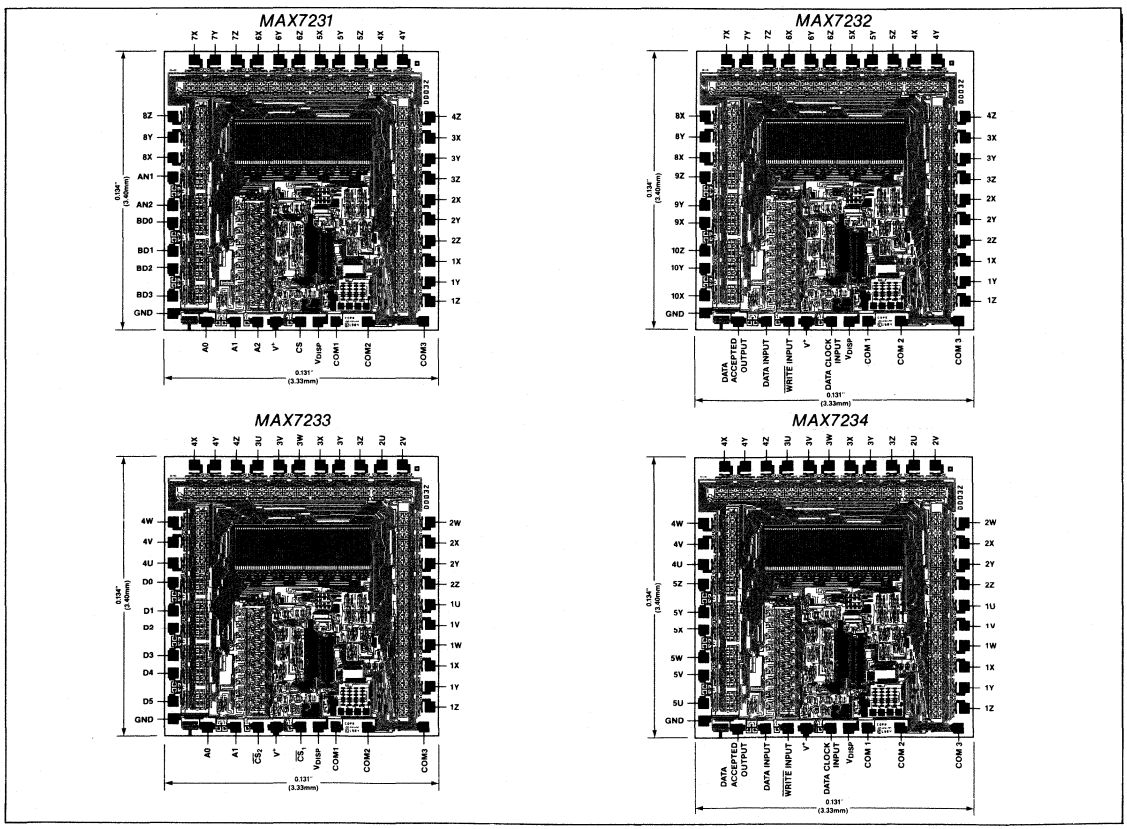
Pin Configuration

Top View





Chip Topography



MAXIM
4 Digit (LED) Presettable Up/Down Counter

General Description

The Maxim ICM7217 family of 4 digit presettable up/down counters contain a 4 digit, 7 segment LED display driver and a presettable comparison (predetermining) register. The counter and comparison register can be preset using either thumbwheel switches, jumpers, or external digital logic.

The ICM7217 (common anode) and ICM7217A (common cathode) are decade counters with a maximum count of 9999. The ICM7217B (common anode) and ICM7217C (common cathode) are modulo 60 counters intended for hours/minutes or minute/seconds timing applications, and have a maximum count of 5959.

These devices also provide multiplexed BCD outputs, a Carry/Borrow output allowing ICM7217s to be cascaded, a Zero output which indicates when the count is equal to zero, and an Equal output which indicates when the count is equal to the value contained in the comparison register. The ICM7217 also has a Reset input and a display latch with store input.

Applications

The Maxim ICM7217 significantly reduces the number of components required in many timing, counting and frequency counter applications.

Typical applications include:

Predetermining Batch Counter
Tachometer
Over/Under Speed Detector
Count Down/Elapsed Tim
Unit Counter
Frequency Counte

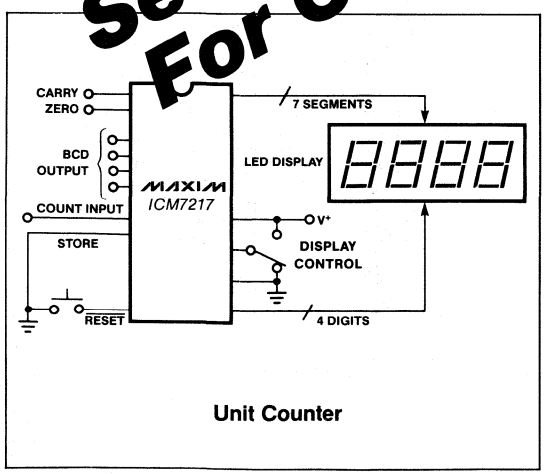
Features

- ♦ **Pin for Pin Second Source!**
- ♦ **4 Digit Up/Down Counter**
- ♦ **Directly Drives LED Display**
- ♦ **Presettable Counter and Compare Register**
  Interfaces with Thumbwheel Switches or Digital Logic
- ♦ **Can Be Cascaded**
- ♦ **Multiplexed BCD I/O**
- ♦ **Up/Down, Store and Reset Inputs**
- ♦ **Monolithic, Low Power CMOS Design**

Ordering Information

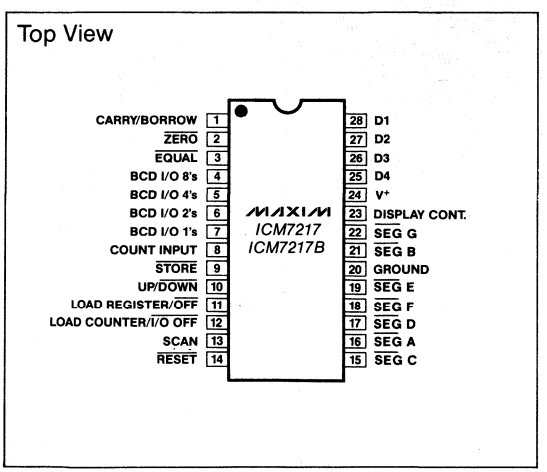
PART	TEMP. RANGE	PACKAGE
ICM7217IJI	-20°C to +85°C	28 Lead CERDIP
ICM7217IPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217CIPI	-20°C to +85°C	28 Lead Plastic DIP

Typical Operating Circuit



Unit Counter

Pin Configuration



MAXIM

4½ Digit Counter/Decoder/Driver

General Description

The Maxim ICM7224(LCD) and ICM7225(LED) are high speed 4½ digit counters, featuring segment decoders, leading zero blanking, store and reset inputs, and a carry output that allows cascading of 8 or more digits. The ICM7224 directly drives a non-multiplexed liquid crystal display(LCD). The ICM7225 has 29 constant current outputs for driving a non-multiplexed common anode display.

These counters operate with inputs from DC to 15 MHz while using only 50 μA of supply current. A Schmitt trigger on the count input ensures reliable operation in noisy environments and in applications with slowly varying inputs.

The ICM7224 and ICM7225 are now available in a 44 lead plastic chip carrier package in addition to the standard 40 lead plastic DIP.

Applications

Unit Counter
Frequency Counter
Tachometer
Hour Meter
Totalizer

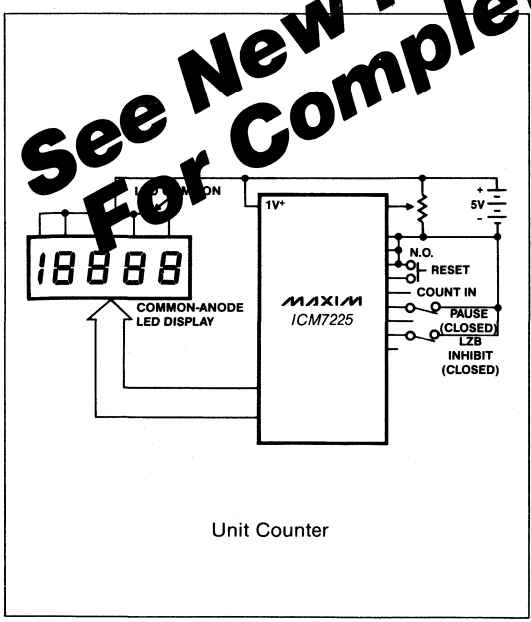
Features

- **Pin For Pin Second Source!**
- **High Speed Up Counter: 25MHz Typ.**
- **Leading Zero Blanking**
- **Can Be Cascaded for 8 or More Digits**
- **STORE and RESET Inputs for Frequency Counter Applications**
- **On-Board Oscillator to Provide Backplane Frequency (ICM7224)**
- **Brightness Control Input(ICM7225)**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7224IPL	[illegible] to +85°C	[illegible] Plastic DIP
ICM7224[illegible]	[illegible] to +85°C	44 Lead Plastic Chip Carrier
ICM7224[illegible]	0°C to +[illegible]	Dice
ICM7225IPL	[illegible] to +85°C	40 Lead Plastic DIP
ICM7225C[illegible]	[illegible] to +85°C	44 Lead Plastic Chip Carrier
ICM7225[illegible]	0°C to +85°C	Dice

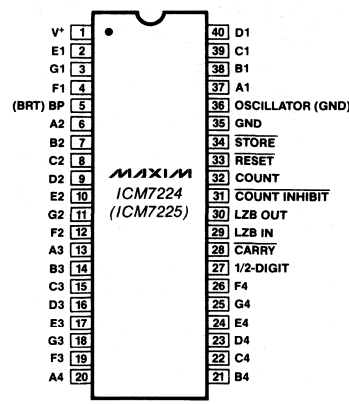
Typical Operating Circuit



Unit Counter

Pin Configuration

Top View



Power Supply Circuits

MAXIM
Monolithic Voltage Converter

General Description

The Maxim ICL7660 is a monolithic charge pump voltage inverter that will convert a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage in the range of −1.5V to −10V. The ICL7660 provides performance far superior to previous implementations of charge pump voltage inverters by combining low quiescent current with high efficiency, and by eliminating diode drop voltage losses. The ICL7660 has an oscillator, control circuitry, and 4 power MOS switches on-chip, with the only required external components being two low cost electrolytic capacitors.

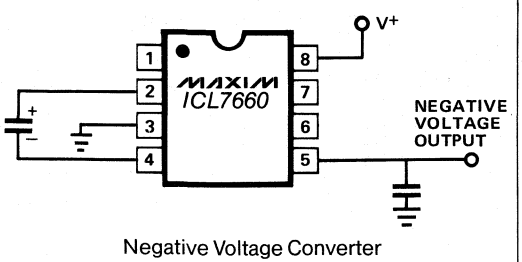
Applications

The ICL7660 can be used wherever negative voltages in the range of −1.5V to −10V are desired. A common use is to generate a −5V supply for use with analog circuitry, using the standard +5V logic supply as the power source. Another popular usage is to convert a +9V battery voltage to −9V, which can then be regulated to −5V by the Maxim ICL7664.

The ICL7660 can also be used to double the output voltage of a battery, generating a 3V total supply voltage from a single 1.5V flashlight battery or generating a 6V total supply voltage from a single lithium cell. Typical applications include:

Handheld instruments
RS-232 power supply
Data acquisition systems
−5V supply from +5V logic supply
Panel meters
Operational amplifier power supplies
Positive to negative voltage conversion

Typical Operating Circuit



Negative Voltage Converter

(Detailed Circuit Diagram — Figure 4)

Features

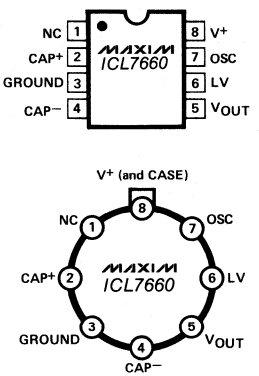
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **No Diode Required for High Voltage Operation**
- **Simple Voltage Conversion: +5V to ±5V**
- **98% Power Efficiency (typ)**
- **Wide Voltage Range: 1.5V to 10V**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7660CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7660CSO	0°C to +70°C	8 Lead Small Outline
ICL7660CTV	0°C to +70°C	TO-99 Can
ICL7660IJA	-20°C to +85°C	8 Lead CERDIP
ICL7660ITV	-20°C to +85°C	TO-99 Can
ICL7660MTV	(Order ICL7660AMTV)	
ICL7660AMTV	-55°C to +125°C	TO-99 Can
ICL7660C/D	0°C to +70°C	Dice

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Monolithic Voltage Converter

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V^++0.3V) for $V^+ < 5.5V$
(V^+−5.5V) to (V^++0.3V) for $V^+ > 5.5V$
Current into LV (Note 1) ..... 20μA for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous
Power Dissipation (Note 2)
ICL 7660CTV 500mW
ICL 7660CPA 300mW
ICL 7660MTV 500mW
ICL 7660C50 (Maxim) 200mW
ICL 7660IJA (Maxim) 500mW
Operating Temperature Range
ICL 7660M ..... −55°C to +125°C
ICL 7660I (Maxim) ..... −20°C to +85°C
ICL 7660C (Maxim) ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature
(Soldering, 10 sec.) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +2 to +15 volts; T_A = 25°C, Unless Noted)

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Supply Current	I^+		170	500	μA	$R_L = \infty$
Supply Voltage Range - Hi	V^+_{H1}	3.0		6.5	V	0°C ≤ T_A ≤ 70°C, R_L = 10kΩ, LV Open
(D_X out of circuit) (Note 3)		3.0		5.0	V	−55°C ≤ T_A ≤ 125°C, R_L = 10kΩ, LV Open
Supply Voltage Range - Lo (D_X out of circuit)	V^+_{L1}	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND
Supply Voltage Range - Hi (D_X in circuit)	V^+_{H2}	3.0		10.0	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV Open
Supply Voltage Range - Lo (D_X in circuit)	V^+_{L2}	1.5		3.5	V	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND
Output Source Resistance	R_{OUT}		55	100	Ω	I_{OUT} = 20mA, T_A = 25°C
				120	Ω	I_{OUT} = 20mA, −20°C ≤ T_A ≤ +70°C
				150	Ω	I_{OUT} = 20mA, −55°C ≤ T_A ≤ +125°C (Note 3)
				300	Ω	V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, −20°C ≤ T_A ≤ +70°C
				400	Ω	V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, −55°C ≤ T_A ≤ +125°C, D_X in circuit (Note 3)
Oscillator Frequency	f_{OSC}		10		kHz	
Power Efficiency	P_{Ef}	95	98		%	R_L = 5kΩ
Voltage Conversion Efficiency	$V_{OUT\ Ef}$	97	99.9		%	$R_L = \infty$
Oscillator Impedance	Z_{OSC}		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V = 5 Volts

NOTE 1: Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.

NOTE 2: Derate linearly above 50°C by 5.5mW/°C.

NOTE 3: ICL7660M only.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Monolithic Voltage Converter

- Lower supply current
- Supply current guaranteed over temperature
- No diode required for high voltage operation (Note 1)
- Wide 1.5V to 10V operating voltage range
- Improved SCR Latch-up protection
- Guaranteed 99% voltage conversion efficiency
- Improved ESD protection (Note 3)
- Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
($V+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test circuit-Figure 1; unless noted.)

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Supply Current	I^+		**110**	**175** **225** **250**	**μA** **μA** **μA**	**$T_A = 25°C$, $R_L = \infty$** **$T_A = 0°C \le T_A \le +70°C$, $R_L = \infty$** **$T_A = -55°C \le T_A \le +125°C$, $R_L = \infty$**
Supply Voltage Range — Hi (Dx out of circuit)(Note 1)	V^+_{H1}	**3.0**		**10.0**	**V**	**MIN $\le T_A \le$ MAX, R_L = 10kΩ, LV Open**
Supply Voltage Range — Lo (Dx out of circuit)	V^+_{L1}	1.5		3.5	V	MIN $\le T_A \le$ MAX, R_L = 10kΩ, LV to GROUND
Output Source Resistance	R_{OUT}		55	100 120 140 150 250 300 400	Ω Ω Ω Ω Ω Ω Ω	I_{OUT} = 20mA, $T_A = 25°C$ I_{OUT} = 20mA, $0°C \le T_A \le +70°C$ I_{OUT} = 20mA, $0°C \le T_A \le +85°C$ I_{OUT} = 10mA, $-55°C \le T_A \le +125°C$ (Note 2) V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, $T_A = 25°C$ V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, $-20°C \le T_A \le +85°C$ V^+ = 2V, I_{OUT} = 3mA, LV to GROUND, $-55°C \le T_A \le +125°C$ (Note 2)
Oscillator Frequency	f_{OSC}		10		kHz	
Power Efficiency	P_{EF}	95	98		%	R_L = 5kΩ
Voltage Conversion Efficiency	$V_{OUT\,Ef}$	**99**	**99.9**		**%**	**$R_L = \infty$**
Oscillator Impedance	Z_{OSC}		1.0		MΩ	V^+ = 2 Volts
			100		kΩ	V^+ = 5 Volts

NOTE 1: The Maxim ICL7660 can operate without an external output diode over the full temperature and voltage range. The Maxim ICL7660 can also be used with the external output diode D_X, when replacing the Intersil ICL7660.

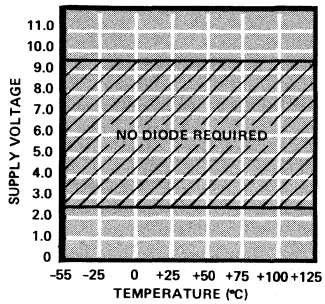
NOTE 2: Maxim ICL7660A only.

NOTE 3: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883B Method 3015.1 Test Circuit).

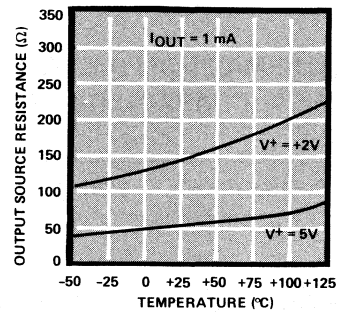
Monolithic Voltage Converter

Typical Operating Characteristics

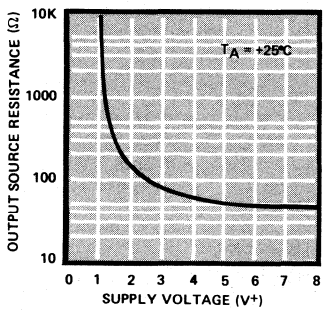
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



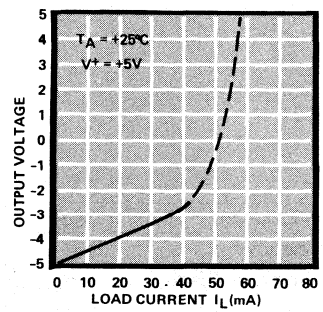
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



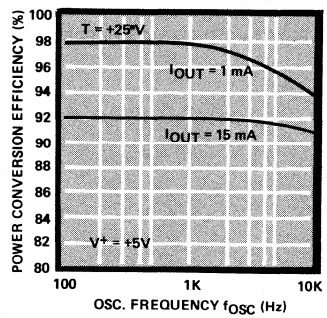
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



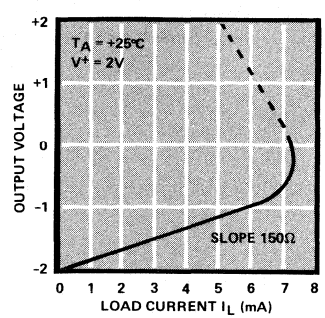
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY

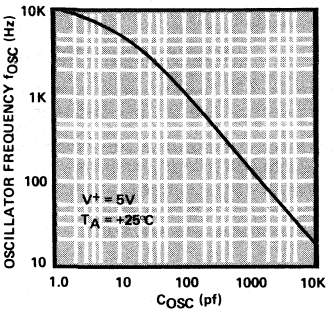


OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

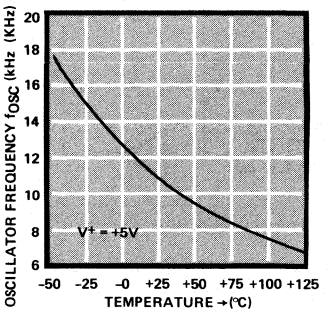


Typical Operating Characteristics

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

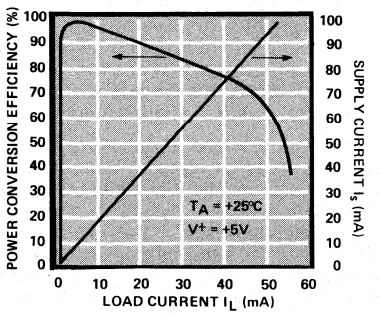


UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

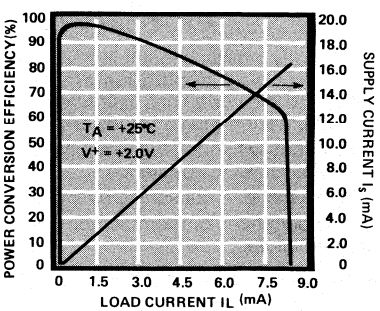


SUPPLY CURRENT CURVES below include current that is fed directly into the load (R_L) from V+ (see Figure 1). The supply current is divided equally into the positive and negative side (via the ICL7660) to the load. Ideally, $V_{OUT} \simeq V_{IN}$, $I_S \simeq 2I_L$ so $V_{IN} \cdot I_S \simeq 2 \cdot V_{OUT} \cdot I_L$.

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



SUPPLY CURRENT POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



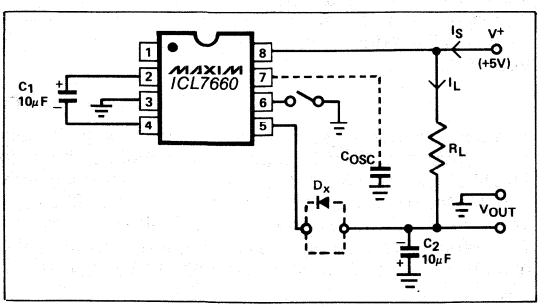


Figure 1. Maxim ICL7660 test circuit. (C_1 and C_2 should be increased to 100μF if C_{OSC} exceeds 10pF.) Note: Dx not required with Maxim ICL7660.

Detailed Description

All the circuitry necessary to complete a voltage doubler is contained on the ICL7660. Only 2 external capacitors are needed. These may be inexpensive 10μF polarized electrolytic capacitors. Figure 2, an idealized voltage doubler, illustrates ICL7660 operation. During the first half of the cycle, switches S_2 and S_4 are open, switches S_1 and S_3 are closed, and the capacitor C_1 is charged to a voltage $V.^+$ During the second half cycle, switches S_1 and S_3 are open, S_2 and S_4 are closed, and the capacitor C_1 undergoes a negative shift equal to V^+ volts. Assuming ideal switches and no load on C_2, charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly $-(V^+)$.

Monolithic Voltage Converter

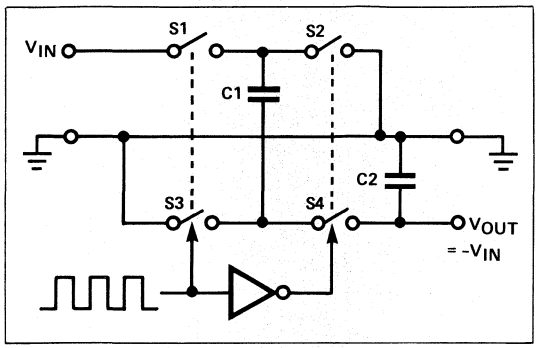


Figure 2. Idealized voltage doubler.

The four switches in Figure 2 are MOS power switches. Switch S_1 is a P-channel device, and switches S_2, S_3, and S_4 are N channel devices.

To improve low voltage operation the regulator should be disabled by connecting the "LV" pin to Ground. This is recommended to compensate for the inherent voltage drop associated with the voltage regulator portion of the ICL7660. To prevent device damage and insure latch-free operation, the "LV" pin must be left open if the supply voltage exceeds 3.5V.

Efficiency Considerations

Theoretically a voltage multiplier can approach 100% efficiency if certain conditions are met. The ICL7660 approaches the conditions listed below for negative voltage multiplication if large values of C_1 and C_2 are used.

- ◊ The output switches have virtually no offset and extremely low ON resistance.
- ◊ Minimal power is consumed by the drive circuitry.
- ◊ The impedances of the reservoir and pump capacitors are negligible.

The energy loss per charge pump cycle is:

$$E = \frac{1}{2} C_1 (V^{+2} - V_{OUT}^2)$$

There will be a substantial voltage difference between V^+ and V_{OUT} if the impedances of C_1 and C_2 at the pump frequency are high compared to the output load R_L. To reduce output ripple, make C_2 as large in value as is practical. Increasing the value of both C_1 and C_2 will improve the efficiency.

General Precautions

- ◊ The positive terminal of C_1 must be connected to Pin 2 of the ICL7660 and the positive terminal of C_2 must be connected to Ground.
- ◊ Never exceed maximum supply voltages.
- ◊ Do not connect the "LV" terminal to Ground for supply voltages greater than 3.5V.
- ◊ The output to V^+ supply should not be short-circuited for extended periods of time when supply voltages exceed 5.5V. Transient conditions including startup are acceptable.

Maximum Operating Limits

The Maxim ICL7660 will operate over the entire operating temperature range with an input voltage of 1.5V to 10V.

The Maxim ICL7660, unlike the Intersil device, does not require a protective diode in series with the output. Leaving this diode in the circuit will have no effect on the Maxim ICL7660, although the diode does reduce the output voltage by approximately 0.6V.

Applications

Changing Oscillator Frequency

Normally the OSC pin of the ICL7660 is left open and the 10kHz nominal oscillator frequency (5kHz charge pump frequency) is used. The oscillator frequency can be lowered by connecting an external capacitor between OSC and V^+. A graph in the Typical Characteristics section shows the nominal frequency vs. capacitor value. Lowering the oscillator frequency will improve the conversion efficiency with very low output current levels. An undesirable effect of lowering the oscillator frequency is that the impedance level of the pump capacitors will increase. Increasing the value of C_1 and C_2 will compensate for this increase in impedance.

In some applications, particularly audio amplifiers, the 5kHz output ripple frequency is objectionable. The oscillator frequency may be increased by overdriving the OSC pin with an external oscillator. To eliminate the possibility of SCR latchup, insert a 1kΩ resistor in series with the OSC input. If the external clock source does not swing all the way to V^+, a 10kΩ pullup resistor should be used. The pump frequency, and therefore the output ripple frequency, will be one-half the external clock frequency. Driving the ICL7660 with a higher frequency clock will slightly increase the quiescent current, but allows the use of smaller value external capacitors and increases the ripple frequency.

Cascading Devices

To produce larger negative multiplication of the initial supply voltage, the ICL7660 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the weighted sum of the individual ICL7660 R_{OUT} values. For light loads, the practical limit is 10 devices. The output voltage where n is an integer representing the number of devices cascaded, is defined by $V_{OUT} = -n (V_{IN})$.

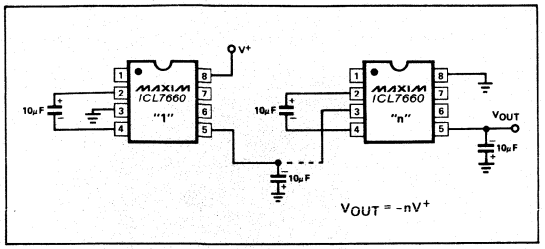


Figure 3. Cascading ICL7660's for increased output voltage.

Negative Voltage Converter

The most common application of the ICL7660 is as a charge pump voltage inverter, converting a positive voltage to the corresponding negative voltage. The simple circuit of Figure 4 shows that only two external components, C_1 and C_2 are needed. In most applications C_1 and C_2 are low cost 10μF electrolytic capacitors. The ICL7660 is NOT a voltage regulator and the output source resistance is approximately 70Ω with +5V input. This means that with an input voltage of +5V, the output voltage will be −5V under light load, but will decrease to about −4.3V with a 10mA load current. The output source resistance vs. temperature and supply voltage is depicted in the typical characteristics graphs. The output impedance of the complete circuit is the sum of the ICL7660 output resistance and the impedance of the pump capacitors at the pump frequency.

The ripple voltage on the output can be calculated by noting that the output current is supplied solely from capacitor C_2 during one-half of the charge pump cycle. This introduces a ripple of:

$$U_{RIPPLE} = [½(F_{PUMP})]\, I_{OUT}\, (1/C_2)$$

For the nominal F_{PUMP} of 5kHz (one-half of the nominal 10kHz oscillator frequency) and a 10μF C_2, the ripple will be approximately 10mV with an output current of 10mA.

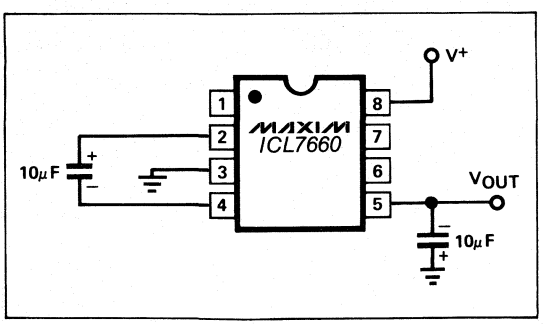


Figure 4. Negative voltage converter.

Paralleling Devices

Paralleling multiple ICL7660's reduces the output resistance. As illustrated in Figure 5, each device requires its own pump capacitor C_1, however the reservoir capacitor, C_2, serves all devices. The equation for calculating output resistance is shown in Figure 5.

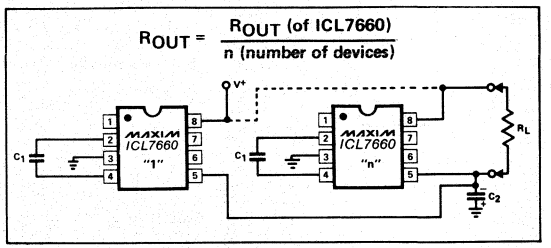


Figure 5. Paralleling ICL7660's to reduce output resistance.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 6. In this circuit, capacitor C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage. Capacitor C_2 and C_4 are respectively pump and reservoir for the multiplied positive voltage. This circuit configuration, however, does lead to higher source impedances of the generated supplies. This is due to the finite impedance of the common charge pump driver.

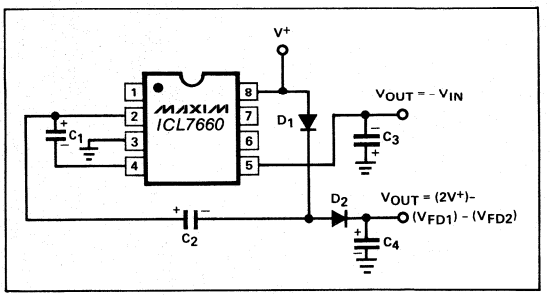


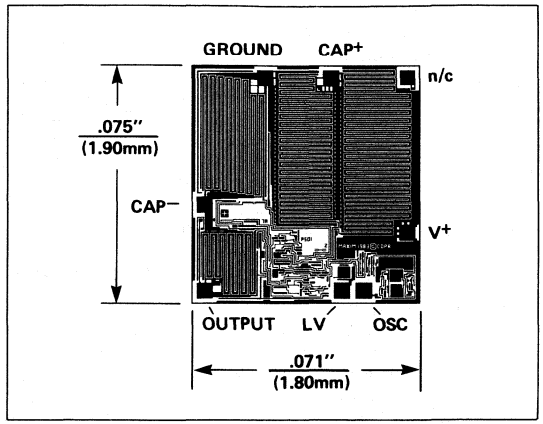
Figure 6. Combined positive multiplier and negative converter.

±5V Supply From a Single 9V Battery

Figure 7 shows a complete ±5V power supply using one 9V battery. The ICL7660 inverts the +9V input voltage for −9V which is then regulated by the ICL7664 negative regulator to a constant −5V output. The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA.

Monolithic Voltage Converter

Chip Topography



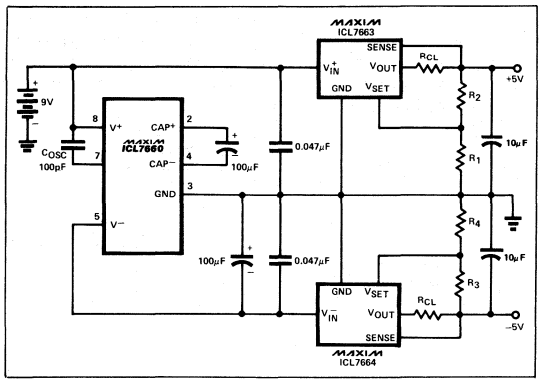
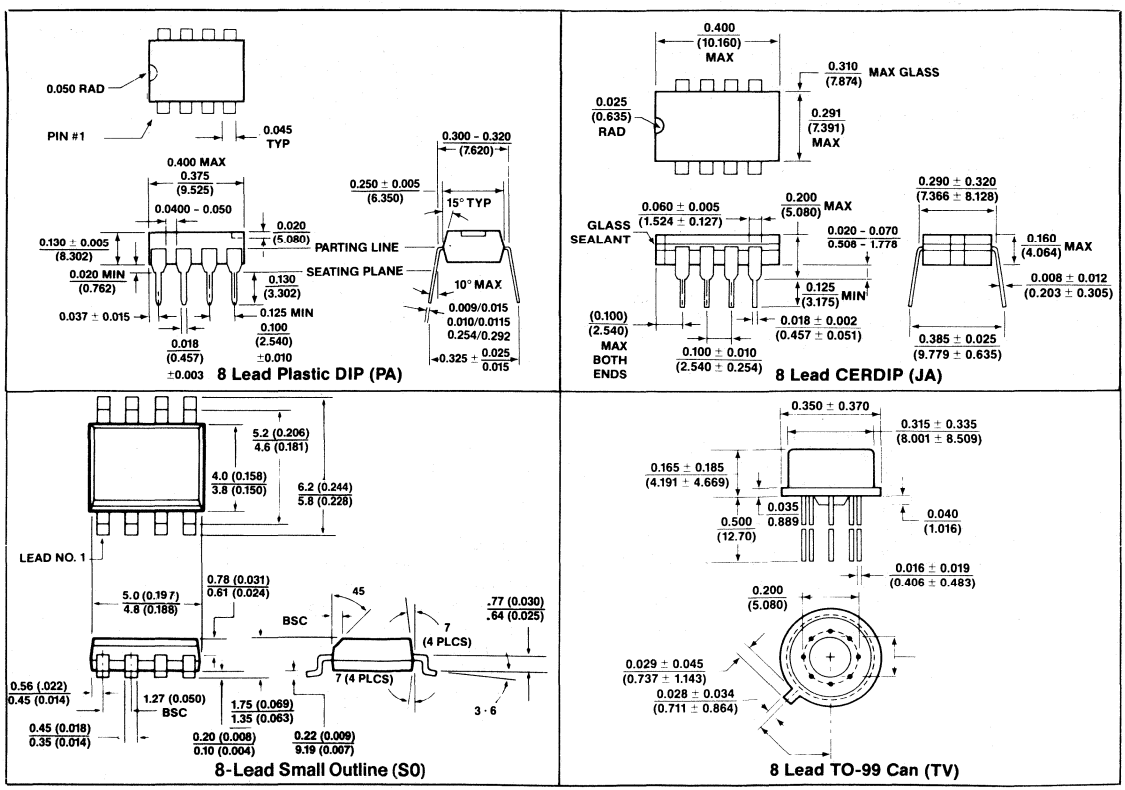


Figure 7. Regulated ±5 Volts from a battery using the Maxim ICL7663 and ICL7664.

Package Information



MAXIM

Programmable Positive Voltage Regulator

General Description

The Maxim ICL7663 is a high efficiency positive voltage regulator with a quiescent current of less than 10μA. The output voltage is set by two external resistors to any voltage in the 1.3–16V range, with an input voltage range of 1.5–16V. The ICL7663 is well suited for battery powered supplies, featuring low quiescent current, 40mA output current capability, low V_{IN} to V_{OUT} differential, and a logic input level shutdown control. In addition, the ICL7663 has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for multiplexed LCD display systems.

The Maxim ICL7663A is an enhanced version of the ICL7663, with a 1% accurate voltage reference, which eliminates the need for trimming the output voltage in most applications.

The ICL7663B is a reduced input voltage range version limited to a maximum of 10V input.

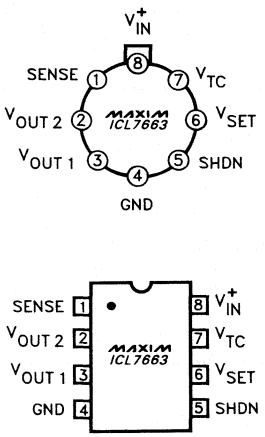
Applications

Designed specifically for battery powered systems, the ICL7663 positive voltage regulator excels wherever low quiescent power, wide voltage range operation, medium output current levels, current limiting, and logic-controlled shutdown is desired.

- Handheld Instruments
- Pagers
- LCD Display Module and Systems
- Remote Data Loggers

Pin Configuration

Top View



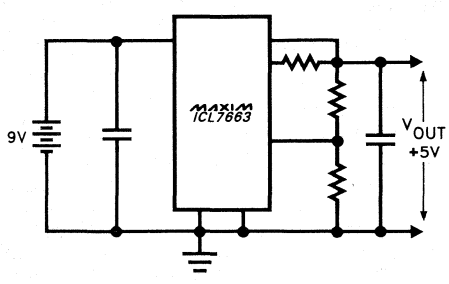
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **1% Output Voltage Accuracy (ICL7663A)**
- **Quiescent Current guaranteed over Temperature**
- **Improved Temperature Coefficient of Output Voltage**
- **40mA Output Current, with Current Limiting**
- **1.5V to 16V Operating Range**
- **Adjustable Output Voltage**
- **Low Input-to-Output Voltage Drop**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7663C/D	0°C to +70°C	Dice
ICL7663CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663IJA	−20°C to +85°C	8 Lead CERDIP
ICL7663ITV	−20°C to +85°C	TO-99 Can
ICL7663AC/D	0°C to +70°C	Dice
ICL7663ACPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663AIJA	−20°C to +85°C	8 Lead CERDIP
ICL7663AITV	−20°C to +85°C	TO-99 Can
ICL7663BC/D	0°C to +70°C	Dice
ICL7663BCPA	0°C to +70°C	8 Lead Plastic DIP
ICL7663BIJA	−20°C to +85°C	8 Lead CERDIP
ICL7663BITV	−20°C to +85°C	TO-99 Can

Typical Operating Circuit



Positive Voltage Regulator

(Detailed Circuit Diagram—Figure 3)

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Programmable Positive Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1)
(Terminals 1, 2, 3, 5, 6, 7) (GND − 0.3V) to (V_{IN}^+ + 0.3V)
Output Source Current
(Terminal 2) 50mA
(Terminal 3) 25mA
Output Sinking Current
(Terminal 7) ..... −10mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW
Cerdip (Maxim) 500mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN}^+ = 9V, V_{OUT} = 5V, T_A = +25°C, test circuit unless noted.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Input Voltage	V_{IN}^+	ICL7663 T_A = 25°C 20°C ≤ T_A ≤ +70°C ICL7663B T_A = 25°C 20°C ≤ T_A ≤ +70°C	 1.5 1.6 1.5 1.6	 	 16.0 16.0 10 10	 V V V V
Quiescent Current	I_Q	R_L = ∞, 1.4V ≤ V_{OUT} ≤ 8.5V; V_{IN}^+ = 16V, ICL7663 only V_{IN}^+ = 9V		4.0 3.5	12 10	µA µA
Reference Voltage	V_{SET}		1.2	1.3	1.4	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	8.5V < V_{IN}^+ < 9V		±200		ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	2V < V_{IN}^+ < 15V, ICL7663 2V < V_{IN}^+ < 9V, ICL7663B		0.03 0.03		%/V %/V
V_{SET} Input Current	I_{SET}			±0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled V_{SHDN}LO: Both V_{OUT} Enabled	1.4		 0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold Voltage	V_{CL}	V_{CL} = V_{OUT2} − V_{SENSE} (Current-Limit Threshold)		0.7		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	V_{IN}^+ = 2V V_{IN}^+ = 9V V_{IN}^+ = 15V, ICL7663 only		200 70 50		Ω Ω Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT1} = 100µA @ V_{OUT1} = 5V ΔI_{OUT2} = 10mA @ V_{OUT2} = 5V		2.0 1.0		Ω
Available Output Current (V_{OUT2})	I_{OUT2}	V_{IN}^+ = 3V V_{OUT} = V_{SET} V_{IN}^+ = 9V V_{OUT} = 5V V_{IN}^+ = 15V V_{OUT} = 5V, ICL7663 only	10 25 40			mA mA mA
Negative Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	(Includes V_{SET} Divider)			1.0	µA

Note 1: Connecting any terminal to voltages greater than (V_{IN}^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Programmable Positive Voltage Regulator

- ◆ 1% Output Voltage Accuracy (ICL7663A)
- ◆ Key Specifications Guaranteed Over Temperature
- ◆ Improved Output Voltage Temperature Coefficient
- ◆ Guaranteed Line and Load Regulation
- ◆ Improved ESD Protection (Note 5)
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS Specifications below satisfy or exceed all "tested" parameters on adjacent page.

V_{IN}^+ = 9V, V_{OUT} = 5V, T_A = 25°C, test circuit unless noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}^+	ICL7663 T_A = 25°C	1.5		16	V
		0°C ≤ T_A ≤ +70°C	1.6		16	V
		ICL7663A				
		0°C ≤ T_A ≤ +70°C	**2.0**		**16**	**V**
		ICL7663B T_A = 25°C	1.5		10	V
		0°C ≤ T_A ≤ +70°C	1.6		10	V
Quiescent Current	I_Q	1.4V ≤ V_{OUT} ≤ 8.5V, no load				
		V_{IN}^+ = 9V				
		ICL7663A, ICL7663, 0°C ≤ T_A ≤ +70°C			**10**	**µA**
		ICL7663B, T_A = 25°C			10	µA
		V_{IN}^+ = 16V				
		ICL7663, ICL7663A, 0°C ≤ T_A ≤ +70°C			**12**	**µA**
Reference Voltage	V_{SET}	I_{OUT1} = 100µA, V_{OUT} = V_{SET}, T_A = +25°C				
		ICL7663, ICL7663B	1.2		1.4	V
		ICL7663A	**1.275**	**1.29**	**1.305**	**V**
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	**0°C ≤ T_A ≤ +70°C**		**100**		**ppm**
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	**ICL7663, ICL7663A, V_{IN} = 2 − 15V,**				
		0°C ≤ T_A ≤ +70°C		**0.03**	**0.35**	**%/V**
		ICL7663B, V_{IN} = 2 − 9V		0.03		%/V
V_{SET} Input Current	I_{SET}	**ICL7663A, ICL7663, 0°C ≤ T_A ≤ +70°C**		**0.01**	**10**	**nA**
		ICL7663B, T_A = 25°C		0.01	10	nA
Shutdown Input Current	I_{SHDN}			±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN}HI: Both V_{OUT} Disabled	1.4			V
		V_{SHDN}LO: Both V_{OUT} Enabled			0.3	V
Sense Pin Input Current	I_{SENSE}			0.01	10	nA
Sense Pin Input Threshold	V_{CL}			0.5		V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	**ICL7663A, ICL7663**				
		V_{IN}^+ = 2V, I_{OUT1} = 1mA		**200**	**500**	**Ω**
		V_{IN}^+ = 9V, I_{OUT1} = 2mA		**70**	**150**	**Ω**
		V_{IN}^+ = 15V, I_{OUT1} = 5mA		**50**	**100**	**Ω**
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	**ICL7663A, ICL7663**				
		1mA ≤ I_{OUT2} ≤ 20mA		**1**	**5**	**Ω**
		50µA ≤ I_{OUT1} ≤ 5mA		**2**	**10**	**Ω**
Available Output Current (V_{OUT2})	I_{OUT2}	3V ≤ V_{IN} ≤ 16, V_{IN} − V_{OUT2} = 1.5V	40			mA
Negative-Tempco Output (Note 4)	V_{TC}	Open-Circuit Voltage		0.9		V
	I_{TC}	Maximum Sink Current	0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		+2.5		mV/°C
Minimum Load Current	$I_{L(min)}$	**(Includes V_{SET} Divider) T_A = 25°C**			**1.0**	**µA**
		0°C ≤ T_A ≤ +70°C		**0.2**	**5**	**µA**

Note 1: Connecting any terminal to voltages greater than (V_{IN}^+ + 0.3V) or less than (GND − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663 power-up.

Note 2: Derate linearly above 50°C at 5mW/°C for plastic minidip, 7.5mW/°C for TO-99 can, and 10mW/°C for CERDIP.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

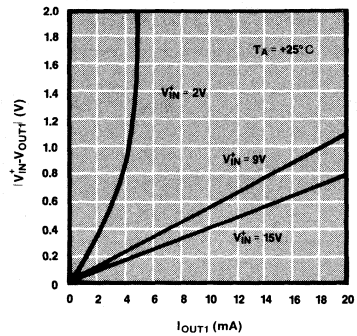
Note 4: This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.

Note 5: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)

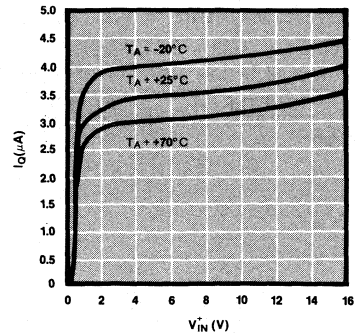
Programmable Positive Voltage Regulator

Typical Operating Characteristics

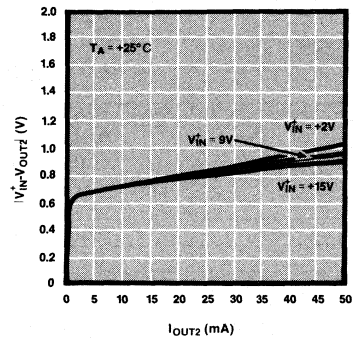
V_{OUT1} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



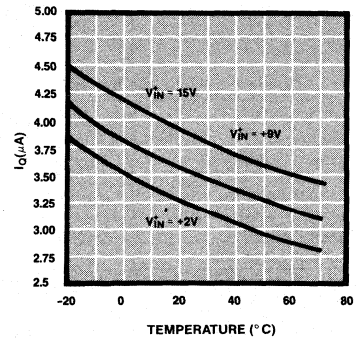
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



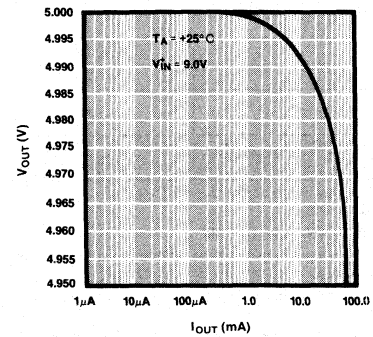
V_{OUT2} INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



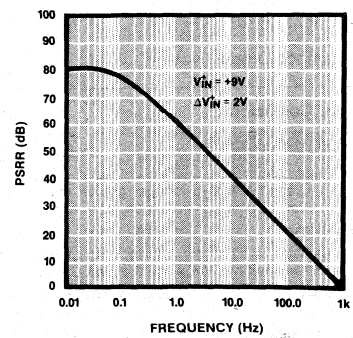
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



INPUT POWER SUPPLY REJECTION RATIO



Programmable Positive Voltage Regulator

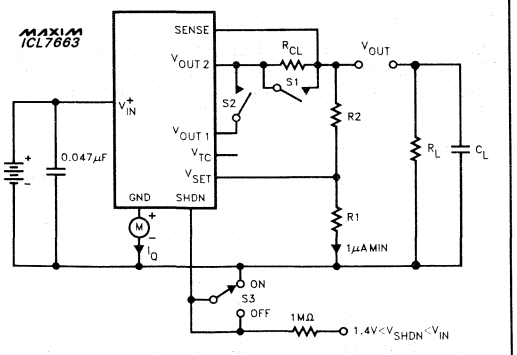
Detailed Description

Block Diagram

As shown in the block diagram of Figure 2, the main elements of the ICL7663 are a micropower bandgap reference, an error amplifier, and an output driver with both FET and NPN bipolar transistors.

The bandgap reference of the Maxim ICL7663A, which uses less than 1μA of quiescent current, is precisely trimmed to 1.29V ± 15mV. The output of the bandgap reference and the input voltage at the V_{SET} terminal are compared in Amplifier A. This output drives the series pass FET output driver which is connected to V_{OUT1}. This output, suitable for output currents less than 5mA, can drive low current loads with a input-to-output voltage differential that approaches 0V with low current loads. The minimum input-to-output differential voltage is the product of the output current and the output saturation resistance. For higher current loads, use the V_{OUT2} pin. The V_{OUT2} pin is driven by an on-chip NPN bipolar transistor whose base is internally connected to the V_{OUT1} output. The NPN bipolar transistor of the Maxim ICL7663 can drive up to 40mA loads with a guaranteed input-to-output differential of 1.5V maximum.

Also onboard the ICL7663 is a sense comparator that will current limit the output when the voltage across the current sense resistor, R_{CL}, is greater than approximately 0.5V; a logic shutdown input that turns off the output by logic level control; and an auxiliary output, V_{TC}, that has a positive temperature coefficient. Using it in combination with the inverting input of Amplifier A, a negative coefficient results in the output voltage.



Note 1: S_1 when closed disables output current limiting

Note 2: Close S_2 for V_{OUT1}, open S_2 for V_{OUT2}

Note 3: $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$

Note 4: I_Q quiescent current is measured at GND pin by meter M

Note 5: S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}

Figure 1. Maxim ICL7663 Test Circuit.

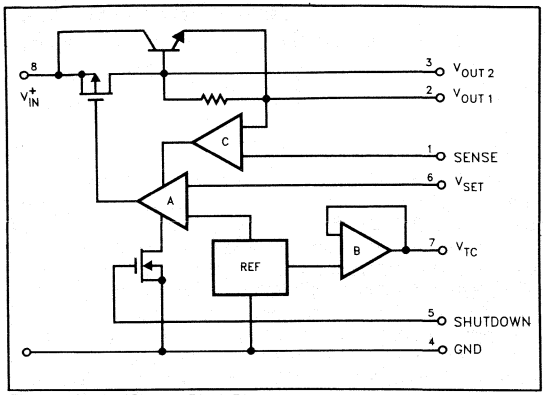


Figure 2. Maxim ICL7663 Block Diagram.

Basic Circuit Operation

Figure 3 shows a typical positive voltage regulator using the ICL7663. The input voltage, V_{IN}^{+} can range from a maximum of 16V to a minimum of the output voltage plus the input-output differential. The output voltage is set by the resistors R2 and R1, and the output current limit is set by R_{CL}. The 0.047μF capacitor on the input limits the rate-of-rise during power-up and also removes some of the high frequency noise on the input voltage. In Figure 3, the logic shutdown is not used and is therefore grounded. V_{OUT2} should be connected directly to SENSE if current limiting is not used.

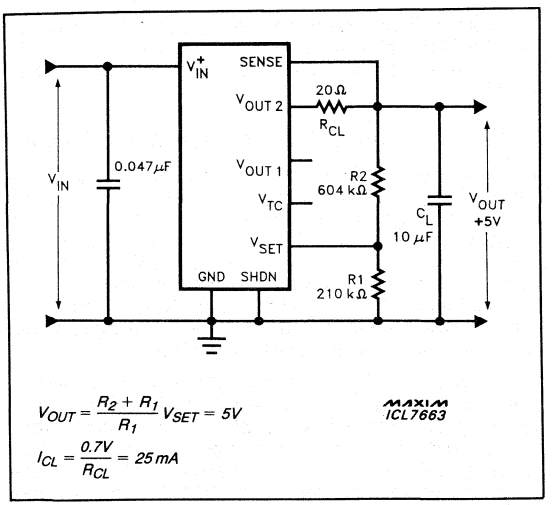


Figure 3. Maxim's Application of ICL7663 (Positive Regulator, Current Limit).

Programmable Positive Voltage Regulator

Output Voltage Selection

The output voltage can be calculated from the formula:

$$V_{OUT} = V_{SET} \times \left(1 + \frac{R_2}{R_1}\right) = V_{SET} \times \left(\frac{R_1 + R_2}{R_1}\right)$$

The Maxim ICL7663A V_{SET} voltage is guaranteed to be 1.29V ± 15mV, eliminating the need for trim pots in most cases. Specifically, using the Maxim ICL7663A and the resistor values shown in Figure 3, the initial voltage will be within ±2.7% of 5V, assuming ±1% tolerance resistors. The output voltage will remain within 5V ± 5%, over 0–70°C. This tolerance includes the effect of ICL7663A V_{SET} error, the ±1% initial tolerance on both resistors, and the resistor ratio temperature coefficient of nearly 200 ppm/°C. Since the resistor ratio temperature coefficient is generally much lower than the absolute temperature coefficient, 100 or 200 ppm resistors can be used, even over the full temperature range while still allowing the output to stay within 4.75V–5.25V.

For 5V supplies that have a looser tolerance, the 5% resistor values of 150kΩ and 430kΩ or 560kΩ and 1.6MΩ are suitable values for R2 and R1. With resistors of ±5% initial tolerance, the initial output voltage will be 5V ± 8.8% and, neglecting the tempco of the resistors, will stay within 5V ± 10% over the entire temperature range.

Current Limiting

The circuit in Figure 3 will limit the output current to approximately 35mA. Current limiting will start, when the output current exceeds 35mA and the voltage drop across the 20Ω R_{CL} is 500mV. For other current limits the value of R_{CL} can be calculated from the formula:

$$R_{CL} = \frac{0.7V}{I_{CL}}; \text{ where } I_{CL} \text{ is the current limit value.}$$

The current limit resistor should be chosen so that neither the 50mA absolute maximum output current specification nor the maximum power dissipation specification is violated.

Input-Output Differential Voltage

The minimum input-output differential voltage (also called dropout voltage) sets the lower limit for the battery voltage in battery powered supplies. The ICL7663 has a dropout voltage of less than one volt. For example, the ICL7663 will continue to supply a regulated 5V output at 40mA until the battery voltage is less than 6.0V. This is significantly better performance than the standard 3 terminal regulators which require a minimum input-output differential of 2–3V to maintain regulation.

As shown in the Typical Characteristics graphs, the minimum input-output differential for the high current output, V_{OUT2}, is relatively independent of output current, varying from 0.6V at low current to about 0.9V at 40mA. This minimum 0.6V input-output differential is caused by the base-emitter voltage drop of the NPN bipolar transistor that drives V_{OUT2}.

By using V_{OUT1} this 0.6V minimum input-output differential voltage is eliminated, but the required input-output differential rises more rapidly (at the rate set by the output saturation resistance — see Electrical Specifications). Ordinarily, it is advantageous to use V_{OUT1} for output currents less than 5mA, and to use V_{OUT2} for higher currents.

If a current limiting resistor is used, the voltage drop across it at the desired operating current must be added to obtain the minimum input-output differential required.

Output Current Booster

Figure 4 shows a circuit that will supply 5 volts at 1 ampere, with a 6.5V input. The high power external series pass NPN transistor is connected in parallel with the internal NPN transistor. The 100Ω resistor in series with V_{OUT2} keeps the current supplied by the ICL7663, and therefore the power dissipation, within the absolute maximum ratings.

This circuit is particularly useful for battery powered systems that alternately draw high current, then shutdown to extend the battery life.

Logic Level Shutdown

The ability to turn off the output of the ICL7663 using a single logic level pin is useful in systems where the equipment is on intermittently. By shutting down the output, the total battery drain is reduced to only the quiescent current of the ICL7663, typically 4μA. The shutdown input should preferably be driven by CMOS logic since the input logic low level is only 0.3V. An alternate way of driving is with an open collector PNP transistor and a resistive pulldown. The pulldown resistor need only draw a fraction of a microamp since the Shutdown terminal input current is less than 10nA.

Figure 4 shows a system that will supply up to 1 ampere of output current when active, but will shutdown to 4μA quiescent current by merely switching the Shutdown pin to the high state.

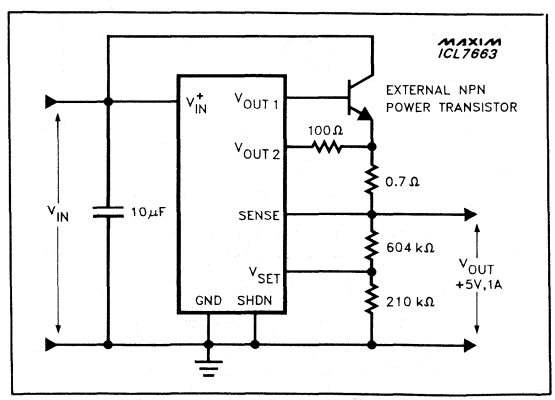


Figure 4. Boosting Output Current with External Transistor.

Programmable Positive Voltage Regulator

Negative Temperature Coefficient Output

The V_{TC} pin has a positive temperature coefficient of about +2.5mV. When connected via a resistor to the inverting summing junction of the error amplifier (the V_{SET} terminal), this positive coefficient results in a controllable negative temperature coefficient at the output of the ICL7663. Figure 5 shows a simplified diagram of the ICL7663 and the pertinent equations for setting both the output voltage and the output tempco.

Negative output temperature coefficients are most commonly used in multiplexed LCD modules or dislay systems to compensate for the negative temperature coefficient of the LCD threshold. Figure 6 shows an ICL7663 generating a temperature compensated V_{DIS} for the Maxim ICM7233 triplexed LCD display driver.

Cautions

The ICL7663 is designed for low quiescent current battery powered systems and has limited line and load regulation at frequencies above 10Hz. The high frequency load and line regulation is easily improved by adding an output filter capacitor across the load.

As with all junction isolated CMOS devices, the ICL7663 can be destroyed by SCR latchup if standard precautions are not observed. First, no pins should ever be driven more than 0.3V below ground or more than 0.3V above V_{IN}^+. Secondly, the rate-of-rise on V_{IN}^+ should not be excessive. The rate-of-rise can be several hundred volts per microsecond if the V_{IN}^+ source has a low internal impedance (such as Nicad or lead-acid batteries). There is no current limiting resistance or inductance between the battery and the ICL7663, and there is no input filtering.

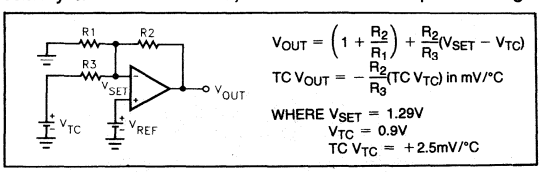


Figure 5. Maxim's Generation of Negative Temperature Coefficients.

Carbon-zinc or alkaline batteries normally do not have sufficient current output capability to cause a rate-of-rise SCR, but the simple addition of a 0.1μF or greater bypass capacitor on the input will ensure that these batteries will not cause SCR latchup.

±5V Power Supply Using One 9V Battery

The ICL7660 inverts the +9V input voltage to −9V which is then regulated by the ICL7664 negative regulator to a constant −5V output (Refer to Figure 7). The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA. The external oscillator capacitor reduces the oscillation frequency of the ICL7660. This allows the battery voltage to be inverted more efficiently.

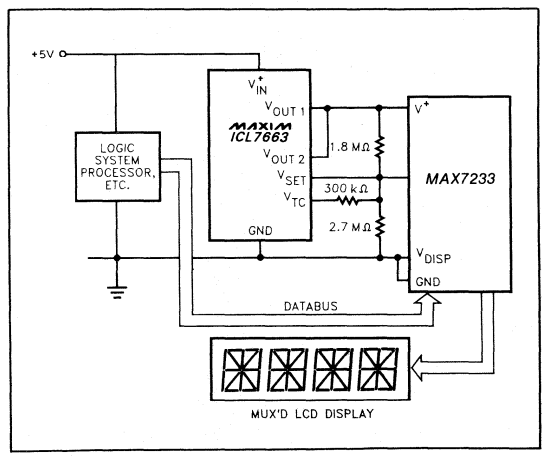


Figure 6. Driving a Multiplexed LCD Display. Consistent operation over more than 40°C temperature span, as opposed to about 10°C with a fixed drive voltage, is allowed by negative temperature coefficient drive voltage to the displays. Based on EPSON LDB-728 Display or equivalent.

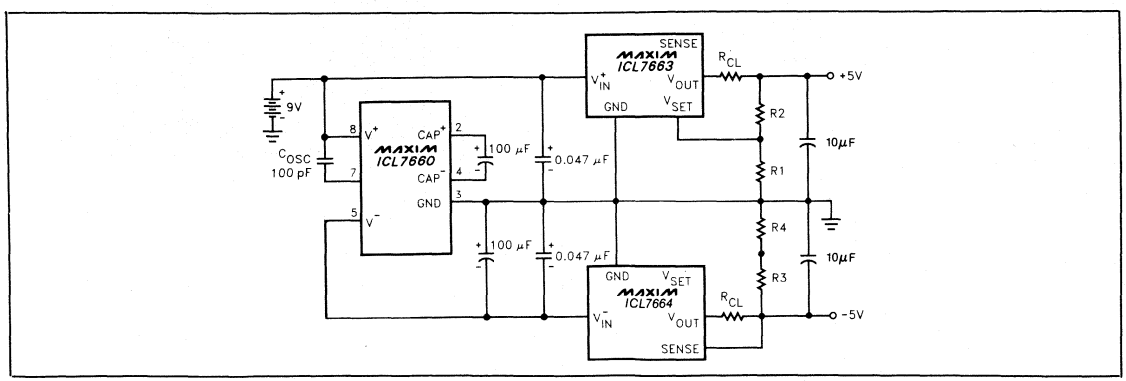
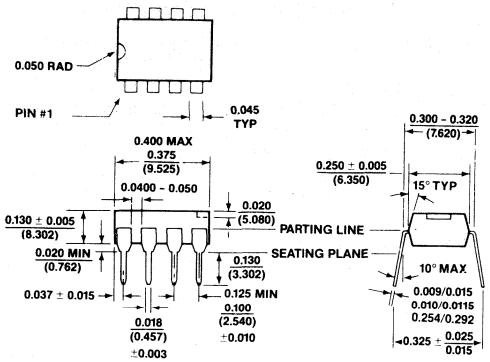


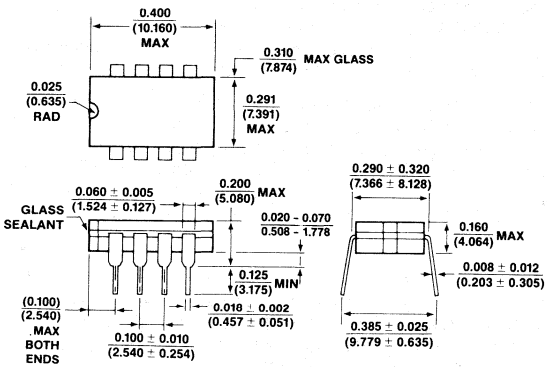
Figure 7. ±5V power supply using one 9V battery.

Programmable Positive Voltage Regulator

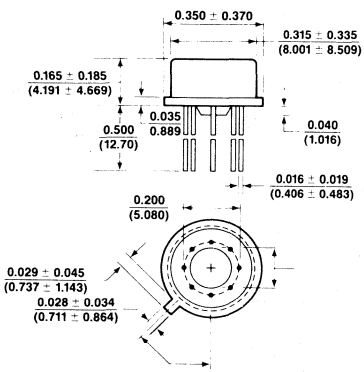
Package Information



8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W

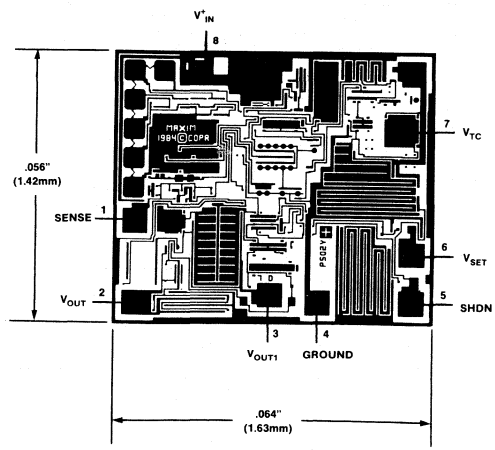


8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

Chip Topography



MAXIM
Programmable Negative Voltage Regulator

General Description

The ICL7664 is a high efficiency negative voltage regulator with a quiescent current of less than 10μA. The output voltage is set by two external resistors to any voltage in the -1.3V to -16V range, with an input voltage range of -2V to -16V. The ICL7664 is well suited for battery powered supplies, with a 10μA quiescent current, an output current capability of 25mA, low V_{IN} to V_{OUT} differential, current limiting, and a logic input level shutdown control.

The Maxim ICL7664 is compatible with existing ICL7664 designs when used with an output filter capacitor of 10μF or greater.

The ICL7664A is an enhanced version of the ICL7664, with a 1% accurate voltage reference, which eliminates the need for trimming the output voltage in most applications.

Applications

Designed specifically for battery powered systems, the ICL7664 negative voltage regulator excels wherever low quiescent power, wide voltage range operation, medium output current levels, current limiting, and logic-controlled shutdown is desired.

Handheld Instruments
LCD Display Modules and Systems
Pagers
Remote Data Loggers

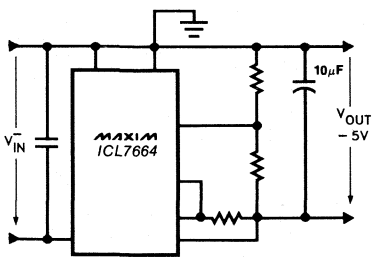
Features

- **1% Output Voltage Accuracy (ICL7664A)**
- **-2V to -16V Operating Range**
- **25mA Output Current, with Current Limiting**
- **Adjustable Output Voltage**
- **Low Input-to-Output Voltage Drop**
- **Low Power CMOS: 4μA Quiescent Current**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7664C/D	0°C to +70°C	Dice
ICL7664CPA	0°C to +70°C	8 Lead Plastic DIP
ICL7664AC/D	0°C to +70°C	Dice
ICL7664ACPA	0°C to +70°C	8 Lead Plastic DIP

Typical Operating Circuit

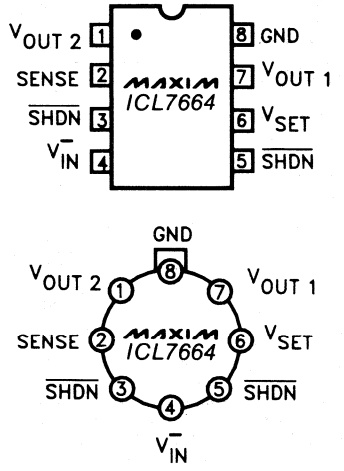


Negative Regulator with Current Limit

(Detailed Circuit Diagram—Figure 3)

Pin Configuration

Top View



Programmable Negative Voltage Regulator

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... -18V
Input or Output Voltage (Note 1) ..... (GND ± 0.3V) to
Terminals (1, 3, 5, 6, 7) (V_{IN} - 0.3V)
Sense Pin ..... (GND + 0.3V) to
(Pin 2) (V_{OUT1} - 0.3V)
Output Sink Current
(Terminals 1, 7) ..... -25mA
Power Dissipation (Note 2)
Minidip 200mW
TO-99 Can 300mW
CERDIP 500mW

Operating Temperature Range
ICL7664C/D ..... 0°C to +70°C
ICL7664CPA ..... 0°C to +70°C
ICL7664IJA ..... -20°C to +85°C
ICL7664ITV ..... -20°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{IN} = -9V, V_{OUT} = -5V, T_A = +25°C, test circuit unless noted

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}	0°C ≤ T_A ≤ +70°C	-2.0		-16.0	V
Quiescent Current	I_Q	R_L = ∞, -1.4V ≤ V_{OUT} ≤ -8.5V V^-_{IN} = -16V, 0°C ≤ T_A ≤ +70°C V^-_{IN} = -9V, 0°C ≤ T_A ≤ +70°C		4.0 3.5	12 10	µA µA
Reference Voltage	V_{SET}	I_{OUT} = 100µA, V_{OUT} = V_{SET} ICL7664A ICL7664	-1.275 -1.2	-1.29 -1.3	-1.305 -1.4	V V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$			±100		ppm/°C
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\Delta V_{IN}}$	-2V ≤ V^-_{IN} ≤ -15V		0.03	0.35	%/V
V_{SET} Input Current	I_{SET}	0°C ≤ T_A ≤ +70°C		±0.01	±10	nA
Shutdown Input Current	$I_{\overline{SHDN}}$	GND ≤ $V_{\overline{SHDN}}$ ≤ V_{IN}		±0.01	±10	nA
Shutdown Input Voltage	$V_{\overline{SHDN}}$	$V_{\overline{SHDN}}$HI: Both V_{OUT} Enabled $V_{\overline{SHDN}}$LO: Both V_{OUT} Disabled	-0.7		 -1.7	V V
Sense Pin Input Current	I_{SENSE}	V_{SENSE} = V_{OUT1}		±0.01	±10	nA
Sense Pin Input Threshold	V_{CL}	V_{CL} = V_{OUT2} - V_{SENSE} (Current-Limit Threshold)		-0.7		V
Input-Output Saturation Resistance (Note 3)	R_{OUT}	V_{OUT1} Connected to V_{OUT2} V^-_{IN} = -2V V^-_{IN} = -9V V^-_{IN} = 15V		 150 40 30	 500 80 60	 Ω Ω Ω
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	ΔI_{OUT} = 100µA		2.0	5.0	Ω
Output Current, V_{OUT1} connected to V_{OUT2}	I_{OUT}	V^-_{IN} = -3V V_{OUT} = V_{SET} V^-_{IN} = -9V V_{OUT} = -5V		-2 -20		mA mA
Minimum Load Current (Includes V_{SET} Divider)	$I_{L(MIN)}$	0°C ≤ T_A ≤ +70°C			1.0	µA

Note 1: Connecting any terminal to voltages greater than (GND + 0.3V) or less than (V^-_{IN} -0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7664 power-up.

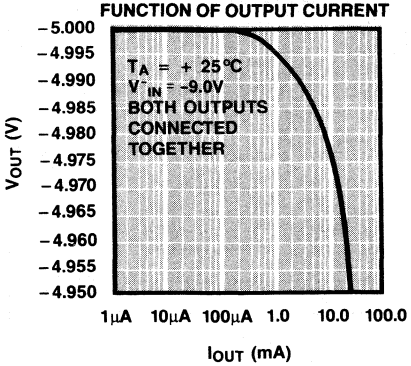
Note 2: Derate linearly above 50°C at 5mW/°C for minidip and 7.5mW/°C for TO-99 can.

Note 3: This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

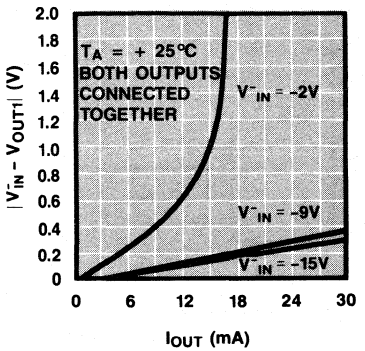
Programmable Negative Voltage Regulator

Typical Operating Characteristics

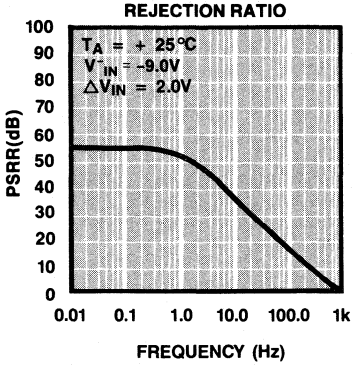
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



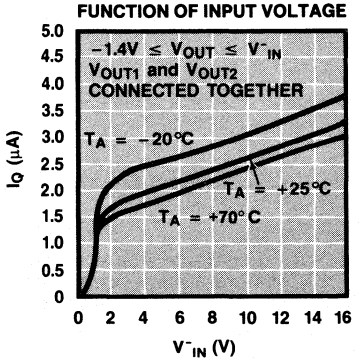
INPUT-OUTPUT DIFFERENTIAL VS OUTPUT CURRENT



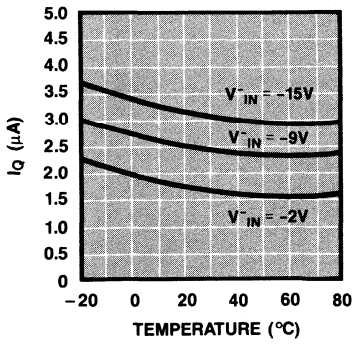
INPUT POWER SUPPLY REJECTION RATIO



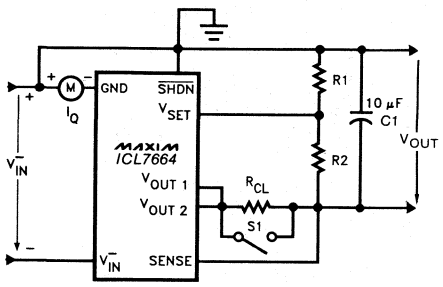
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



Programmable Negative Voltage Regulator



Note 1: Closing S_1 disables current limiting.

Note 2: Quiescent current, I_Q, is measured at the GND pin by meter M.

Note 3: $V_{OUT} = \frac{R_1 + R_2}{R_1} \times V_{SET}$

$$I_{CL} \approx \frac{0.7V}{R_{CL}}$$

Note 4: The value of C1 must be 10µF or greater to ensure stability.

Figure 1. Test Circuit

Detailed Description

Block Diagram

As shown in the block diagram of Figure 2, the main elements of the ICL7664 are a micropower bandgap reference, an error amplifier, and two n channel FET output drivers.

The bandgap reference of the ICL7664A, which uses less than 1µA of quiescent current, is precisely trimmed to 1.29 ± 15mV. The output of the bandgap reference and the input voltage at the V_{SET} terminal are compared in Amplifier A. This output drives the series pass FET output drivers which are connected to V_{OUT1} and V_{OUT2}. These outputs, suitable for output currents of up to 50mA total, can drive low current loads with an input-to-output voltage differential that approaches 0V. The minimum input-to-output voltage increases at the rate of $I_{OUT} \times R_{SAT}$.

Also onboard the ICL7664 is a sense comparator that will current limit the output when the voltage across the current sense resistor, R_{CL}, is greater than approximately 0.7V; and a logic shutdown input that turns off the output by logic level control.

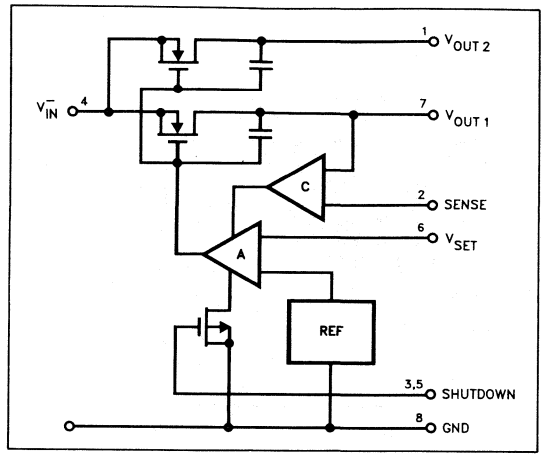


Figure 2. Block Diagram of the ICL7664.

Basic Circuit Operation

Figure 3 shows a typical negative voltage regulator using the ICL7664. The input voltage, V_{IN}, can range from a maximum of -16V to a minimum of the output voltage plus the input-output differential. The output voltage is set by the resistors R2 and R1, and the output current limit is set by R_{CL}. The 0.047µF capacitor on the input is used to limit the rate-of-rise during power-up and also removes some of the high frequency noise on the input voltage. In Figure 3, the logic shutdown is not used and is therefore grounded. V_{OUT1} and V_{OUT2} should be connected directly to SENSE if current limiting is not used.

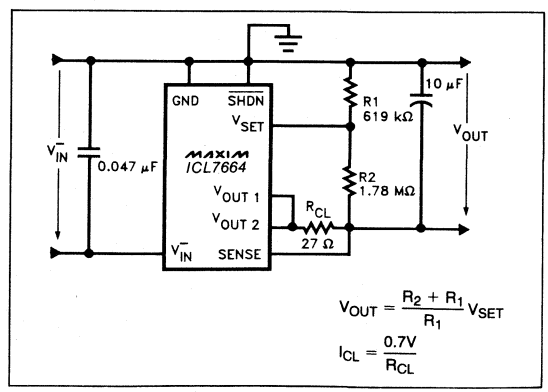


Figure 3. ICL7664 as Negative Regulator with Current Limit

Programmable Negative Voltage Regulator

Output Voltage Selection

The output voltage can be calculated from the formula:

$$V_{OUT} = V_{SET} \times \frac{R1 + R2}{R1}$$

The ICL7664A V_{SET} voltage is guaranteed to be 1.29V ± 15mV at 25°C, eliminating the need for trim pots in most cases. Specifically, using the ICL7664A and the resistor values shown in Figure 3, the initial voltage will be within ±2.7% of 5V, assuming ±1% tolerance resistors. The output voltage will still be within 5V ± 5%, including the ICL7664A effects of the V_{SET} error, the ±1% initial tolerance on both resistors, and the resistor ratio temperature coefficient of nearly 200ppm. Since the resistor ratio temperature coefficient is generally much lower than the absolute temperature coefficient, 100 or 200ppm resistors can be used, even over the full temperature range while still guaranteeing that the output will stay within 4.75V to 5.25V.

For 5V supplies that have a looser tolerance, the 5% resistor values of 1.6MΩ and 560kΩ are suitable values for R2 and R1. With resistors of ±5% initial tolerance, the initial output voltage will be 5V ± 8.7%.

Current Limiting

The circuit in Figure 3 will limit the output current to approximately 25mA. Current limiting will start when the output current exceeds 25mA and the voltage drop across the 27Ω R_{CL} is 700mV. For other current limits the value of R_{CL} can be calculated from the formula:

$$R_{CL} = \frac{0.7V}{I_{CL}}; \text{ where } I_{CL} \text{ is the current limit value.}$$

The current limit resistor should be chosen so that neither the 50mA absolute maximum output current specification (25mA each from V_{OUT1} and V_{OUT2}) nor the maximum power dissipation specification is violated.

The ICL7664 activates current limiting by internally pulling the V_{SET} terminal down towards V_{IN}^-. The main error amplifier then reacts as if the output voltage is greater than the desired output voltage, and shuts off the output. For this current limiting action to work, the parallel resistance of the voltage divider connected to V_{SET} must be greater than 10kΩ.

Input-Output Differential Voltage

The minimum input-output differential voltage (also called dropout voltage) sets the lower limit for usable battery voltage in battery powered supplies. In the ICL7664, the minimum input-output differential voltage is the product of the output current and the ICL7664 output saturation resistance. See the typical characteristics graphs for a plot of input-output differential vs. output current.

Output Current Booster

Figure 4 shows a circuit that will supply -5 volts at 2 amperes, with a 6.5V input. The base of the high power external series pass PNP transistor is driven by V_{OUT1} and V_{OUT2} in parallel. This circuit is useful in circuits where the 50mA maximum output current of the ICL7664 is inadequate, with the only limitation to output current being that the ICL7664 must not supply more than 50mA of base drive to the external PNP transistor. With a beta of 40, the output current would be a maximum of 2 amperes.

This circuit is particularly useful for battery powered systems that alternately draw high current, then shut down to extend the battery life. In the shutdown state, the circuit will draw only the 4μA typical quiescent current of the ICL7664, plus the leakage current of the transistor, which is normally less than 1μA.

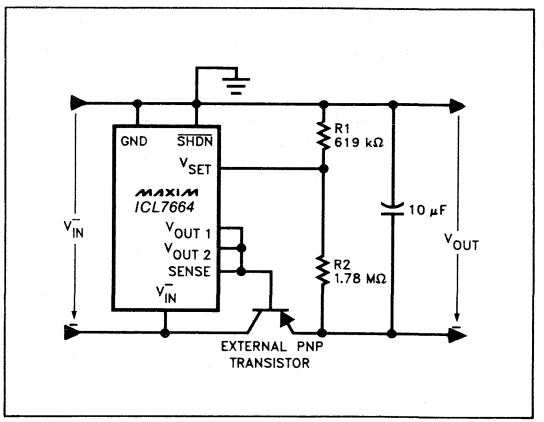


Figure 4. Output Current Boosting

Logic Level Shutdown

The ability to turn off the output of the ICL7664 using a single logic level pin is useful in systems where the equipment is on intermittently. The Shutdown input should preferably be driven by CMOS logic since the input logic high level is only -0.3V. An alternate way of driving is with an open collector PNP transistor and a resistive pullup to ground. The pullup resistor need only draw a fraction of a microamp since the Shutdown terminal input current is less than 10nA.

Figure 4 shows a circuit that will supply up to 2 amperes of output current when active, but will shut down to 4μA quiescent current by merely switching the Shutdown pin to the high state.

Cautions

While the ICL7664 is stable under most conditions, **a 10μF output filter capacitor is required** to ensure stability under all conditions. This output filter capacitor will also improve the high frequency line and load regulation.

As with all junction isolated CMOS devices, the ICL7664 can be destroyed by SCR latchup if standard precautions are not observed. First, no pins should ever

Programmable Negative Voltage Regulator

be driven more than ±0.3V above ground or more than -0.3V below the V_{IN}^-. Secondly, the rate-of-rise on V_{IN}^- should not be excessive. The rate-of-rise can be several hundred volts per microsecond if the V_{IN}^- source has a low internal impedance (such as Nicad or lead-acid batteries). There is no current limiting resistance or inductance between the battery and the ICL7664, and there is no input filtering. Carbon-zinc and alkaline batteries normally do not have sufficient current output capability to cause a rate-of-rise SCR, but the simple addition of a 0.1μF or greater bypass capacitor on the input will ensure that these batteries will not cause SCR latchup.

Figure 5 shows a combined application of the ICL7664, an ICL7663 positive regulator, and the ICL7660 voltage inverter in a ±5V regulated power supply whose power source is a single +9V battery. The ICL7660 inverts the +9V input voltage to -9V which is then regulated by the ICL7664 negative regulator to a constant -5V output. The ICL7663 positive voltage regulator uses the +9V input directly to generate a regulated +5V output. The combined quiescent current of the Maxim ICL7660 and the two regulators is less than 100μA, while the output current capability is 40mA.

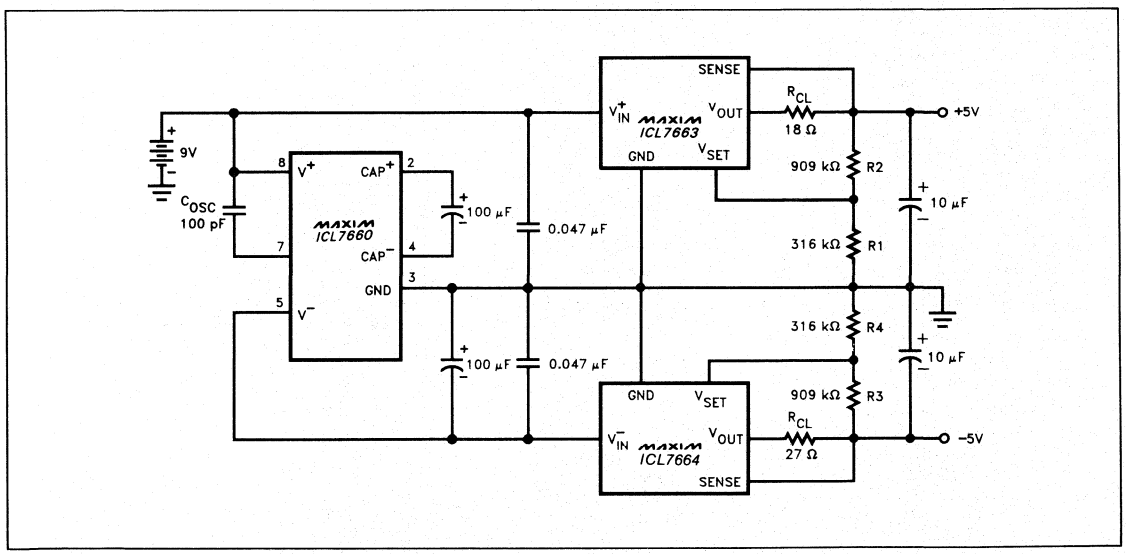
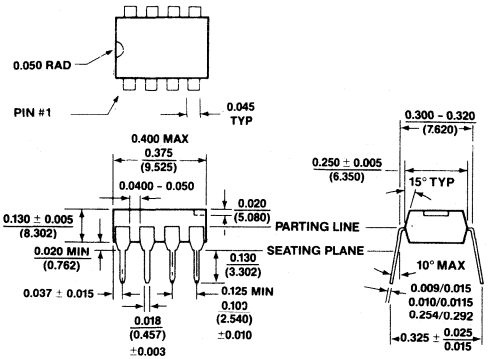


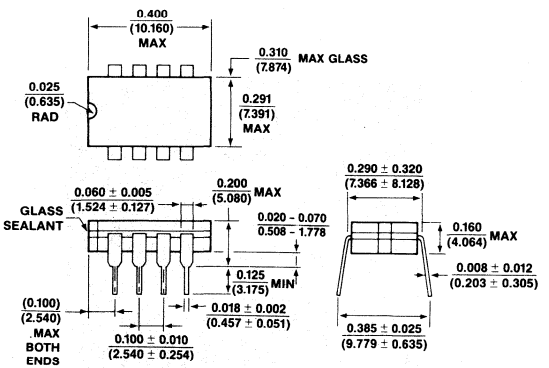
Figure 5. ±5V Power Supply Using One 9V Battery



8 Lead Plastic DIP (PA)

θ_{JA} = 160° C/W

θ_{JC} = 75° C/W



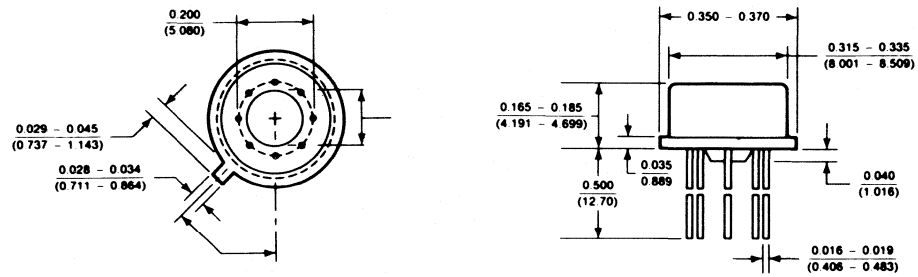
8 Lead CERDIP (JA)

θ_{JA} = 125° C/W

θ_{JC} = 55° C/W

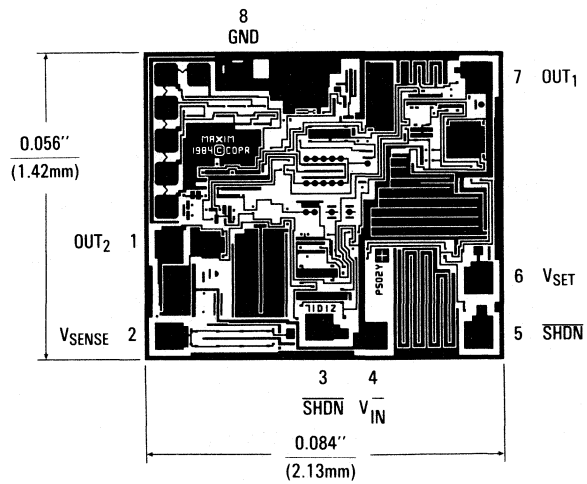
Programmable Negative Voltage Regulator

Package Information



8-Lead TO-99 (TV)
θ_{JA} = 150°C/W, θ_{JC} = 45°C/W

Chip Topography



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

MAXIM

Dual Over/Under Voltage Detector

General Description

The ICL7665 is a low power dual over/under voltage detector drawing a typical operating current of only 3μA. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors to any voltage greater than 1.3V. The ICL7665 will operate from any supply voltage in the 1.6V to 16V range, while monitoring voltages from 1.3V to several hundred volts.

The Maxim ICL7665 and ICL7665B are equivalent to the original manufacturer's parts in both pinout and specification. The Maxim ICL7665A is an improved version with a 2% accurate V_{SET1} threshold and guaranteed performance over temperature. All three versions of the Maxim ICL7665 undergo 100% burn-in and are rigorously tested at temperature extremes to enhance their quality and reliability.

Applications

The 3μA quiescent current of the ICL7665 makes it ideal for voltage monitoring in battery powered systems. In both battery and line-powered systems, the unique combination of a reference, two comparators and hysteresis outputs reduces size and component count of many circuits.

Low Battery Detection
Power Fail and Brownout Detector
Battery Backup Switching
Power Supply Fault Monitoring
Over/Under-Voltage Protection
Hi/Low Temperature, Pressure and Voltage Alarms

Features

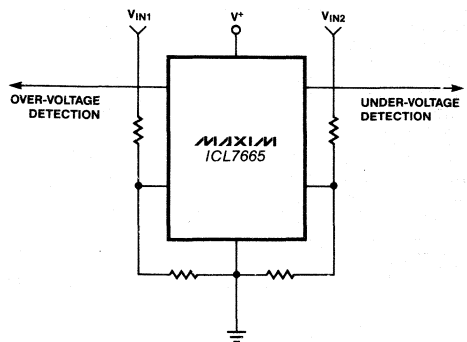
- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Dual Comparator with Precision Internal Reference**
- **3μA Operating Current**
- **2% Threshold Accuracy (ICL7665A)**
- **1.6V to 16V Supply Voltage Range**
- **Onboard Hysteresis Outputs**
- **Trip Points Externally Programmable**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP RANGE	PACKAGE
ICL7665CPA*	0°C to +70°C	8 Lead Plastic Dip
ICL7665CTV*	0°C to +70°C	TO-99 Can
ICL7665CSO*	0°C to +70°C	8 Lead Small Outline
ICL7665C/D*	0°C to +70°C	Dice
ICL7665ACPA	0°C to +70°C	8 Lead Plastic Dip
ICL7665ACTV	0°C to +70°C	TO-99 Can
ICL7665ACSO	0°C to +70°C	8 Lead Small Outline
ICL7665AC/D	0°C to +70°C	Dice

*"B" version also available. Order part number ICL7665B___.

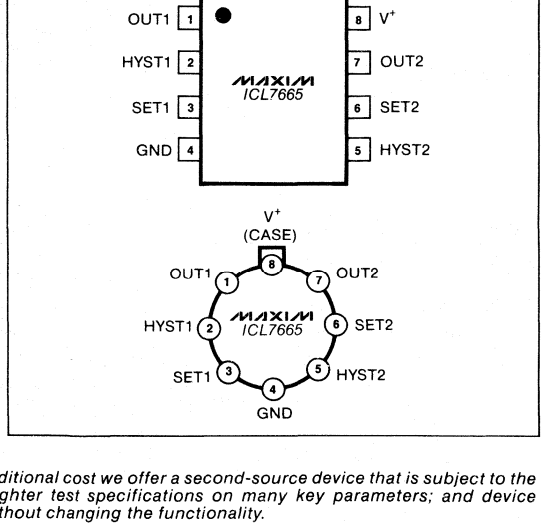
Typical Operating Circuit



SIMPLE THRESHOLD DETECTOR

(Detailed Circuit Diagram — Figure 3)

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... -0.3V to +18V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... -0.3V to +18V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to -18V
Input Voltages SET1 and SET2
(Note 2) ..... (GND - 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA

Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA* ..... 0°C to +70°C
ICL7665BCTV* ..... 0°C to +70°C
ICL7665BCSO* ..... 0°C to +70°C
ICL7665BC/D* ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

*Also applies to "A" version (Maxim).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = +25°C$, test circuit unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	$T_A = +25°C$ $-20°C \le T_A \le +70°C$	1.6 1.8		16.0 16.0	V
Supply Current	I^+	$GND \le V_{SET1}, V_{SET2} \le V^+$ All Outputs Open Circuit $V^+ = 2V$ $V^+ = 9V$ $V^+ = 15V$		 2.5 2.6 2.9	 10 10 15	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	$R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1M\Omega$		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	$V_{SET} = 0V$ or $V_{SET} \ge 2V$		10 -10	200 -100	nA
	I_{OLK} I_{HLK}	$V^+ = 15V$, $T_A = 70°C$ $V^+ = 15V$, $T_A = 70°C$			2000 -500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	$V^+ = 2V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$ $V^+ = 15V$, $V_{SET1} = 2V$, $I_{OUT1} = 2mA$		0.2 0.1 0.06	0.5 0.3 0.2	V
	V_{HYST1} V_{HYST1} V_{HYST1}	$V^+ = 2V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 5V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$ $V^+ = 15V$, $V_{SET1} = 2V$, $I_{HYST1} = -0.5mA$		-0.15 -0.05 -0.02	-0.3 -0.15 -0.10	
	V_{OUT2} V_{OUT2} V_{OUT2}	$V^+ = 2V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 5V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$ $V^+ = 15V$, $V_{SET2} = 0V$, $I_{OUT2} = 2mA$		0.2 0.15 0.11	0.5 0.3 0.25	
	V_{HYST2} V_{HYST2} V_{HYST2}	$V^+ = 2V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.2mA$ $V^+ = 5V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$ $V^+ = 15V$, $V_{SET2} = 2V$, $I_{HYST2} = -0.5mA$		-0.25 -0.43 -0.35	-0.8 -1.0 -0.8	
V_{SET} Input Leakage Current	I_{SET}	$GND \le V_{SET} \le V^+$		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	$R_{OUT} = 4.7k\Omega$, $R_{HYST} = 20k\Omega$ $V_{OUT}LO = 1\% V^+$, $V_{OUT}HI = 99\% V^+$		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	$R_{OUT}, R_{HYST} = 1M\Omega$		±5	±50	
Output/Hysteresis Difference		$R_{OUT}, R_{HYST} = 1M\Omega$		±1		

Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Dual Over/Under Voltage Detector

- ♦ 2% Threshold Accuracy (ICL7665A)
- ♦ Key Specifications Guaranteed over Temperature
- ♦ Improved Temperature Coefficient (ICL7665A)
- ♦ Significantly Improved ESD Protection (Note 1)
- ♦ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: ICL7665 specifications below satisfy or exceed all "tested" parameters on adjacent page. (V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	ICL7665A MIN	ICL7665A TYP	ICL7665A MAX	ICL7665 MIN	ICL7665 TYP	ICL7665 MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C −20°C ≤ T_A ≤ +70°C 0°C ≤ T_A ≤ +70°C	 2.0	 	 16.0	1.6 1.8 	 	16.0 16.0 	V V V
Supply Current	I^+	**GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit 0°C ≤ T_A ≤ +70°C (ICL7665A only) V^+ = 2V V^+ = 9V V^+ = 15V**	 	 **2.5** **2.6** **2.9**	 **10** **10** **15**	 	 2.5 2.6 2.9	 10 10 15	 µA µA µA
Input Trip Voltage	**V_{SET1} V_{SET2}**		**1.275 1.225**	**1.3 1.3**	**1.325 1.375**	1.15 1.2	1.3 1.3	1.45 1.4	V V
Temperature Coefficient of V_{SET}	**$\frac{\Delta V_{SET}}{\Delta T}$**			**100**			200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		.004			.004		%/V
Output Leakage Currents of OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 −10	200 −100		10 −10	200 −100	nA nA
	I_{OLK} I_{HLK}	V^+ = 15V, T_A = 70°C V^+ = 15V, T_A = 70°C			2000 −500			2000 −500	nA nA
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 15V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	 0.3 0.2		0.2 0.1 0.06	0.5 0.3 0.2	V V V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = −0.5mA V^+ = 15V, V_{SET1} = 2V, I_{HYST1} = −0.5mA		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10		−0.15 −0.05 −0.02	−0.3 −0.15 −0.10	V V V
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 15V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.25		0.2 0.15 0.11	0.5 0.3 0.25	V V V
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = −0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = −0.5mA V^+ = 15V, V_{SET2} = 2V, I_{HYST2} = −0.5mA		−0.25 −0.43 −0.35	−0.8 −1.0 −1.0		−0.25 −0.43 −0.35	−0.8 −1.0 −0.8	V V V
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		±0.01	±10		±0.01	±10	nA
ΔV_{SET} Input for Complete Output Change	**ΔV_{SET}**	**R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT} LO = 1% V^+, V_{OUT} HI = 99% V^+**		**0.1**			1.0		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50		±5	±50	mV
Output/Hysteresis Difference		**R_{OUT}, R_{HYST} = 1MΩ**		**±0.1**			±1		mV

Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Dual Over/Under Voltage Detector

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... -0.3V to +12V
Output Voltages OUT1 and OUT2
(with respect to GND) (Note 2) ..... -0.3V to +12V
Output Voltages HYST1 and HYST2
(with respect to V^+) (Note 2) ..... +0.3V to -12V
Input Voltages SET1 and SET2
(Note 2) ..... (GND - 0.3V) to (V^+ + 0.3V)
Maximum Sink Output Current
OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA

Power Dissipation (Note 1) 200mW
Operating Temperature Range
ICL7665BCPA ..... 0°C to +70°C
ICL7665BCTV ..... 0°C to +70°C
ICL7665BCSO ..... 0°C to +70°C
ICL7665BC/D ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature
(Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS, ICL7665B

(V^+ = 5V, T_A = +25°C, test circuit unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V^+	T_A = +25°C 0 ≤ T_A ≤ +70°C	1.6 1.8		10 10	V
Supply Current	I^+	GND ≤ V_{SET1}, V_{SET2} ≤ V^+ All Outputs Open Circuit V^+ = 2V V^+ = 9V		 2.5 2.6	 10 10	µA
Input Trip Voltage	V_{SET1} V_{SET2}		1.15 1.2	1.3 1.3	1.45 1.4	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$			±200		ppm/°C
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{HYST2} = 1MΩ		0.004		%/V
Output Leakage Currents on OUT and HYST	I_{OLK} I_{HLK}	V_{SET} = 0V or V_{SET} ≥ 2V		10 -10	200 -100	nA
	I_{OLK} I_{HLK}	V^+ = 9V, T_A = 70°C V^+ = 9V, T_A = 70°C			2000 -500	
Output Saturation Voltages	V_{OUT1} V_{OUT1} V_{OUT1}	V^+ = 2V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 5V, V_{SET1} = 2V, I_{OUT1} = 2mA V^+ = 9V, V_{SET1} = 2V, I_{OUT1} = 2mA		0.2 0.1 0.06	0.5 0.3 0.25	V
	V_{HYST1} V_{HYST1} V_{HYST1}	V^+ = 2V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 5V, V_{SET1} = 2V, I_{HYST1} = -0.5mA V^+ = 9V, V_{SET1} = 2V, I_{HYST1} = -0.5mA		-0.15 -0.05 -0.02	-0.3 -0.15 -0.15	
	V_{OUT2} V_{OUT2} V_{OUT2}	V^+ = 2V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 5V, V_{SET2} = 0V, I_{OUT2} = 2mA V^+ = 9V, V_{SET2} = 0V, I_{OUT2} = 2mA		0.2 0.15 0.11	0.5 0.3 0.3	
	V_{HYST2} V_{HYST2} V_{HYST2}	V^+ = 2V, V_{SET2} = 2V, I_{HYST2} = -0.2mA V^+ = 5V, V_{SET2} = 2V, I_{HYST2} = -0.5mA V^+ = 9V, V_{SET2} = 2V, I_{HYST2} = -0.5mA		-0.25 -0.43 -0.35	-0.8 -1 -1	
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V^+		0.01	10	nA
ΔV_{SET} Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ V_{OUT}LO = 1% V^+, V_{OUT}HI = 99% V^+		1		mV
Difference in Trip Voltages	V_{SET1}-V_{SET2}	R_{OUT}, R_{HYST} = 1MΩ		±5	±50	
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1MΩ		±1		

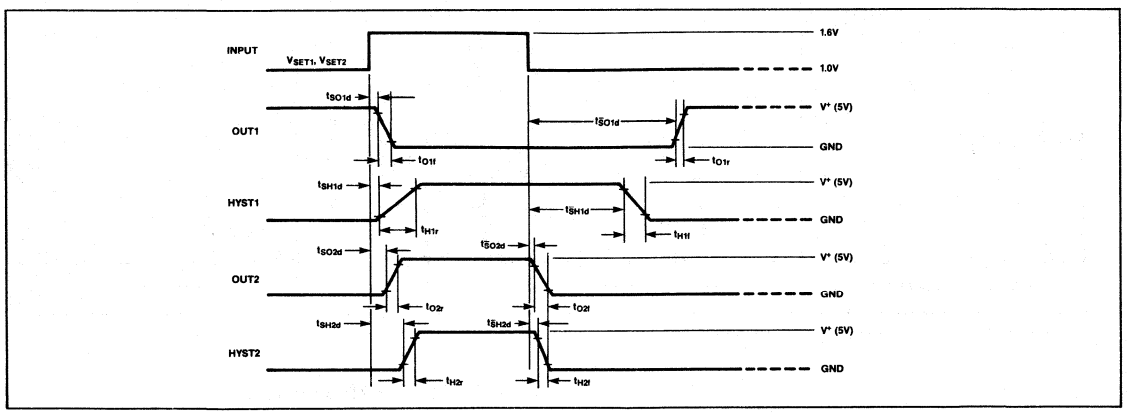
Note 1: Derate above +25°C ambient temperature at 4mW/°C.

Note 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V^+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665 be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.

AC OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Delay Times Input Going HI	t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	V_{SET} Switched from 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		85 90 55 55		µS
Input Going LO	$t_{\overline{SO}1d}$ $t_{\overline{SH}1d}$ $t_{\overline{SO}2d}$ $t_{\overline{SH}2d}$	V_{SET} Switched from 1.6V to 1.0V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		75 80 60 60		µS
Output Rise Times	t_{O1r} t_{O2r} t_{H1r} t_{H2r}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.8 7.5 0.7		µS
Output Fall Times	t_{O1f} t_{O2f} t_{H1f} t_{H2f}	V_{SET} Switched between 1.0V and 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF		0.6 0.7 4 1.8		µS

Switching Waveforms



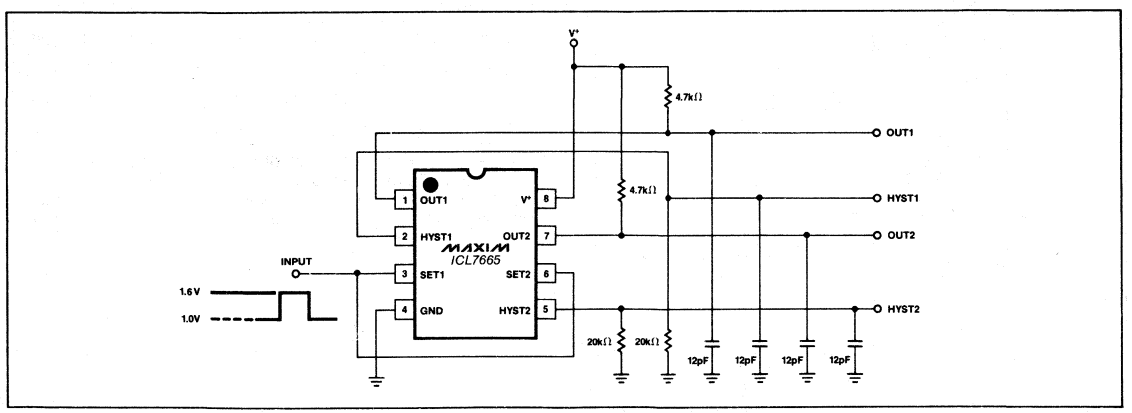
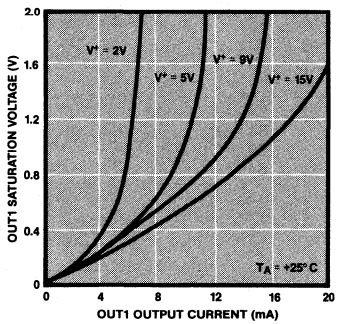


Figure 1. Maxim ICL7665 Test Circuit

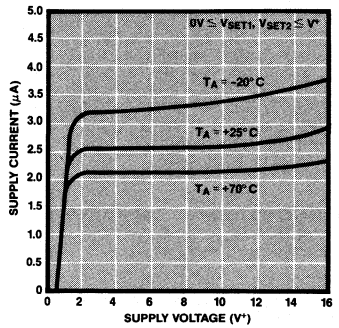
Dual Over/Under Voltage Detector

Typical Operating Characteristics

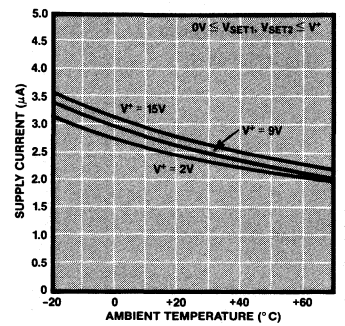
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



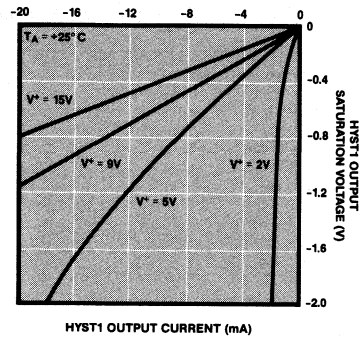
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



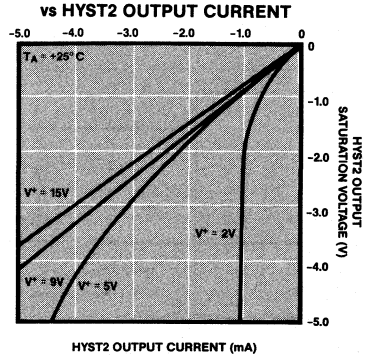
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



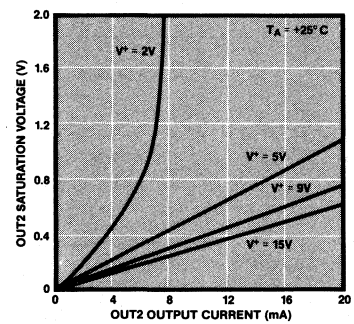
HYST1 OUTPUT SATURATION VOLTAGE vs HYST1 OUTPUT CURRENT



HYST2 OUTPUT SATURATION VOLTAGE vs HYST2 OUTPUT CURRENT



OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



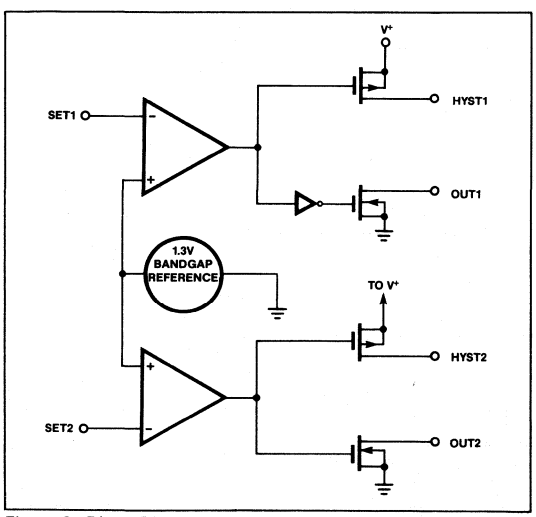


Figure 2. Block Diagram

Table I: ICL7665 TRUTH TABLE

INPUT*	OUTPUT	HYSTERESIS
V_{SET1} > 1.3V	OUT1 = ON = LOW	HYST1 = ON = HI
V_{SET1} < 1.3V	OUT = OFF = HI	HYST1 = OFF = LOW
V_{SET2} > 1.3V	OUT2 = OFF = HI	HYST2 = ON = HI
V_{SET2} < 1.3V	OUT2 = ON = LOW	HYST2 = OFF = LOW

OUT1 is an inverting output, all others are non-inverting.
OUT1 and OUT2 are open drain N-channel current sinks.
HYST1 and HYST2 are open drain P-channel current sources.
*See Electrical Characteristics for exact input threshold range.

Detailed Description

As shown in the block diagram of Figure 2, the Maxim ICL7665 combines a 1.3V reference with two comparators, two open drain n-channel outputs, and two open drain p-channel hysteresis outputs. The reference and comparator are very low power linear CMOS circuits, with a total operating current of 10μA maximum, 3μA typical. The n-channel outputs can sink greater than 10mA but are unable to source any current. These outputs are suitable for wired OR connections and capable of driving TTL inputs when an external pullup resistor is added.

The ICL7665 Truth Table is shown in Table I. OUT1 is an inverting output, all other outputs are non-inverting. HYST1 and HYST2 are p-channel current sources whose sources are connected to V+. OUT1 and OUT2 are n-channel current sinks with their sources connected to ground. Both OUT1 and OUT2 can drive at least one TTL load with a V_{OL} of 0.4V.

In spite of the very low operating current, the ICL7665 has a typical propagation delay of only 75μs. Since the comparator input bias current and the output leakages are very low, high impedance external resistors can be used. This design feature minimizes both the total supply current used and loading on the voltage source that is being monitored.

Basic Over/Under-Voltage Detection Circuits

Figures 3, 4, and 5 show the three basic voltage detection circuits.

The simplest circuit, depicted in Figure 3, does not have any hysteresis. The comparator trip point formulas can easily be derived by observing that the comparator changes state when the V_{SET} input is 1.3V. The external resistors are simply a voltage divider that attenuates the input signal. This ensures that the V_{SET} terminal is at 1.3V when the input voltage is at the desired comparator trip point. Since the bias current of the comparator is only a fraction of a nA the current in the voltage divider can be less than one μA without losing accuracy due to bias currents. The ICL7665A has a 2% threshold accuracy at 25°C and a typical temperature coefficient of 100 ppm/°C including comparator offset drift, eliminating the need for external potentiometers in most applications.

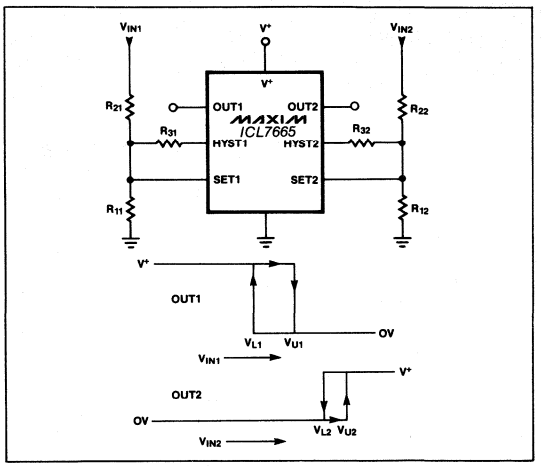


Figure 4. Threshold Detector with Hysteresis

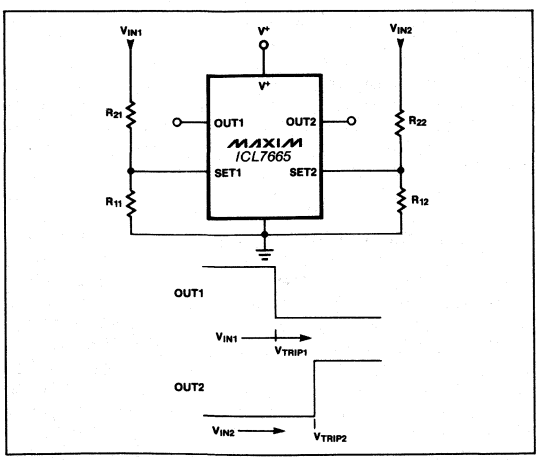


Figure 3. Simple Threshold Detector

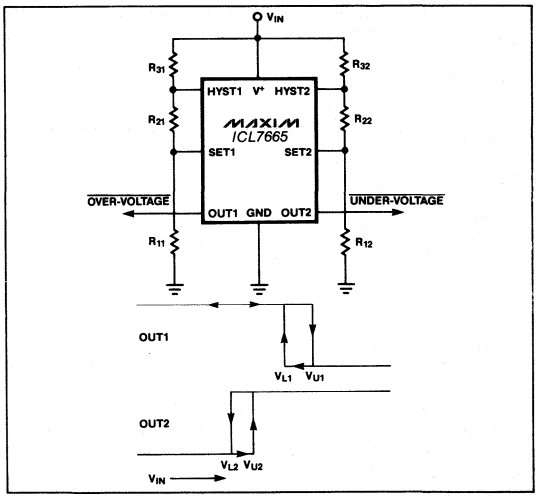


Figure 5. Threshold Detector, $V_{IN} = V^+$

Dual Over/Under Voltage Detector

Figure 4 adds another resistor to each voltage detector. This third resistor supplies current from the HYST output whenever the V_{SET} input is above the 1.3V threshold. As the formulas show, this hysteresis resistor affects only the lower trip point. Hysteresis (defined as the difference between the upper and lower trip points) keeps noise or small variations in the input signal from repeatedly switching the output when the input signal remains near the trip point for a long period of time.

The third basic circuit (Figure 5), is suitable only when the voltage to be detected is also the power supply voltage for the ICL7665. This circuit has the advantage that all of the current flowing through the input divider resistors flows through the hysteresis resistor. This allows the use of higher value resistors without hysteresis output leakage having an appreciable effect on the trip point.

Resistor Value Calculations

Figure 3

1) First choose a value for R11. The value of R11 determines the amount of current flowing through the input divider, equal to $V_{SET}/R11$. R11 can typically be in the range of 10kΩ to 10MΩ.

2) Choose R21 based on the previously chosen R11 and the desired trip point.

$$R21 = R11 \times \frac{V_{TRIP} - V_{SET}}{V_{SET}} = R11 \times \frac{V_{TRIP} - 1.3V}{1.3V}$$

Figure 4

1) Choose a resistor value for R11. Typical values are in the 10kΩ to 10MΩ range.

2) Calculate R21 for the desired upper trip point, V_U using the formula

$$R21 = R11 \times \frac{V_U - V_{SET}}{V_{SET}} = R21 \times \frac{V_U - 1.3V}{1.3V}$$

3) Calculate R31 for the desired amount of hysteresis:

$$R31 = \frac{R21 \times (V^+ - V_{SET})}{V_U - V_L} = \frac{R21 \times (V^+ - 1.3V)}{V_U - V_L}$$

or if $V^+ = V_{IN}$:

$$R31 = \frac{R21 \times (V_L - V_{SET})}{V_U - V_L} = \frac{R21 \times (V_L - 1.3V)}{V_U - V_L}$$

4) The trip voltages are not affected by the absolute value of the resistors as long as the impedances are high enough that the resistance of R31 is much greater than the HYST output's resistance and the current through R31 is much lower than the HYST output's leakage current. Normally R31 will be in the 100kΩ to 22MΩ range. Multiplying or dividing all three resistors by the same factor will not affect the trip voltages.

Figure 5

1) First select a value for R11, usually between 10kΩ and 10MΩ.

2) Calculate R21.

$$R21 = R11 \times \frac{V_L - V_{SET}}{V_{SET}} = R11 \times \frac{V_L - 1.3V}{1.3V}$$

3) Calculate R31

$$R31 = R11 \times \frac{V_U - V_L}{V_{SET}}$$

4) As in the other circuits, all three resistor values may be scaled up or down in value without changing V_U and V_L. V_U and V_L depend only on the ratio of the three resistors if the absolute values are such that the hysteresis output resistance and the leakage currents of the V_{SET} input and hysteresis output can be ignored.

Typical Applications

Fault Monitor for a Single Supply

Figure 6 shows a typical over/under-voltage fault monitor for a single supply. In this case the upper trip points (controlling OUT1) are centered on 5.5V, with 100mV of hysteresis (V_U = 5.55V, V_L = 5.45V); and the lower trip points (controlling OUT2) are centered on 4.5V, also with 100mV of hysteresis. OUT1 and OUT2 are connected together in a wired OR configuration to generate a Power OK signal.

Multiple Supply Fault Monitor

The ICL7665 can simultaneously monitor several power supplies, as shown in Figure 7. The easiest way to calculate the resistor values is to note that when the V_{SET} input is at the trip point (1.3V), the current through R11 is 1.3V/R11. The sum of the currents through R21A, R21B and R31 must equal this current when the two input voltages are at the desired low voltage detection point. Ordinarily R21A and R21B are chosen so that the current through the two resistors is equal. Note that since the voltage at the ICL7665 V_{SET} input depends on the voltage of both supplies being monitored, there will be some interaction between the low voltage trip points for the two supplies. In this example OUT1 will go low when either supply is 10% below nominal (assuming the other supply is at the nominal voltage), or when both supplies are 5% or more below their nominal voltage. R31 sets the hysteresis, in this case, to about 43mV at the 5V supply or 170mV at the 15V supply. The second section of the ICL7665 can be used to detect overvoltage, or as shown in Figure 7, can be used to detect the absence of negative supplies. Note that the trip points for OUT2 depend on both the voltages of the negative power supplies and the actual voltage of the +5V supply.

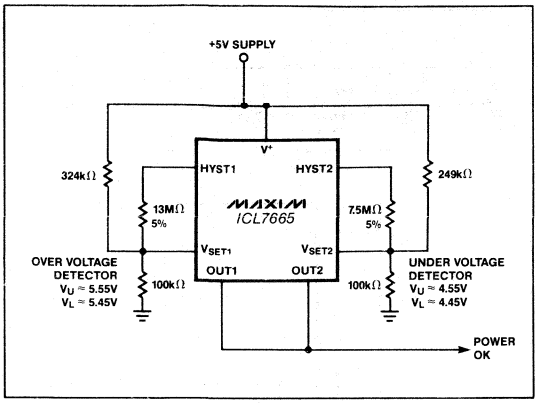


Figure 6. Fault Monitor for a Single Supply

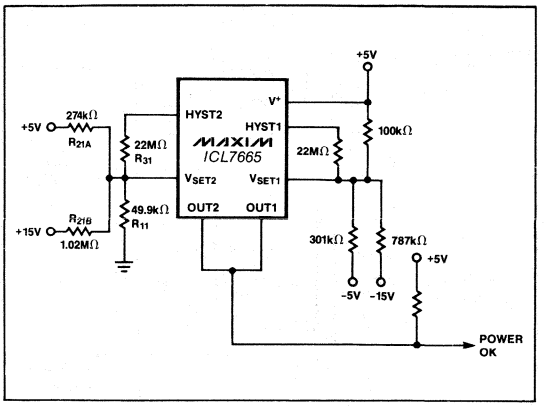


Figure 7. Multiple Supply Fault Monitor

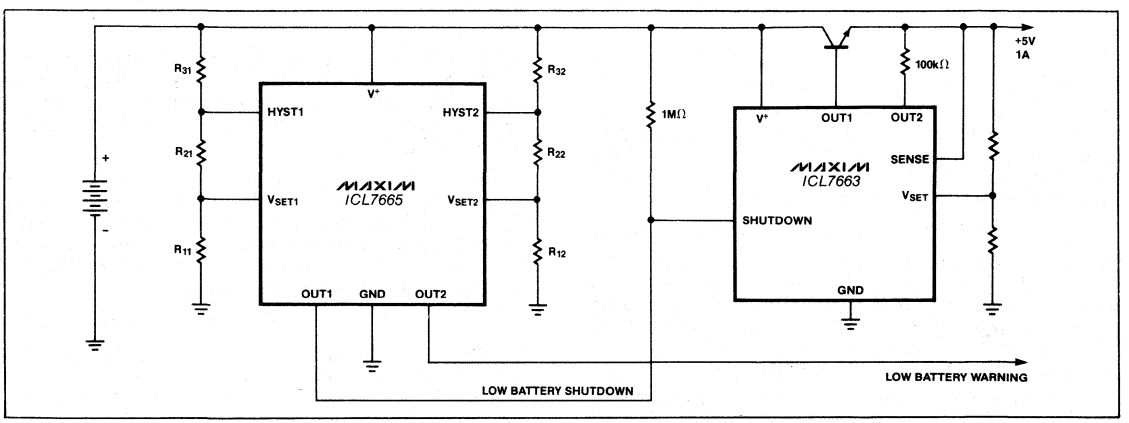


Figure 8. Low Battery Warning and Low Battery Disconnect

Combination Low Battery Warning and Low Battery Disconnect

Nickel Cadmium (NiCad) batteries are excellent rechargeable power sources for portable equipment, but care must be taken to ensure that NiCad batteries are not damaged by overdischarge. Specifically, a NiCad battery should not be discharged to the point where the polarity of lowest capacity cell is reversed and that cell is reverse charged by the higher capacity cells. This reverse charging will dramatically reduce the life of a NiCad battery. Figure 8 both prevents reverse charging and also gives a low battery warning. A typical low battery warning voltage is 1V per cell. Since a NiCad "9V" battery is ordinarily made up of 6 cells with a nominal voltage of 7.2V, a low battery warning of 6V is appropriate, with a small hysteresis of 100mV. To prevent overdischarge of a battery the load should be disconnected when the battery voltage is 1V x (N-1), where N = number of cells. In this case the low battery load disconnect should occur at 5V. Since the battery voltage will rise when the load is disconnected, 800mV of hysteresis is used to prevent repeated on-off cycling.

Power Fail Warning and Powerup/Powerdown Reset

Figure 9 illustrates a power fail warning circuit which monitors raw DC input voltage to the 7805 three terminal 5V regulator. The Power Fail warning signal goes high when the unregulated DC input falls below 8.0V. When the raw DC power source is disconnected or the AC power fails, the voltage on the input of the 7805 decays at a rate of I_{OUT}/C (in this case 200mV/ms). Since the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will give at least 3.5ms of warning before the 5V output begins to drop. If additional warning time is needed,

Dual Over/Under Voltage Detector

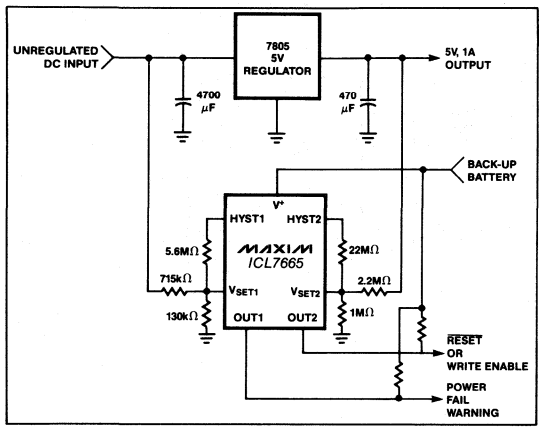


Figure 9. Power Fail Warning and Powerup/Powerdown Reset

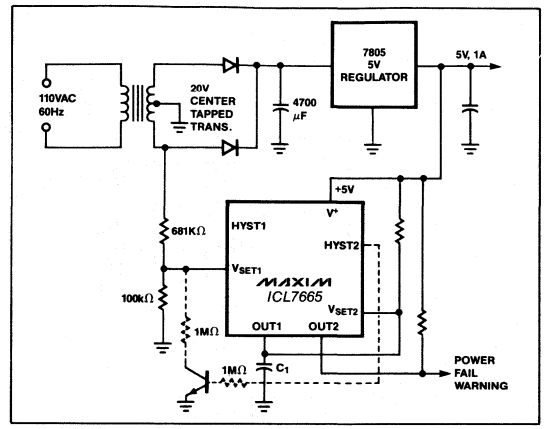


Figure 10. AC Power Fail and Brownout Detector

either the trip voltage or filter capacitance should be increased or the output current should be decreased.

The ICL7665 OUT2 is set to trip when the 5V output has decayed to 3.9V. This output can be used to prevent the microprocessor from writing spurious data to a CMOS battery backup memory, or can be used to activate a battery backup system.

AC Power Fail and Brownout Detector

By monitoring the secondary of the transformer, the circuit in Figure 10 performs the same power failure warning function as Figure 9. With a normal 110VAC input to the transformer, OUT1 will discharge C1 every 16.7ms when the peak transformer secondary voltage exceeds 10.2V. When the 110VAC power line voltage is either interrupted or reduced so that the peak voltage is less than 10.2V, C1 will be charged through R1. OUT2, the Power Fail Warning output, goes high when the voltage on C1 reaches 1.3V. The time constant R1 x C1 determines the delay time before the Power Fail Warning signal is activated, in this case 42ms or 2½ line cycles. Optional components R2, R3 and Q1 add hysteresis by increasing the peak secondary voltage required to discharge C1 once the Power Fail Warning is active.

Battery Switchover Circuit

The circuit in Figure 11 performs two functions: switching the power supply of a CMOS memory to a backup battery when the line-powered supply is turned off, and lighting a low-battery-warning LED when the backup battery is nearly discharged. The PNP transistor, Q1, connects the line-powered +5V to the CMOS memory whenever the line-powered +5V supply voltage is greater than 3.5V. The voltage drop across Q1 will only be a couple of hundred mV since it will be saturated. Whenever the input voltage falls below 3.5V. OUT1 goes high, turns off Q1 and connects the 3V lithium cell to the CMOS memory.

The second voltage detector of the ICL7665 monitors the voltage of the lithium cell. If the battery voltage falls below 2.6V, OUT2 goes low and the low-battery-warning LED turns on (assuming that the +5V is present, of course).

Another possible use for the second section of the ICL7665 is the detection of the input voltage falling below 4.5V. This signal could then be used to prevent the microprocessor from writing spurious data to the CMOS memory while its power supply voltage is outside its guaranteed operating range.

Simple High/Low Temperature Alarm

The circuit in Figure 12 is a simple high/low temperature alarm which uses a low cost NPN transistor as the sensor and an ICL7665 as the high/low detector. The NPN transistor and potentiometer R1 form a Vbe multiplier whose output voltage is determined by the Vbe of the transistor and the position of R1's wiper arm. The voltage at the top of R1 will have a temperature coefficient of approximately -5mV/°C. R1 is set so that the voltage at V_{SET2} is equal to the V_{SET2} trip voltage when the temperature of the NPN transistor reaches the temperature selected for the high temperature alarm desired. R2 can be adjusted so that the voltage at V_{SET1} is 1.3V when the NPN transistor's temperature reaches the low temperature limit.

SCR Latchup

Like all junction isolated CMOS circuits, the ICL7665 has an inherent 4 layer or SCR structure that can be triggered into destructive latchup under certain conditions. Avoid destructive latchup by following these precautions:

1) If either V_{SET} terminal can be driven to a voltage greater than V^+ or less than ground, limit the input current to 500µA maximum. Usually an input voltage

divider resistance can be chosen to ensure the input current remains below 500μA, even when the input voltage is applied before the ICL7665 V+ supply is connected.

2) Limit the rate-of-rise of V+ by using a bypass capacitor near the ICL7665. Rate-of-rise SCRs rarely occur unless: a) the battery has a low impedance — as is the case with NiCad and lead acid batteries; b) the battery is connected directly to the ICL7665 or is switched on via a mechanical switch with low resistance and c) there is little or no input filter capacitance near the ICL7665. In line-powered systems the rate-of-rise is usually limited by other factors and will not cause a rate-of-rise SCR action under normal circumstances.

3) Limit the maximum supply voltage (including transient spikes) to 18V. Likewise limit the maximum voltage on OUT1 and OUT2 to +18V and the maximum voltage on HYST1 and HYST2 to 18V below V+.

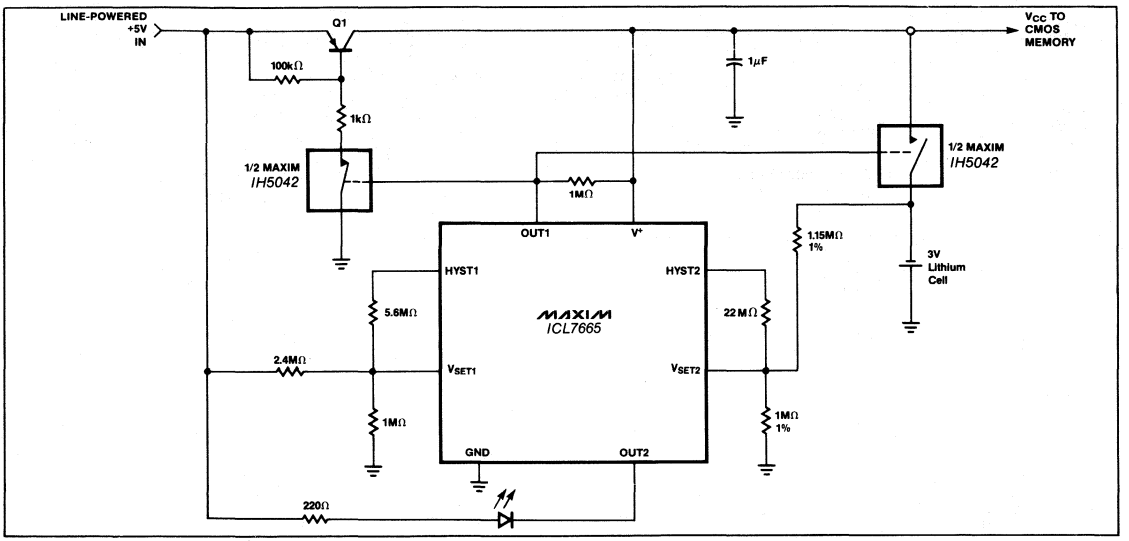


Figure 11. Battery Switchover Circuit

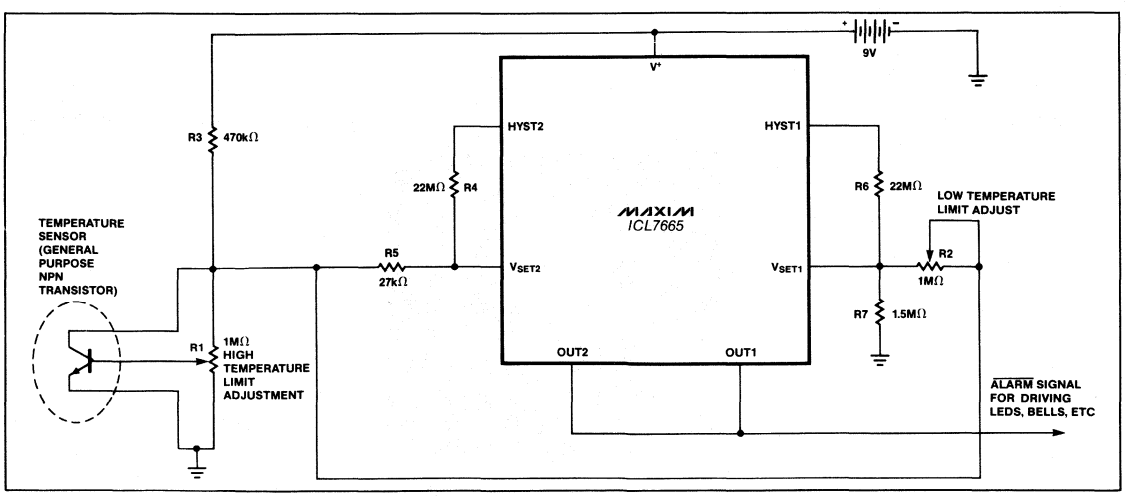
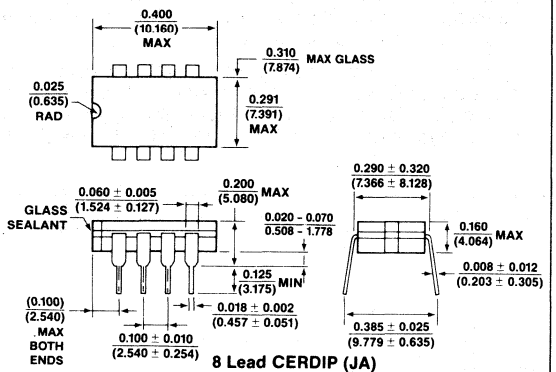


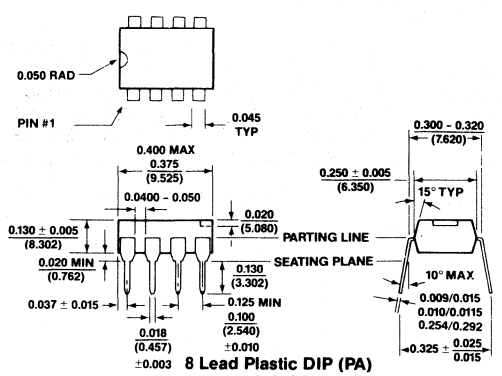
Figure 12. Simple High/Low Temperature Alarm

Dual Over/Under Voltage Detector

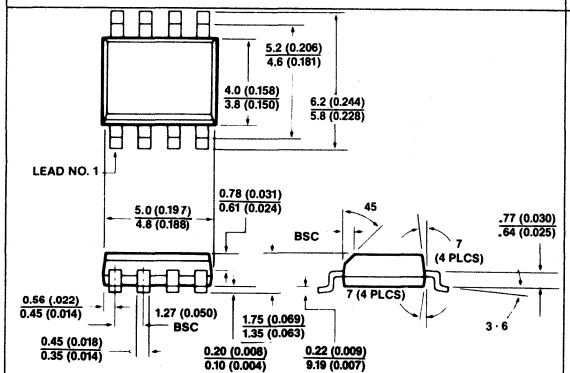
Package Information



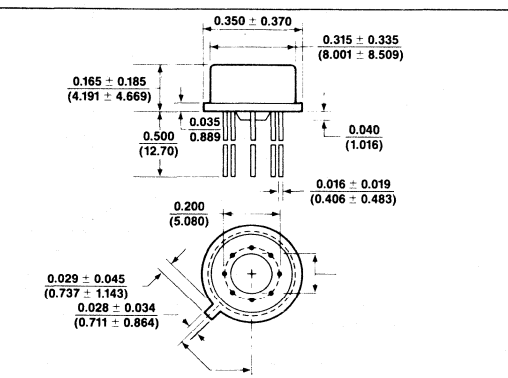
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W

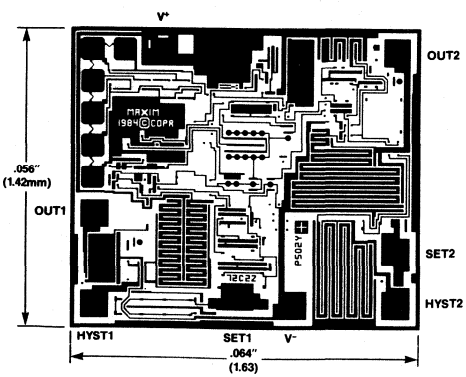


8 Lead Small Outline (SO)
θ_{JA} = 180° C/W
θ_{JC} = 90° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

Chip Topography



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General Purpose Analog Circuits

MAXIM
General Purpose Timers

General Description

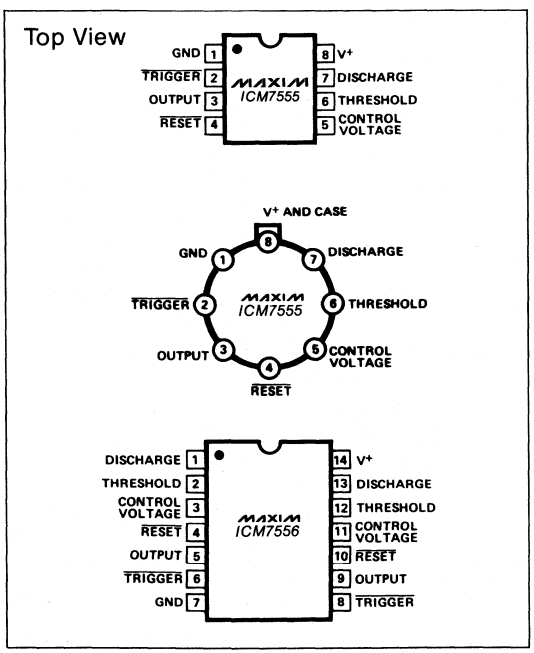
The Maxim ICM7555 and ICM7556 are respectively single and dual general purpose RC timers capable of generating accurate time delays or frequencies. The primary feature is an extremely low supply current, making this device ideal for battery-powered systems. Additional features include low THRESHOLD, TRIGGER, and RESET currents, a wide operating supply voltage range, and improved performance at high frequencies.

These CMOS low-power devices offer significant performance advantages over the standard 555 and 556 bipolar timers. Low-power consumption, combined with the virtually non-existent current spike during output transitions, make these timers the optimal solution in many applications.

Applications

Pulse Generator
Precision Timing
Time Delay Generation
Pulse Width Modulation
Pulse Position Modulation
Sequential Timing
Missing Pulse Detector

Pin Configuration



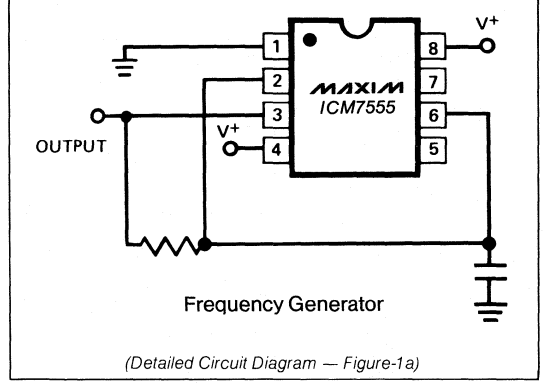
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Wide Supply Voltage Range: 2-18V**
- **No Crowbarring of Supply During Output Transition**
- **Adjustable Duty Cycle**
- **Low THRESHOLD, TRIGGER and RESET Curents**
- **TTL Compatible**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7555IPA	-20°C to +85°C	8 Lead Plastic DIP
ICM7555IJA	-20°C to +85°C	8 Lead CERDIP
ICM7555ITV	-20°C to +85°C	TO-99 Can
ICM7555MJA	-55°C to +125°C	8 Lead CERDIP
ICM7555MTV	-55°C to +125°C	TO-99 Can
ICM7555ISO	-20°C to +85°C	8 Lead Small Outline
ICM7555/D	0°C to +70°C	Dice
ICM7556IPD	-20°C to +85°C	14 Lead Plastic DIP
ICM7556MJD	-55°C to +125°C	14 Lead CERDIP
ICM7556ISO	-20°C to +85°C	14 Lead Small Outline
ICM7556/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram — Figure-1a)

5

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

General Purpose Timers

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... +18 Volts
Input Voltage TRIGGER
Control Voltage THRESHOLD <V+ + 0.3V to ≥ − 0.3V
RESET

Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Operating Temperature Range
ICM7555IJA (Maxim) ..... −20°C to +85°C
ICM7555ISO (Maxim) ..... −20°C to +85°C
ICM7555IPA ..... −20°C to +85°C
ICM7555ITV ..... −20°C to +85°C
ICM7556IPD ..... −20°C to +85°C
ICM7555MTV ..... −55°C to +125°C
ICM7556MJD ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 60 Seconds) ..... +300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +2 to +15 volts; T_A = 25°C, Unless Noted)

PARAMETER	SYMBOL	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	V^+	−20°C ≤ T_A ≤ +70°C			2		18	V
		−55°C ≤ T_A ≤ +125°C			3		16	V
Supply Current[3]	I^+	ICM7555	V^+ = 2V			60	200	µA
			V^+ = 18V			120	300	µA
		ICM7556	V^+ = 2V			120	400	µA
			V^+ = 18V			240	600	µA
Timing Error		R_A, R_B = 1k to 100k, C = 0.1µF	5V ≤ V^+ ≤ 15V					
Initial Accuracy		Note 4				2.0	5.0	%
Drift with Temperature		Note 4	V^+ = 5V			50		ppm/°C
			V^+ = 10V			75		
			V^+ = 15V			100		
Drift with Supply Voltage		V^+ = 5V				1.0	3.0	%/V
Threshold Voltage	V_{TH}		V^+ = 5V		0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}		V^+ = 5V		0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	V^+ = 18V				50		pA
		V^+ = 5V				10		pA
		V^+ = 2V				1		pA
Threshold Current	I_{TH}	V^+ = 18V				50		pA
		V^+ = 5V				10		pA
		V^+ = 2V				1		pA
Reset Current	I_{RST}	V_{RESET} = Ground	V^+ = 18V			100		pA
			V^+ = 5V			20		pA
			V^+ = 2V			2		pA
Reset Voltage	V_{RST}	V^+ = 18V			0.4	0.7	1.0	V
		V^+ = 2V			0.4	0.7	1.0	V
Control Voltage Lead	V_{CV}		V^+ = 5V		0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	V^+ = 18V	I_{SINK} = 3.2mA		0.1	0.4	V
			V^+ = 5V	I_{SINK} = 3.2mA		0.15	0.4	V
		Output Hi	V^+ = 18V	I_{SOURCE} = 1.0mA	17.25	17.8		V
			V^+ = 5V	I_{SOURCE} = 1.0mA	4.0	4.5		V
Rise Time of Output	t_r	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Fall Time of Output	t_f	R_L = 10MΩ	C_L = 10pF	V^+ = 5V	35	40	75	ns
Guaranteed Max Osc Freq	f_{max}	Astable Operation			500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ +0.3V or less than V^- −0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

General Purpose Timers

- **Lower Supply Current**
- **Increased Output Source Current**
- **Guaranteed THRESHOLD, TRIGGER and RESET Input Currents**
- **Guaranteed Discharge Output Voltage**
- **Supply Current Guaranteed Over Temperature**
- **Significantly Improved ESD Protection (Note 6)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

($V^+ = +2$ to $+15$ volts; $T_A = 25°C$, unless noted.)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Voltage	V^+	$-20°C \le T_A \le +85°C$ $-55°C \le T_A \le +125°C$			2 3		18 16	V V
Supply Current (Note 3)	I^+	**ICM 7555**	$V^+ = 2\text{-}18V; T_A = +25°C$ $V^+ = 5V; -20°C \le T_A \le +85°C$ $V^+ = 5V; -55°C \le T_A \le +125°C$			**30**	**120** **250** **300**	**µA** **µA** **µA**
		ICM 7556	$V^+ = 2\text{-}18V; T_A = +25°C$ $V^+ = 5V; -20°C \le T_A \le +85°C$ $V^+ = 5V; -55°C \le T_A \le +125°C$			**60**	**240** **500** **600**	**µA** **µA** **µA**
Timing Error (Note 4)		Circuit of figure 1(b); $R_A = R_B = 100k\Omega$, $C = 0.1\mu F$, $V^+ = 5V$						
Initial Accuracy (Note 5)						2.0	5.0	%
Drift with Temperature		$V^+ = 5V$ $V^+ = 10V$ $V^+ = 15V$				50 75 100		ppm/°C ppm/°C ppm/°C
Drift with Supply Voltage		$V^+ = 5V$				1.0	3.0	%/V
Threshold Voltage	V_{TH}	$V^+ = 5V$			0.63	0.66	0.67	V^+
Trigger Voltage	V_{TRIG}	$V^+ = 5V$			0.29	0.33	0.34	V^+
Trigger Current	I_{TRIG}	**$V^+ = 18V$**				**50**	**500**	**pA**
		$V^+ = 5V$ $V^+ = 2V$				10 1		pA pA
Threshold Current	I_{TH}	**$V^+ = 18V$**				**50**	**500**	**pA**
		$V^+ = 5V$ $V^+ = 2V$				10 1		pA pA
Reset Current	I_{RST}	**V_{RESET} = Ground**	**$V^+ = 18V$**			**100**	**500**	**pA**
			$V^+ = 5V$ $V^+ = 2V$			20 2		pA pA
Reset Voltage	V_{RST}	$V^+ = 18V$ $V^+ = 2V$			0.4 0.4	0.7 0.7	1.0 1.0	V V
Control Voltage	V_{CV}	$V^+ = 5V$			0.62	0.66	0.67	V^+
Output Voltage Drop	V_O	Output Lo	$V^+ = 18V$ $V^+ = 5V$	$I_{SINK} = 3.2mA$ $I_{SINK} = 3.2mA$		0.1 0.15	0.4 0.4	V V
		Output Hi	**$V^+ = 18V$** **$V^+ = 5V$**	**$I_{SOURCE} = 2.0mA$** **$I_{SOURCE} = 2.0mA$**	17.25 4.0	17.8 4.5		V V
Discharge Output Voltage	V_{DIS}	**$V^+ = 5V, I_{DIS} = 3.2mA$**				**0.1**	**0.4**	**V**
Rise Time of Output (Note 4)	t_r	$R_L = 10M\Omega$	$C_L = 10pF$	$V^+ = 5V$	35	40	75	ns
Fall Time of Output (Note 4)	t_f	$R_L = 10M\Omega$	$C_L = 10pF$	$V^+ = 5V$	35	40	75	ns
Guaranteed Max Osc. Freq. (Note 4)	f_{max}	Astable Operation			500			kHz

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V^+ + 0.3V$ or less than $V^- - 0.3V$ may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

Note 2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).

Note 3: The supply current value is essentially independent of the TRIGGER, THRESHOLD AND RESET voltages.

Note 4: Parameter is not 100% tested. Majority of all units meet this specification.

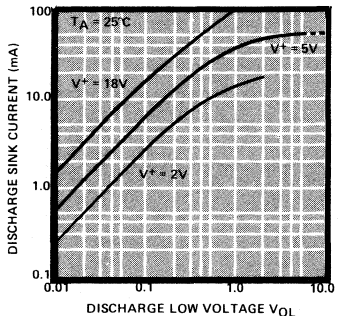
Note 5: Deviation from $f = 1.46/(R_A + 2R_B)C$, $V^+ = 5V$.

Note 6: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Mil Std 883B, Method 3015.1 Test Circuit.)

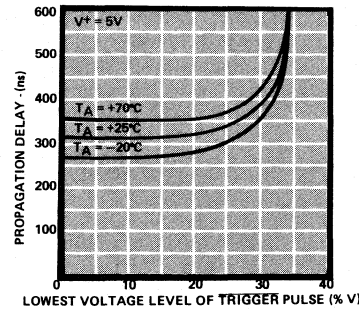
General Purpose Timers

Typical Operating Characteristics

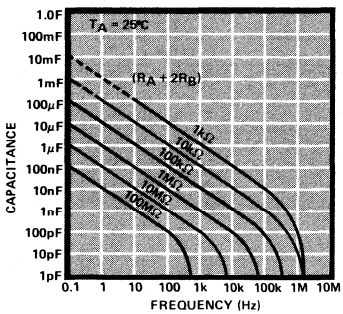
DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



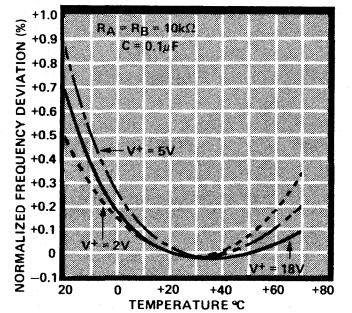
PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE



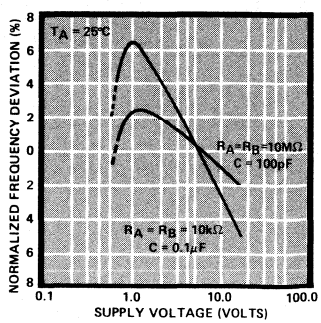
FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B AND C



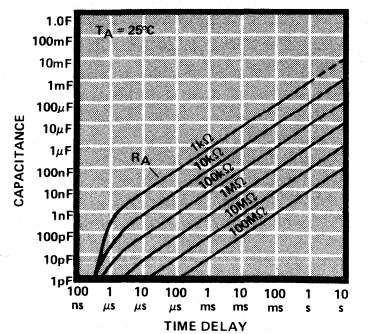
NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

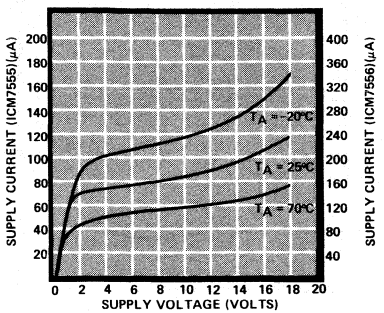


TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C

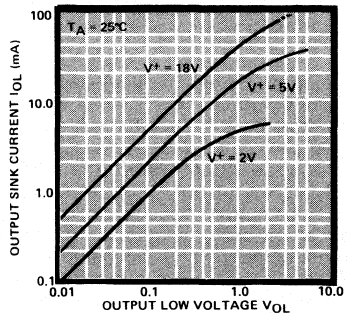


Typical Operating Characteristics

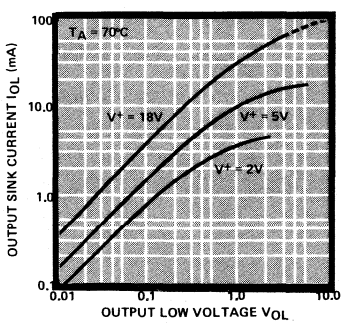
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



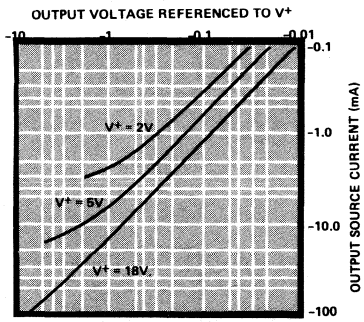
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



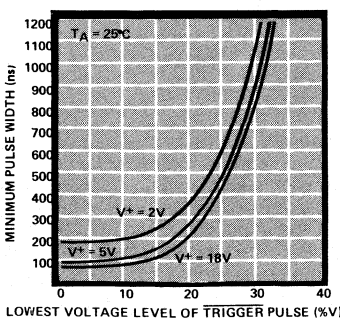
OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



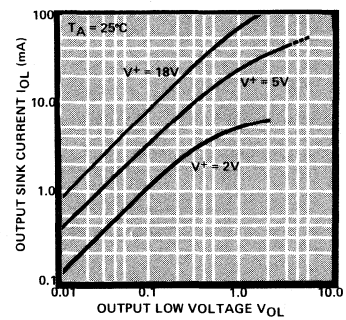
OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



5

General Purpose Timers

Detailed Description

Both the ICM7555 timer and the ICM7556 dual timer can be configured for either astable or monostable operation. In the astable mode the free running frequency and the duty cycle are controlled by two external resistors and one capacitor. Similarly, the pulse width in the monostable mode is precisely controlled by one external resistor and capacitor.

The external component count is decreased when replacing a bipolar timer with the ICM7555 or ICM7556. The bipolar devices produce large crowbar currents in the output driver. To compensate for this spike, a capacitor is used to decouple the power supply lines. The CMOS timers produce supply spikes of only 2-3mA vs. 300-400mA (Bipolar), therefore supply decoupling is typically not needed. This current spike comparison is illustrated in Figure 3. Another component is eliminated at the control voltage pin. These CMOS timers, due to the high impedance inputs of the comparators, do not require decoupling capacitors on the control voltage pin.

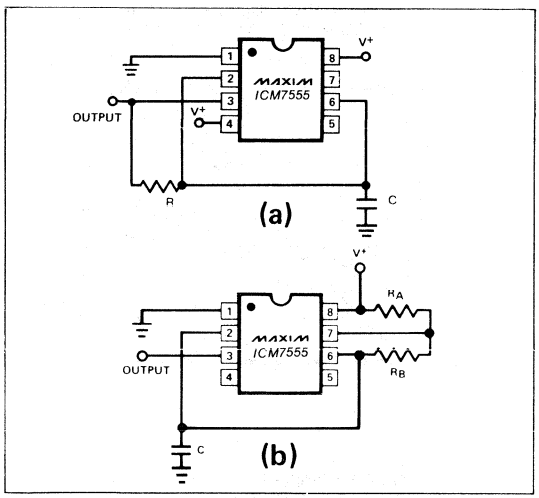


Figure 1. Maxim ICM7555 used in two different astable configurations.

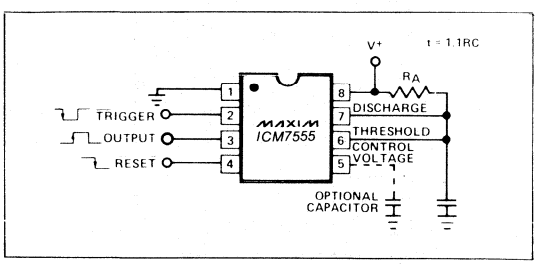


Figure 2. Maxim ICM7555 in a monostable operation.

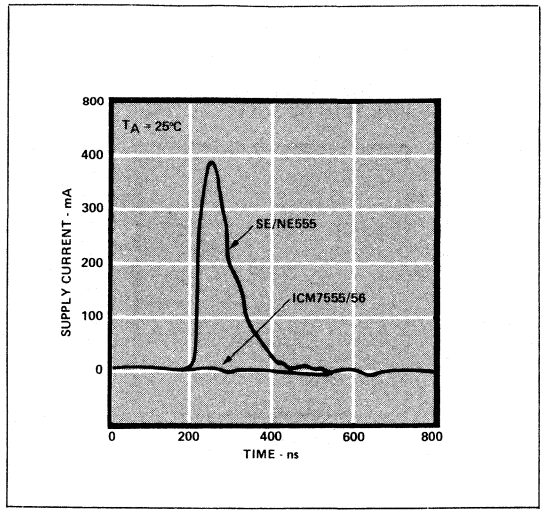


Figure 3. Supply current transient compared with a standard bipolar 555 during an output transition.

Applications Information

Astable Operation

We recommend either of the two astable circuit configurations illustrated in Figure 1. The circuit in (1a) provides a 50% duty cycle output using one timing resistor and capacitor. The oscillator waveform across the capacitor is symmetrical and triangular, swinging from ⅓ to ⅔ of the supply voltage. The frequency generated is defined by:

$$f = \frac{1}{1.4\,RC}$$

The circuit in (1b) provides a means of varying the duty cycle of the oscillator. The frequency is defined by:

$$f = \frac{1.46}{(R_A + 2R_B)C}$$

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

Monostable Operation

The circuit diagram in Figure 2 illustrates monostable operation. In this mode the timer acts as a one shot. Initially the external capacitor is held discharged by the discharge output. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the capacitor begins to charge exponentially through R_A. The device resets after the voltage across the capacitor reaches ⅔(V^+).

$$t_{output} = -\ln(⅓)R_AC = 1.1\,R_AC$$

Reset

The reset function is significantly improved over the standard bipolar 555 and 556 in that it controls only the internal flip-flop, which in turn simultaneously controls the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow-falling edges of the bipolar devices. This input is designed to have essentially the same trip voltage as the standard bipolar devices (0.6 to 0.7V). At all supply voltages this input maintains an extremely high impedance.

Control Voltage

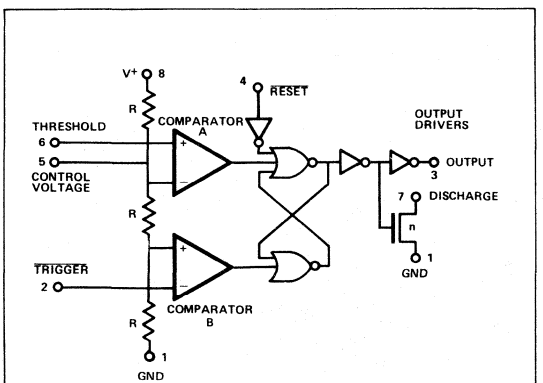
The control voltage regulates the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators. This pin can be used for frequency modulation in the astable mode. By varying the applied voltage to the control voltage pin, delay times can be changed in the monostable mode.

Power Supply Considerations

Since the $\overline{\text{TRIGGER}}$, THRESHOLD and Discharge leakage currents are very low, high impedance timing components may be used, keeping total system supply current at a minimum.

Output Drive Capability

The CMOS output stage is capable of driving most logic families including CMOS and TTL. The ICM7555 and ICM7556 will drive at least two standard TTL loads at a supply voltage of 4.5V or greater. When driving CMOS, the output swing at all supply voltage levels will equal the supply voltage.



This block diagram reduces the circuitry down to its simplest equivalent components.
R = 100kΩ, ±20% typ.

Figure 4. Block diagram of ICM7555.

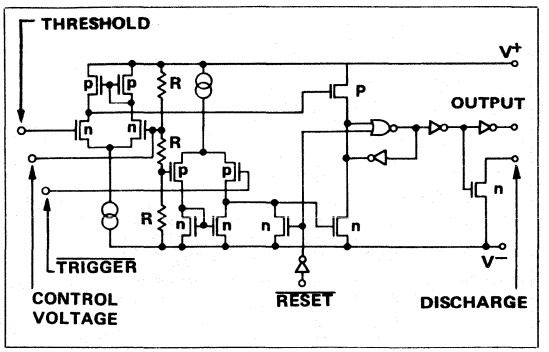


Figure 5. Equivalent circuit.

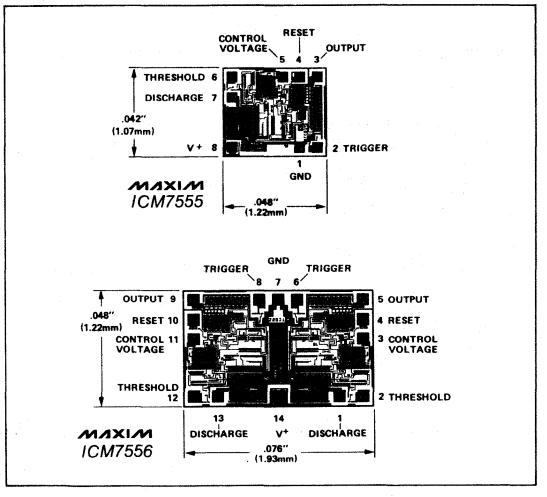
Function Table

RESET	TRIGGER VOLTAGE†	THRESHOLD VOLTAGE†	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	$< \frac{1}{3} V^+$	Irrelevant	High	Off
High	$> \frac{1}{3} V^+$	$> \frac{2}{3} V^+$	Low	On
High	$> \frac{1}{3} V^+$	$< \frac{2}{3} V^+$	As previously established	

†Voltages levels shown are nominal.

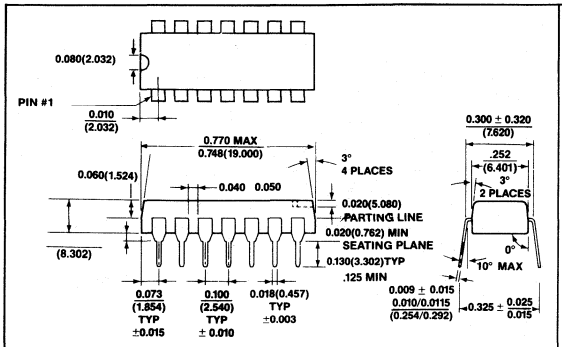
NOTE: $\overline{\text{RESET}}$ will dominate all other inputs. $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Chip Topographies

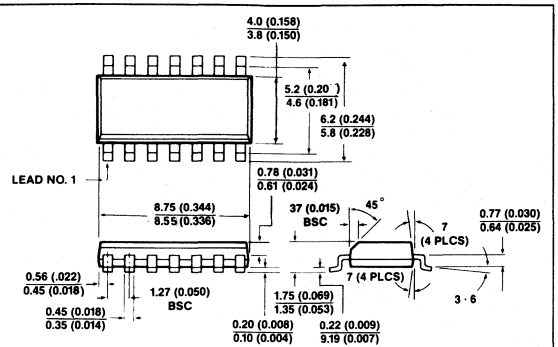


General Purpose Timers

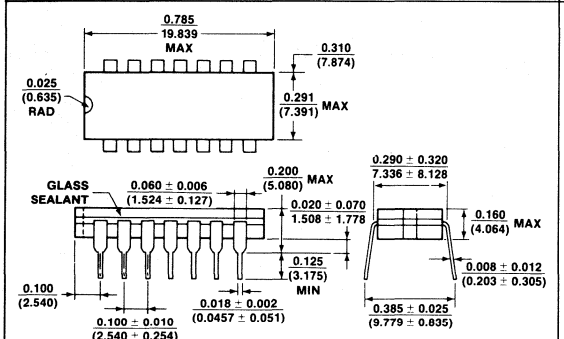
Package Information



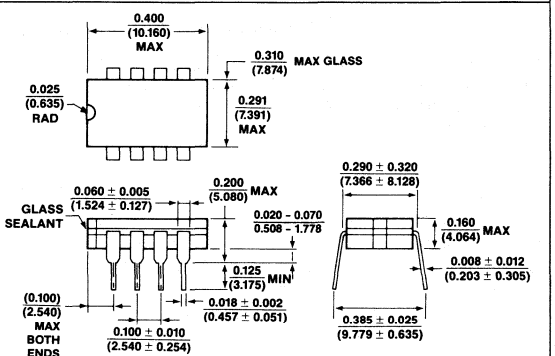
14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W



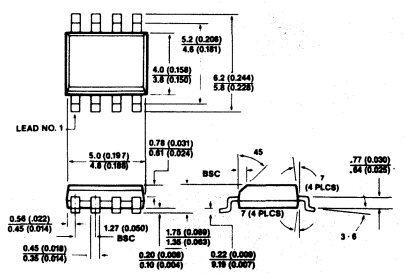
14-Lead Small Outline (SO)



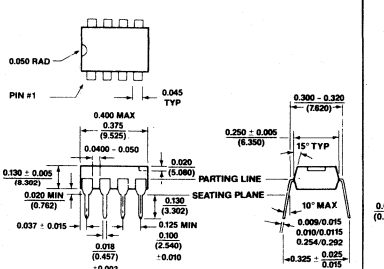
14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W



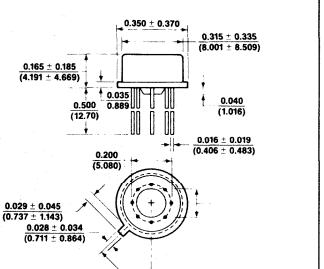
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



8-Lead Small Outline (SO)



8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

MAXIM
Long Range Fixed Timer/Counter

General Description

The Maxim ICM7242 Timer/Counter combines a ÷256 counter with an internal oscillator whose period is controlled by an external resistor and capacitor. This device requires only 120μA of supply current and operates from 2 to 16 volts, making it ideal for battery operated systems.

This device operates in either an astable or monostable configuration, using the onboard control flip-flop with Trigger and Reset inputs. The onboard divider generates much longer time delays than can be produced by a conventional RC Timer. For example, the ICM7242 generates a delay period of over one hour with timing components of 22MΩ and 1.5μF. By cascading two or more ICM7242's even longer time delays can be produced.

Features

- **Pin for Pin Second Source!**
- **Low Supply Current: 120μA**
- **Wide Supply Voltage Range: 2 to 16 Volts**
- **÷2, ÷256 Outputs**
- **Cascadable For Long Range Timing**
- **Monostable or Astable Operation**
- **Low Power CMOS**

Applications

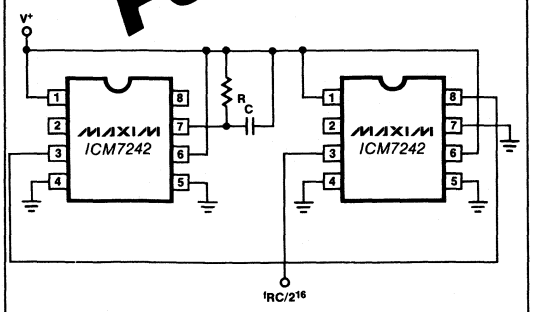
The combination of low operating current, long time delays and cascadability make the ICM7242 well suited for a variety of timing and control applications.

ON/OFF Delay Timers
Cycle Timers
Sequence Timers
Long Delay Time Generators

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7242BA	-20°C to +85°C	8 Lead Plastic DIP
ICM7242IJA	-20°C to +85°C	8 Lead CERDIP
ICM7242C/D	0°C to +70°C	Dice

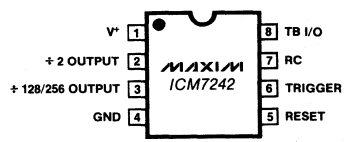
Typical Operating Circuit



Cascading Two ICM7242's to Generate Low Frequency Output

Pin Configuration

Top View



MAXIM
Programmable Timer/Counters

General Description

The Maxim ICM7240/50/60 programmable timer/counter family requires only 120μA of supply current while generating programmable delays from μs to hours. Each device combines a programmable counter with an internal oscillator whose period is controlled by an external resistor and capacitor. For counter/divider applications, the osciilator can be inhibited and an external clock applied to the TB I/O terminal. The counter can be programmed using thumbwheel switches, jumpers, or analog switches.

The ICM7240 has an 8 bit programmable counter and can generate time delays from 1 to 255 RC time constants. The ICM7250 has a two digit programmable BCD counter and can generate time delays from 1 to 99 RC time constants. The ICM7260 is used for "real time" applications and has a modulo 60 programmable divider, producing time delays from 1 to 59 RC time constants. These three devices are easily cascaded and can operate in either astable or monostable configurations, using the on-chip control flip-flop with Trigger and Reset inputs.

Applications

The combination of low operating current, long time delays, programmability and cascadability make the ICM7240/50/60 family well suited for a variety of timing and control applications:

- ON/OFF Delay Timers
- Batch Timer/Sequencers
- Cycle Timers
- Programmable Timers
- Frequency Synthesizers
- Ultra-Long Time Delay Generators

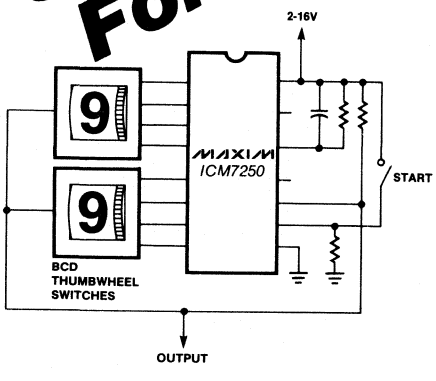
Features

- ♦ **Pin for Pin Second Source!**
- ♦ **Low Supply Current: 120μA @5V**
- ♦ **Timing from μs to Days**
- ♦ **Programmable with Standard Thumbwheel Switches**
- ♦ **Cascadable for Long Range Timing**
- ♦ **Monostable or Astable Operation**
- ♦ **Low Power CMOS**

Ordering Information

PART	TEMPERATURE RANGE	PACKAGE
ICM7240IPE	-20°C to +85°C	16 Lead Plastic DIP
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240C/D	0°C to +70°C	Dice
ICM7250IPE	-20°C to +85°C	16 Lead Plastic DIP
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250C/D	0°C to +70°C	Dice
ICM7260IPE	-20°C to +85°C	16 Lead Plastic DIP
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260C/D	0°C to +70°C	Dice

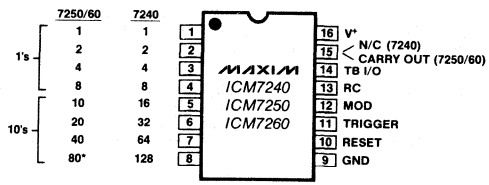
Typical Operating Circuit



1-99 Second Timer

Pin Configuration

Top View



*ICM7260 — Open Circuit

MAXIM
Dual Universal Switched Capacitor Filter

General Description

The MF10 is a dual 2nd order, switched capacitor, state variable filter. Each of the two filter sections uses two switched capacitor integrators and an op amp to generate a second order function. The location of the poles (and thus the center frequency and Q) is determined by the frequency of an external clock and 2 to 4 external resistors. No external capacitors are used.

Each of the two filter sections of the MF10 can generate all standard 2nd order functions: bandpass, lowpass, highpass, notch (band-reject), complex zeroes and allpass functions. Three of these functions are simultaneously available. The frequency of the 2nd order poles is accurate to ±0.2% and the Q is accurate to within 2%.

Fourth order filters can be made by cascading the two 2nd order filter sections of the MF10, and higher order filters can easily be made by cascading more MF10s. The excellent accuracy and stability of MF10 based filters eliminates the complex, costly tuning normally required in the production of high order (multipole) filters. Design equations for Butterworth, Bessel, Chebyshev, and Cauer (Elliptic) filters are provided.

Features

- **No External Capacitors Required**
- **Low Sensitivity to External Component Variation**
- **Excellent Frequency and Q Stability**
- **Easily Cascaded for Multipole Filters**
- **Filter Frequency Set by External Clock Frequency**
- **0.2% Clock to Center Frequency Ratio Accuracy**
- **Highpass, Lowpass, Bandpass, Notch, and Allpass Filter Functions.**
- **Up to 3 Simultaneous Filter Function Outputs**
- **Up to 30kHz Operation**
- **Easy to use—Design Directly from the Data Sheet**
- **Monolithic, Low Power CMOS Design**

Applications

This versatile device is used for a wide range of filtering applications such as:

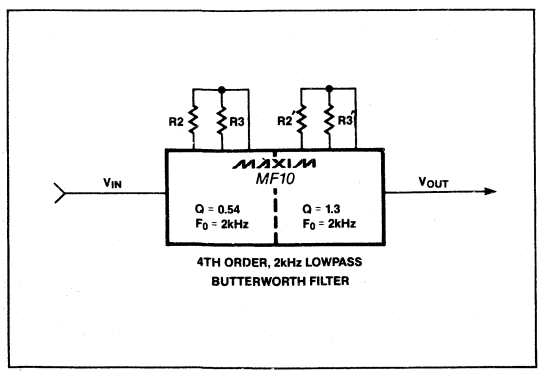
Tunable active filters
Multi-pole filters
Anti-aliasing filters
Adaptive Filtering
Phase locked loops
Signal Processing/ Conditioning

Ordering Information

PART	TEMP. RANGE	PACKAGE
MF10BD	0°C to +70°C	20 Lead CERDIP
MF10BN	0°C to +70°C	20 Lead Plastic DIP
MF10CD	0°C to +70°C	20 Lead CERDIP
MF10CN	0°C to +70°C	20 Lead Plastic DIP

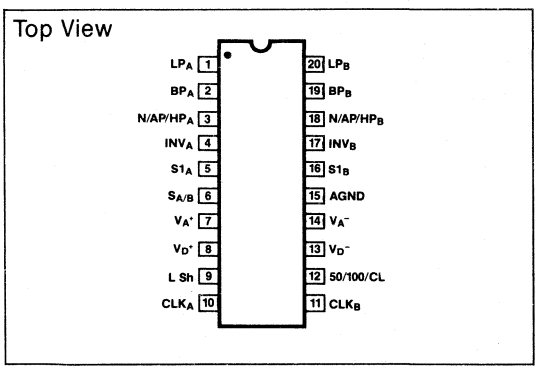
5

Typical Operating Circuit



4TH ORDER, 2kHz LOWPASS BUTTERWORTH FILTER

Pin Configuration



Dual Universal Switched Capacitor Filter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 14V
Power Dissipation 500mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Complete Filter)

(V_S = ±5V, T_A = +25°C)

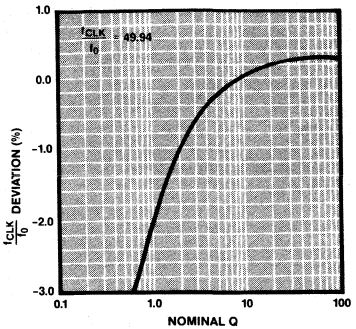
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	$f_o \times Q \leq 200$ kHz	20	30		kHz
Clock to Center Frequency Ratio, f_{CLK}/f_o					
MF10BN	Pin 12 High, Q = 10		49.94 ± 0.2%	±0.6%	
MF10CN	$f_o \times Q \leq$ 50kHz, Mode 1		49.94 ± 0.2%	±1.5%	
MF10BN	Pin 12 at Mid Supplies		99.35 ± 0.2%	±0.6%	
MF10CN	Q = 10, $f_o \times Q \leq$ 50kHz, Mode 1		99.35 ± 0.2%	±1.5%	
Q Accuracy (Q Deviation from an Ideal Continuous Filter)	$f_o \times Q \leq$ 50kHz $f_o \leq$ 5kHz, Mode 1		±2%	±6%	
f_o Temperature Coefficient	Pin 12 High (~50:1) Pin 12 Mid Supplies (~100:1) $f_o \times Q \leq$ 100kHz, Mode 1 External Clock Temperature Independent		±10 ±100		ppm/°C ppm/°C
Q Temperature Coefficient	$f_o \times Q \leq$ 100kHz, Q Setting Resistors Temperature Independent		±500		ppm/°C
DC Low Pass Gain Accuracy	Mode 1, R1 = R2 = 10kΩ		±1	±2	%
Crosstalk			50		dB
Clock Feedthrough			10		mV
Maximum Clock Frequency		1	1.5		MHz
Power Supply Current			7	10	mA

ELECTRICAL CHARACTERISTICS (Internal Op Amps)

(V_S = ±5V, T_A = +25°C)

PARAMETER	CONDITIONS	MIN	Typ	MAX	UNITS
Supply Voltage		±4	±5		V
Voltage Swing (Pins 1, 2, 19, 20)	R_L = 5kΩ				
MF10BN		±4.0	±4.1		V
MF10CN		±3.8	±3.9		V
Voltage Swing (Pins 3 and 18)	R_L = 3.5kΩ				
MF10BN		±4.0	±4.1		V
MF10CN		±3.8	±3.9		V
Output short Circuit Current					
Source			3		mA
Sink			1.5		mA
Gain Bandwidth Product			2.5		MHz
Slew Rate			7		V/μS

Dual Universal Switched Capacitor Filter



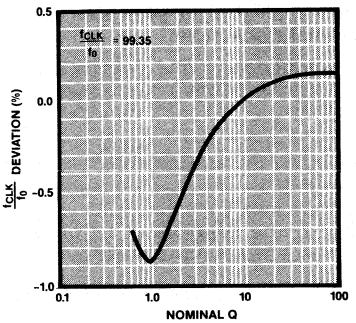


Table 1. PIN DESCRIPTION

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
LP	1	20	These are the lowpass, bandpass, and notch/allpass/highpass outputs of each 2nd order section. The LP and BP outputs can typically sink 1mA and source 3mA. The N/AP/HP output can typically sink 1.5mA and source 3mA.
BP	2	19	
N/AP/HP	3	18	
INV	4	17	INV is the inverting input of the summing op amp of each filter.
S1	5	16	This is an alternate signal input pin used in modes 1A, 4, 5 and 6B. This pin must be driven with a low source impedance.
$S_{A/B}$	6		The $S_{A/B}$ input controls a switch connecting one of the inputs of the filter's 2nd summer — either to analog ground ($S_{A/B}$ low) or to the low pass output ($S_{A/B}$ high). The $S_{A/B}$ input controls the configuration of both sections of the MF10.
V_A^+	7		Analog and digital positive supply inputs.
V_D^+	8		These pins are internally connected through the MF10's substrate and therefore V_A^+ and V_D^- should be derived from the same power supply source.
LSh	9		Level shift pin. This pin controls the digital input threshold level of the clock inputs, CLK_A and CLK_B. With the level shift pin at 0V and with ±5V power supplies, the clock inputs are TTL compatible. With the level shift pin connected to V_D^- the clock input thresholds are approximately 2V above V_D^-.

PIN NAME	PIN NUMBER Filter A	PIN NUMBER Section B	DESCRIPTION
CLK	10	11	Clock inputs for each switched capacitor building block. The duty cycle should be close to 50% to allow the op amps the maximum time to settle, particularly when the clock frequency is above 200kHz.
50/100/CL	12		This three-level input pin selects one of three MF10 operating conditions. When the 50/100/CL pin is connected to V_D^+ the ratio between clock frequency and center frequency is 50:1. With this pin at mid supplies (i.e., analog ground with dual supplies) the clock frequency to center frequency ratio is 100:1. Tying the pin low activates a simple current limiting circuitry which halts normal filtering operation and reduces the supply current by 70%.
V_D^-	13		Analog and digital negative supply inputs. These pins are internally connected. V_A^- and V_D^+ should be derived from the same power supply source.
V_A^-	14		
AGND	15		Analog Ground. This pin should be connected to the system ground for dual supply operation or driven to mid supply for single supply operation. The non-inverting inputs of the filter op amps are internally connected to the AGND pin, therefore AGND should be well bypassed.

Dual Universal Switched Capacitor Filter

Definition of Terms

f_{CLK}: The frequency applied to the switched capacitor filter external clock input.

f_0: The center frequency of the second order complex pole pair, f_0, is determined by measuring the peak response frequency at the bandpass output.

Q: "Quality factor", or Q, is the ratio of f_0 to the -3dB bandwidth of the second order bandpass filter. Q also determines the amount of amplitude peaking at the lowpass and highpass outputs, but is not measured at these outputs.

H_{OBP}: The gain in V/V of the bandpass output at $f=f_0$. See Figure 1.

H_{OLP}: The gain in V/V of the lowpass output as $f \rightarrow 0Hz$, See Figure 2.

H_{OHP}: The gain in V/V of the highpass output at $f = f_{CLK}/2$. See Figure 3.

Q_Z: The quality factor of the 2nd order function complex zero pair, if any.

f_z: The center frequency of the 2nd order complex zero pair. If f_z is different from f_0, and Q_z is high, f_z can be observed as a notch frequency at the allpass output.

f_{notch}: The frequency of minimum amplitude response at the notch output.

H_{OCZ1}: The complex zero output gain as $f \rightarrow 0Hz$.

H_{OCZ2}: The complex zero output gain at $f = f_{CLK}/2$.

H_{ON1}: The notch output gain as $f \rightarrow 0Hz$.

H_{ON2}: The notch output gain at $f = f_{CLK}/2$.

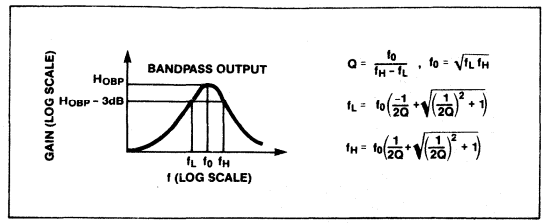


Figure 1. Bandpass Filter Terminology

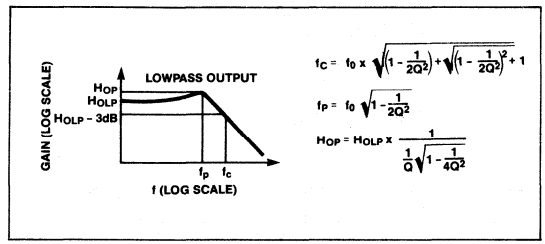


Figure 2. Lowpass Filter Terminology

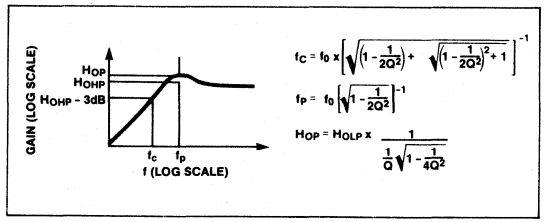


Figure 3. Highpass Filter Terminology

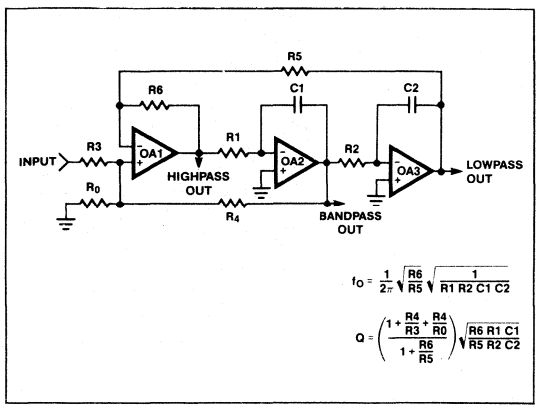


Figure 5. The Universal State Variable 2nd Order Active Filter Using RC Integrators

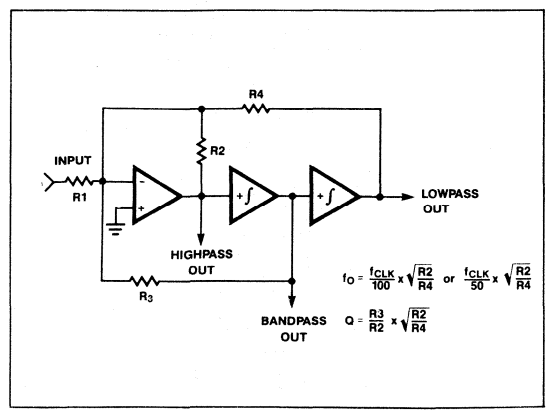


Figure 6. MF10 Universal State Variable 2nd Order Active Filter (Mode 3)

Dual Universal Switched Capacitor Filter

General Description

The MF10 is a switched capacitor (sampled data) filter. While the time domain approach most accurately describes the MF10's transfer functions, time domain calculations are cumbersome and most circuit designers are more familiar with the frequency domain approach used in designing RC active filters. Fortunately, the MF10 closely emulates RC active filters when the sampling frequency is much higher than the frequency band of interest. The operation of the MF10 can then be described in terms of the frequency domain with reasonable accuracy. Specifically, each of the two sections of an MF10 can be treated as a second order state variable filter. The similarity between the MF10 and the classic state variable filter allows the use of the extensive literature available on the design of 2nd order state variable filters.

The RC second order state variable filter (Figure 5) requires 3 op amps, 7 resistors, and 2 capacitors. This filter lacks the frequency stability and tunability of the MF10 switched capacitor filter. The MF10 excels in these areas because the center frequency of a switched capacitor filter is determined by the frequency of the clock, which, if crystal controlled, can achieve a stability of a few parts per million over the entire operating temperature range. Having the center frequency controlled by an external digital clock frequency also simplifies tuning of the filter since it is easier to accurately control a variable modulo divider than it is to precisely vary the time constant of an RC integrator.

The MF10's maximum guaranteed operating clock frequency is 1MHz, corresponding to a 20kHz maximum filter center frequency with a 50:1 clock to center frequency ratio, and a 10kHz maximum center frequency with a 100:1 clock to center frequency ratio.

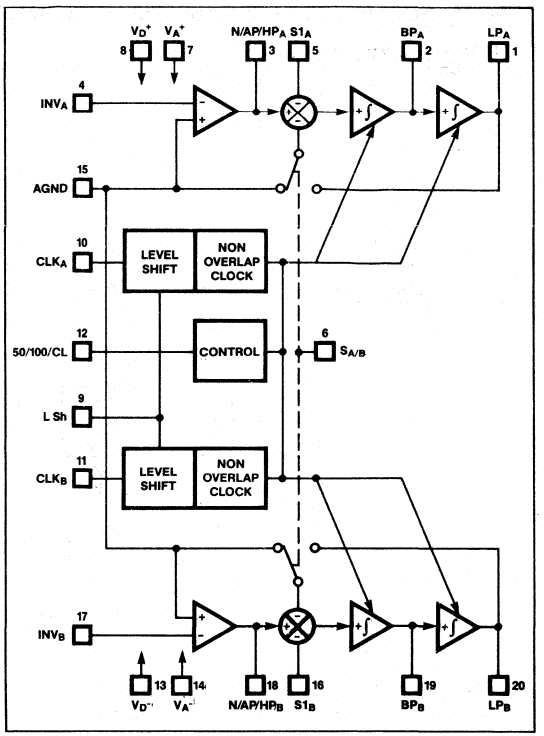


Figure 4. Block Diagram of the MF10

Filter Design

Simple 2nd Order Bandpass Filter Design

All modes except mode 6 offer a 2nd order bandpass response. The simplest circuit, mode 1A uses only two external resistors, but is limited to low Q operation by output swing limitations. Mode 1 uses three resistors and is suitable for either low or high Q bandpass functions. The center frequency of modes 1 and 1A is determined solely by the external clock frequency. Modes 2 and 3 are also suitable for bandpass filters, and are easier to implement in some applications since the center frequency is controlled by both the external clock frequency and a resistor ratio. See Table 2.

Second order bandpass filter functions are characterized by Q, center frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The center frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Table 2. MODE SELECTION

FILTER TYPE	MODE
Lowpass	1, 1A, 2, 3, 3A, 4, 5, 6A, 6B
Highpass	3, 3A, 6A
Bandpass	1, 1A, 2, 3, 3A, 4, 5
Notch	2, 3A, 5 (Complex Zero)
Allpass	4, 5

Dual Universal Switched Capacitor Filter

Table 3A. NORMALIZED LOWPASS FILTER PARAMETERS

NUMBER OF POLES	BUTTERWORTH		BESSELL		CHEBYSHEV					
					0.1dB RIPPLE		0.5dB RIPPLE		2dB RIPPLE	
	fn	Q	fn	Q	fn	Q	fn	Q	fn	Q
2	1.0	0.707	1.274	0.577	1.820	0.767	1.231	0.864	0.907	1.129
3	1.0	Real Pole	1.325	Real Pole	0.969	Real Pole	0.625	Real Pole	0.369	Real Pole
	1.0	1.000	1.450	0.691	1.300	1.341	1.069	1.706	0.941	2.552
4	1.0	0.541	1.432	0.522	0.789	0.619	0.597	0.705	0.471	0.929
	1.0	1.307	1.606	0.806	1.153	2.183	1.031	2.941	0.964	4.594
5	1.0	Real Pole	1.505	Real Pole	0.539	Real Pole	0.362	Real Pole	0.218	Real Pole
	1.0	0.618	1.559	0.564	0.797	0.915	0.690	1.178	0.627	1.775
	1.0	1.618	1.758	0.917	1.093	3.282	1.018	4.545	0.976	7.232
6	1.0	0.518	1.607	0.510	0.513	0.599	0.396	0.684	0.316	0.902
	1.0	0.707	1.692	0.611	0.834	1.332	0.768	1.810	0.730	2.844
	1.0	1.933	1.908	1.023	1.063	4.633	1.011	6.513	0.983	10.462
7	1.0	Real Pole	1.687	Real Pole	0.377	Real Pole	0.256	Real Pole	0.155	Real Pole
	1.0	0.555	1.719	0.532	0.575	0.846	0.504	1.092	0.461	1.646
	1.0	0.802	1.82	0.661	0.868	1.847	0.823	2.575	0.797	4.115
	1.0	2.247	2.053	1.126	1.045	6.233	1.008	8.842	0.987	14.280
8	1.0	0.510	1.781	0.506	0.382	0.593	0.297	0.677	0.238	0.892
	1.0	0.601	1.835	0.560	0.645	1.183	0.599	1.611	0.572	2.533
	1.0	0.900	1.956	0.711	0.894	2.453	0.861	3.466	0.842	5.584
	1.0	2.563	2.192	1.226	1.034	8.082	1.006	11.530	0.990	18.687

The normalized frequencies for the Butterworth and Bessel filters are for a -3dB frequency of 1Hz. The Chebyshev and Elliptic normalized frequencies are for filters whose amplitude response passes from the ripple band to the stopband at 1Hz.

Simple Lowpass Filter Design

Use mode 6 or 6A if a single pole lowpass filter is desired (such as the odd pole in an odd-ordered complex filter). Single pole resistor values are determined using the equations for modes 6 and 6A:

1) Select a value for R2, typically 10 to 100 kΩ.

2) Determine R3, using the selected value of R2, the available external clock frequency, and the desired cutoff frequency.

3) Determine the value of R1 to obtain the desired gain.

Modes 1 and 1A, with a fixed clock to cutoff frequency, are the simplest 2nd order lowpass configurations. Modes 2 and 3 allow tuning of the cutoff frequency by either changing the clock frequency or adjusting resistor ratios.

Second order lowpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 2 and 3 only, determine the value of R4 using the available external clock frequency and the selected value for R2. (The cutoff frequency of mode 1 and 1A is determined solely by the external clock frequency.)

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Simple Highpass Filter Design

Use mode 3 or 3A to implement 2nd order highpass filters and mode 6 for a single pole highpass filter.

Second order highpass filter functions are characterized by Q, cutoff frequency, and gain (or amplitude response). Resistor selection should follow these steps, using the design equations for the selected mode:

1) Pick a value for R2, typically 10 to 100 kΩ.

2) For modes 3 and 3A, determine the value of R4 using the available external clock frequency and the selected value for R2.

3) Determine the value of R3, using the desired Q and the previously determined values of R2 and R4.

4) Determine the value of R1 required to obtain the desired filter gain.

Multi-pole Filter Design

The two 2nd order filter sections of the MF10 can be cascaded to obtain a 4th order (4 pole) filter response. Several MF10s can be cascaded to get very high order filter responses. Unlike filters based on RC time constants, MF10-based filters usually do not require tuning of each section since the Q and center frequencies are precisely controlled by the external clock frequency and the ratio of external resistors.

The information included here is for the most common types of multi-pole filters: Butterworth, Bessel, Chebyshev, and Elliptic or Cauer. The design information given is for a 1Hz lowpass filter. However this filter can be transformed to any desired filter type and frequency using the following steps:

Table 3B. CAUER OR ELLIPTICAL FILTER PARAMETERS

NUMBER OF POLES	STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 1.5, PASSBAND RIPPLE = 0.5dB				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 2.0, PASSBAND RIPPLE = 0.5db				STOPBAND EDGE FREQUENCY / PASSBAND EDGE FREQUENCY = 3.0, PASSBAND RIPPLE = 0.5dB			
	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)	F_n	Q	F_z	A_{min} (dB)
2	1.266	0.969	1.982	8.3	1.262	0.803	2.732	13.9	1.247	0.737	4.182	21.5
3	0.767 1.072	Real Pole 2.208	1.675	21.9	0.693 1.072	Real Pole 1.859	2.27	31.2	0.653 1.070	Real Pole 1.697	3.439	42.8
4	1.03 0.687	3.922 1.087	1.592 3.478	36.2	1.031 0.641	3.32 1.13	2.143 4.992	48.6	1.031 0.615	3.032 1.159	3.3233 7.647	64.2
5	0.426 1.016 0.759	Real Pole 6.118 1.754	1.557 2.332	50.6	0.393 1.017 0.725	Real Pole 5.193 1.723	2.089 3.251	66.1	0.375 1.017 0.705	Real Pole 4.747 1.711	3.146 5.008	85.5

1) Identify the type of transfer function (lowpass, highpass, bandpass, etc.); the type of response (Butterworth, Bessel, Chebyshev, etc.); the number of poles, and the cutoff frequency.

2) Determine the normalized lowpass filter frequency and Q of each filter section, using Table 3A or 3B.

3) If a multi-pole transfer function other than lowpass is desired, perform the filter type transformation, as described below.

4) Denormalize each filter section frequency, fn, by multiplying the fn by the actual desired cutoff or center frequency.

5) Select a mode of operation for each filter section. Mode 3 is suitable for most filters, including Bessel and Chebyshev. Butterworth filters can be implemented using either mode 3 or mode 1. Elliptical filters can be implemented using modes 2 and 3A. Modes 6 and 6A provide a single, real pole needed for odd-ordered transfer functions. Allpass and complex zeroes can be generated in modes 4 and 5.

6)Select a clock frequency. The ratio of clock frequency to center frequency can be adjusted with resistor ratios in modes 2,3,5 and 6; allowing the use of any conveniently available clock frequency that is approximately 20 to 200 times the desired cutoff or center frequency.

7) Determine the resistor values for each filter section, using the design procedures given in the sections above for simple 2nd order bandpass, lowpass and highpass filters.

Tables 3A and 3B gives the normalized filter frequency and Q for each second order section of a multi-pole filter. Filters with an odd number of poles have one entry with "real pole" in the Q column. This denotes a real pole that should be implemented using mode 6 or a simple RC section.

Lowpass to Highpass Transformation.

The cutoff frequency and Q of each lowpass section is transformed using these equations:

$$f_n(\text{highpass}) = \frac{1}{f_n(\text{lowpass})}$$

$$Q(\text{highpass}) = Q(\text{lowpass})$$

Lowpass to Bandpass Transformation.

If the ratio between the upper and lower -3dB cutoff frequencies is greater than 1.5, the best way to make the desired bandpass filter is to cascade a lowpass filter and a highpass filter. The lowpass filter's cutoff frequency should be set to the desired bandpass upper cutoff frequency, and the highpass filter's cutoff frequency should be set to the desired bandpass filter lower cutoff frequency.

For very narrowband filters, several sections with identical center frequencies can be cascaded. When identical bandpass filters are cascaded, the Q of the resultant filter is

$$Q = \frac{Q}{\sqrt{2^n - 1}}$$

where Q is the Q of each individual filter section, B is the bandwidth of each individual filter section, and n is the number of identical sections cascaded. See table 4.

Table 4. CASCADING IDENTICAL BANDPASS FILTER SECTIONS

NUMBER OF IDENTICAL BANDPASS SECTIONS	BANDWIDTH	Q
1	1.000 B	1.00 Q
2	0.644 B	1.55 Q
3	0.510 B	1.96 Q
4	0.435 B	2.30 Q
5	0.386 B	2.60 Q

Dual Universal Switched Capacitor Filter

Application Hints

1) The maximum output swing is typically to within 1V of either supply rail. Check the peak amplitude response gains, H_{OBP}, H_{OLP}, H_{OHP}, and the input signal level to ensure that the outputs will not be driven beyond their maximum output swing range. This caution particularly applies to mode 1A when used with high Q values. The section labeled "Circuit Dynamics" is included in the description of each mode to clarify the relationship between the various filter parameters and the output amplitude peaking at the filter outputs. The lower Q sections of cascaded filters should precede the sections with high Q. This reduces the possibility of output clipping.

2) The absolute values of resistors are not critical, only the ratios between resistors directly affect filter operation. The absolute values must be high enough so that the output drive currents do not approach the limits of 3mA source current and 1mA sink current. At the other extreme, resistor values should not be so high that stray leakage currents and stray capacitances have a significant effect on circuit operation.

3) Selecting 100:1 operation doubles the number of samples per output cycle, and halves the number of output steps compared to 50:1 operation. On the other hand, 50:1 allows higher frequency operation (20kHz max vs. 10kHz max), and also offers better center frequency stability (±10ppm/°C vs. ±100ppm/°C).

4) The minimum frequency of operation is limited by the rate of discharge of the internal switched capacitors. The droop rate at the output of the integrators will be approximately 0.1mV/ms. This limits the lower value of clock frequency to about 100Hz for reasonable accuracy, corresponding to a center frequency of 1Hz using the 100:1 mode.

5) For the best accuracy in setting the center frequency, use the corrections shown in the Typical Operating Characteristic graphs. These graphs aid in the correction for the slight interaction between clock frequency, Q, and center frequency.

6) As with all sampled data systems, high frequency components of the input signal above half the clock rate will be aliased. In particular, input signal components with frequencies near the clock rate will generate difference frequencies that may fall within the passband of the lowpass and bandpass filters. Since the ratio of clock frequency to center frequency is approximately 50:1 or 100:1, a simple one pole passive RC filter will be sufficient filtering in many cases. In many other cases the input signal will itself be band-limited and will not require additional filtering.

7) The $S_{A/B}$ input controls the source of feedback into the three input summer of both sections of the MF10. If your design requires that the input of one section's summer be grounded and the input to the other section's summer be connected to the lowpass output, check to see if $S_{A/B}$ can be connected to V_D^- and the lowpass output connection made via the $S1_A$ (or $S1_B$) input.

8) If large input voltage signals are applied to the filter, the DC offset voltages of the MF10 may cause output clipping. For a more detailed discussion see the section on DC Offsets.

9) For best results, the positive and negative supplies should be bypased to AGND with a 10μF tantalum and 0.1μF ceramic capacitors.

Mode 1A
Non-Inverting Bandpass, Inverting Bandpass, Lowpass.

This minimum component count configuration uses only two external resistors. The peak gain at the inverting bandpass output is equal to the Q times the input voltage, so this circuit should only be used for low Q applications. The ratio of bandpass center frequency to clock frequency is fixed at either 50:1 or 100:1, as selected by the 50/100/CL input.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -1$$

$$H_{OBP1} = -\frac{R3}{R2}$$

$$H_{OBP2} = 1 \text{ (non-inverting)}$$

Circuit Dynamics

$H_{OBP1} = Q$ (this is the reason for the low Q recommendation)

$H_{OLP\ (peak)} = Q \times H_{OLP}$ (for high Qs)

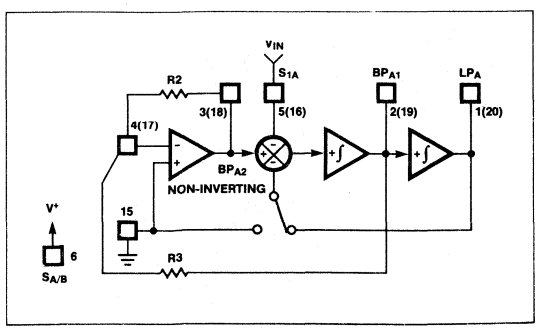


Figure 7. Mode 1A

Dual Universal Switched Capacitor Filter

Mode 1
Notch, Bandpass, and Lowpass

Like Mode 1A, f_0 is fixed at $f_{CLK}/50$ or $f_{CLK}/100$. The gain at all three outputs is inversely proportional to the value of R1; and unlike Mode 1A, high Q bandpass filters can be built without exceeding the output swing range of the bandpass output amplifier. The notch and bandpass center frequencies are identical. The notch output gain is the same above and below the notch center frequency.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

$$f_{notch} = f_0$$

$$Q = \frac{R3}{R2}$$

$$H_{OLP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\left(\text{as } f \rightarrow 0\right) = -\frac{R2}{R1}$$

$$H_{ON}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$$

Circuit Dynamics

$H_{OBP} = H_{OLP} \times Q = H_{ON} \times Q$

$H_{OLP(peak)} = Q \times H_{OLP}$ (if the DC gain of the LP output is too high, a high Q value could cause clipping at the lowpass output resulting in gain non-linearity and distortion at the bandpass output).

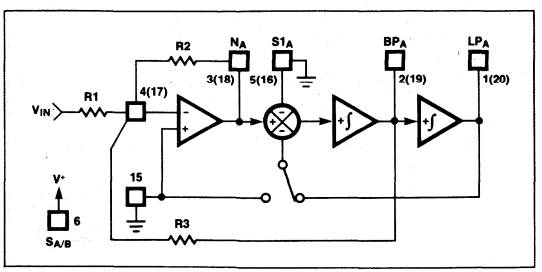


Figure 8. Mode 1

Mode 2
Notch, Bandpass, and Lowpass

The circuit of mode 2 is created by adding resistor R4 to the circuit of mode 1. This fourth resistor causes the ratio of the bandpass center frequency to clock frequency to be less than the fixed 50:1 or 100:1 ratio of mode 1. Stated another way, R4 allows the center frequency of the bandpass filter to be tuned to a higher frequency while maintaining a constant clock frequency. The notch frequency remains at $f_{CLK}/50$ or $f_{CLK}/100$, making mode 2 suitable for elliptic highpass filters, where the complex zero pair (f_{notch}) must be lower than the complex pole (f_0).

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_n = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50} \quad ; \quad Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$H_{OLP} = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}} \quad ; \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON1}\left(\text{as } f \rightarrow 0\right) = \frac{-\frac{R2}{R1}}{1 + \frac{R2}{R4}}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

Circuit Dynamics

$$H_{OBP} = Q\sqrt{H_{OLP} \times H_{ON_2}} = Q\sqrt{H_{ON_1} \times H_{ON_2}}$$

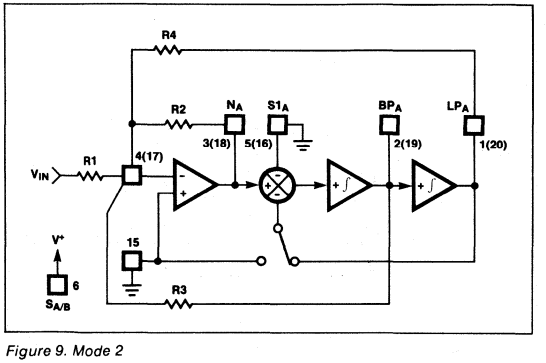


Figure 9. Mode 2

Dual Universal Switched Capacitor Filter

Mode 3
Highpass, Bandpass, and Lowpass

This mode is a sampled time (Z transform) equivalent of the classical 2nd order state variable filter. In this versatile mode, the ratio of resistors R2 and R4 can move the center frequency both above and below the $f_{CLK}/50$ and $f_{CLK}/100$ values. Mode 3 is commonly used to make multiple pole Chebyshev filters with a single clock frequency. A small (10-100pF) capacitor in parallel with R4 may be needed to avoid Q enhancement.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \quad \text{or} \quad \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$H_{OHP} = -\frac{R2}{R1}$$

$$H_{OBP} = -\frac{R3}{R1}$$

$$H_{OLP} = -\frac{R4}{R1}$$

Circuit Dynamics

$$H_{OHP} = H_{OLP}\left(\frac{R2}{R4}\right)$$

$$H_{OLP(peak)} = Q \times H_{OLP}$$

$$H_{OBP} = Q\sqrt{H_{OHP} \times H_{OLP}}$$

$$H_{OHP(peak)} = Q \times H_{OHP}$$

Mode 3A
Highpass, Bandpass, Lowpass, and Notch

Similar to mode 3, this mode adds an external op amp. This op amp creates a notch output by summing the highpass and lowpass outputs of the MF10. The ratio of resistors R_H and R_L adjusts the notch frequency, while R2 and R4 adjust the bandpass center frequency. Since the notch (zero pair) frequency can be adjusted to both above and below f_0, mode 3A is suitable for both lowpass and highpass elliptic or Cauer filters. In multipole elliptic filters only one external op amp is needed. Use the inverting input of the internal op amp as the summing node for all but the final section of the filter.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{\frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R2}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{\frac{R2}{R4}}$$

$$f_{notch} = \frac{f_{CLK}}{100} \times \sqrt{\frac{R_H}{R_L}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{\frac{R_H}{R_L}}$$

$$H_{OHP} = -\frac{R2}{R1} \quad H_{OLP} = -\frac{R4}{R1} \quad H_{OBP} = -\frac{R3}{R1}$$

$$H_{ON}\ (\text{at } f = f_0) = \left|Q\left(\frac{R_G}{R_L} H_{OLP} - \frac{R_G}{R_H} H_{OLP}\right)\right|$$

$$H_{ON1}\ (\text{as } f \to 0) = \frac{R_G}{R_L} \times H_{OLP}$$

$$H_{ON2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R_G}{R_H} \times H_{OHP}$$

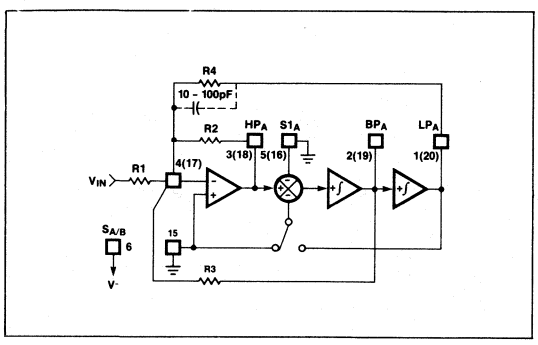


Figure 10. Mode 3

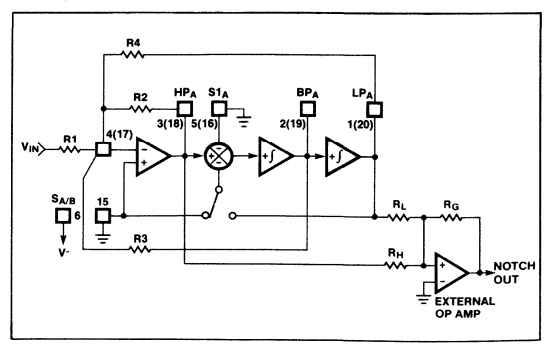


Figure 11. Mode 3A

Dual Universal Switched Capacitor Filter

Mode 4
Allpass, Bandpass, and Lowpass

Mode 4 provides an allpass output which has a nearly flat amplitude response with a phase shift that changes linearly with frequency (a constant time delay). For a flat amplitude response R2 must equal R1, fixing the allpass gain at -1.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50}$$

f_z (frequency of complex zero pair) = f_0

$$Q = \frac{R3}{R2}$$

Q_z (Q of complex zero pair) = $\frac{R3}{R1}$

$$H_{OAP} = -\frac{R2}{R1} = -1$$

$$H_{OLP} = -\left(\frac{R2}{R1} + 1\right) = -2$$

$$H_{OBP} = -\left(1 + \frac{R2}{R1}\right) \times \frac{R3}{R2} = -2\frac{R3}{R2}$$

Circuit Dynamics

$$H_{OBP} = H_{OLP} \times Q = (H_{OAP} + 1)Q$$

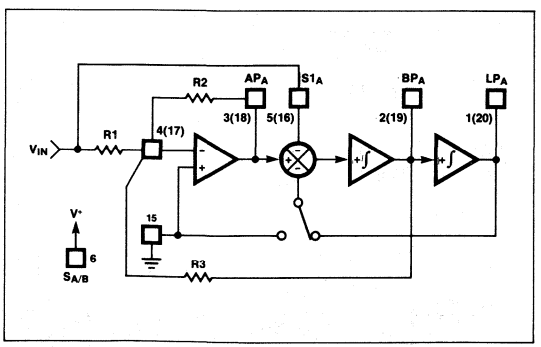


Figure 12. Mode 4

Mode 5
Complex Zero, Bandpass, and Lowpass

The addition of R4 to the circuit of mode 4 allows the independent tuning of the complex zero frequency, f_Z, and the complex pole frequency, f_0. Mode 5 can achieve a more constant allpass amplitude vs. frequency response than can be achieved with mode 4.

Design Equations

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 + \frac{R2}{R4}}$$

$$f_z = \frac{f_{CLK}}{100} \times \sqrt{1 - \frac{R1}{R4}} \text{ or } \frac{f_{CLK}}{50} \times \sqrt{1 - \frac{R1}{R4}}$$

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

$$Q_z = \frac{R3}{R1} \times \sqrt{1 - \frac{R1}{R4}}$$

$$H_{OCZ1} \text{ (as } f \to 0) = \frac{R2(R4 - R1)}{R1(R2 + R4)}$$

$$H_{OCZ2}\left(\text{at } f = \frac{f_{CLK}}{2}\right) = \frac{R2}{R1}$$

$$H_{OBP} = \frac{R3}{R2} \times \left(1 + \frac{R2}{R1}\right)$$

$$H_{OLP} = \frac{R4}{R1} \times \left(\frac{R2 + R1}{R2 + R4}\right)$$

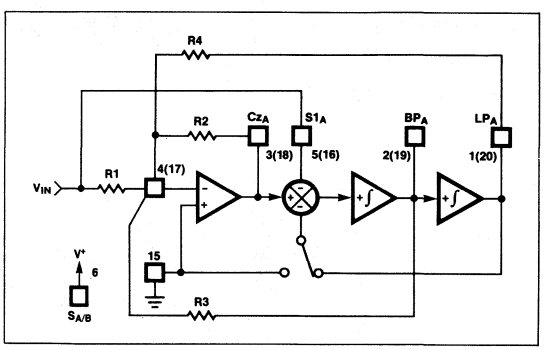


Figure 13. Mode 5

Dual Universal Switched Capacitor Filter

Mode 6A
Single Pole; Highpass and Lowpass

This circuit provides a single real pole for use in odd-ordered cascaded filters. Unlike the simple RC pole used in continuous filters, the MF10 single pole filter can be tuned by simply changing the clock frequency. The cutoff frequency is also resistor tunable.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} = -\frac{R3}{R1}$$

$$H_{OHP} = -\frac{R2}{R1}$$

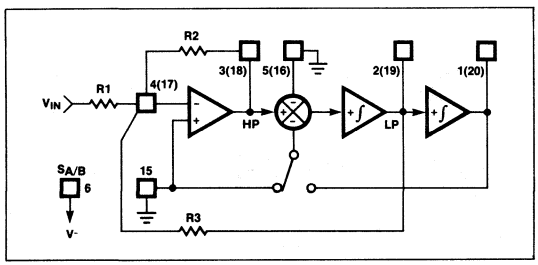


Figure 14. Mode 6A

Mode 6B
Single Lowpass Pole; Inverting and Non-Inverting

As with mode 6A, this mode is useful in implementing filters with an odd number of poles.

Design Equations

$$f_c \text{ (cutoff frequency)} = \frac{f_{CLK}}{100} \times \left(\frac{R2}{R3}\right) \text{ or } \frac{f_{CLK}}{50} \times \left(\frac{R2}{R3}\right)$$

$$H_{OLP} \text{ (inverting output)} = -\frac{R3}{R2}$$

$$H_{OLP} \text{ (non-inverting output)} = +1$$

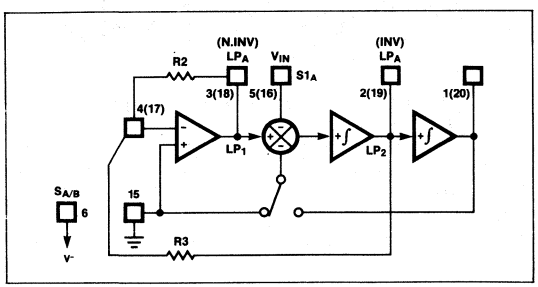


Figure 15. Mode 6B

MF10 Offsets

The MF10's switched capacitor integrators have higher equivalent input offsets than the typical RC integrator in a continuous active filter. The MF10 offsets are produced by parasitic charge injection from the switches into the integrating capacitors. These offsets are relatively independent of clock frequency and temperature. The input offset of the CMOS op amps also contribute to the overall offset error, but these offsets are small in comparison to the offsets caused by charge injection. Figure 16 shows the equivalent circuit for calculating output DC offsets.

V_{OS1} = 0 mV to ±10 mV

V_{OS2} = charge injected offset plus op amp offset
≈ -60 mV to -80 mV (50:1)

V_{OS3} = charge injected offset plus op amp offset
≈ +100 mV to +150 mV (at 50:1)

(At 100:1 the V_{OS2} and V_{OS3} are approximately doubled.)

Using the same designation for resistors as are used in Figures 7 to 15, the output offsets can be calculated as shown below.

Mode 1 and Mode 4 Output Offsets

$$V_{OS(N)} = V_{OS1}\left(\frac{1}{Q} + 1 + |H_{OLP}|\right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

Mode 2 and Mode 5 Output Offsets

$$V_{OS(N)} = \left(\frac{R2}{R_p} \pm 1\right) V_{OS1} \times \frac{1}{1 + R2/R4}$$

$$+ V_{OS2}\frac{1}{1 + R4/R2} - \frac{V_{OS3}}{Q\sqrt{1 + R2/R4}}$$

$$R_p = R1//R2//R4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

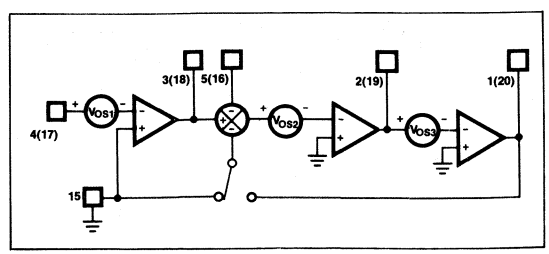


Figure 16. MF10 Offset Model

Mode 3 Output Offsets

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = -\frac{R4}{R2} \times \left(\frac{R2}{R3} V_{OS3} + V_{OS2}\right) + \frac{R4}{R2} \times \left(1 + \frac{R2}{R_p}\right) V_{OS1}$$

$$R_p = R1//R3//R4$$

Mode 1A Output Offsets

$$V_{OS(N.INV.BP)} = \left(1 + \frac{1}{Q}\right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$

In most applications the outputs are AC coupled and the DC offsets present no problem unless large input voltages are applied to the filter.

For Mode 3 operation it should be noted that the use of small R2/R4 ratios and high Q will produce an LP output with a couple of volts DC offset and an offset adjustment should be made. Make the offset adjustment by injecting a small amount of current into the first op amp's inverting input (see Figure 17). This changes V_{OS1} but leaves the output DC offset of the integrators unchanged.

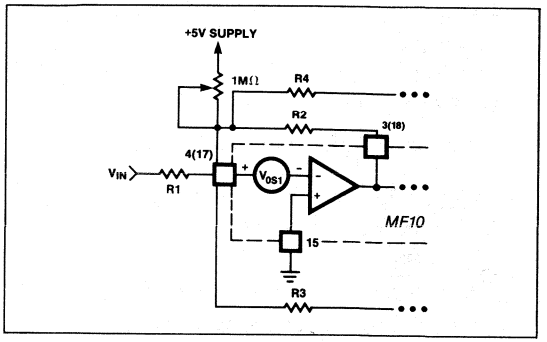


Figure 17. V_{OS} Adjustment

Application Examples

4th Order, 2kHz Lowpass Butterwoth Filter

A 4th order lowpass filter can be made by cascading the two second order filter sections of the MF10 (See Figure 18). Table 3 shows that the two sections of a Butterworth 4th order filter will have the same cutoff frequency, with one stage having a Q of 0.541 and the other stage having a Q of 1.307. Any of the modes may be used, but mode 1A uses only 2 resistors per section, and should therefore be used. The Q of both sections is low, so output clipping will not be a problem.

Using the 2nd order lowpass filter design steps shown in the Filter Design section, the resistor values for the first filter section can be calculated as follows:

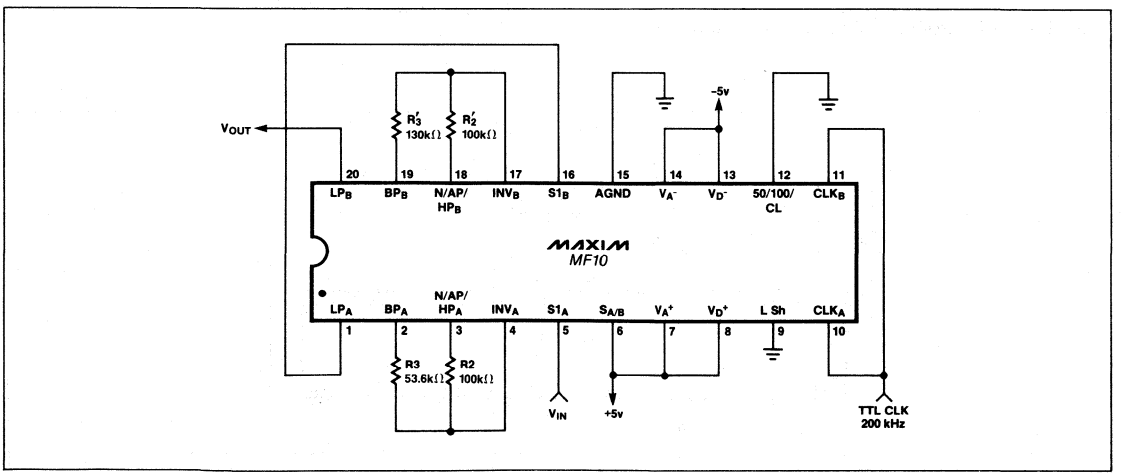


Figure 18. 4th Order, 2kHz Lowpass Butterworth Filter

Dual Universal Switched Capacitor Filter

Mode = 1A

f_0 = 2kHz
Q = 0.541

1) Let R2 be 100kΩ.

2) $f_0 = 2kHz = \frac{f_{CLK}}{100}$ (pin 12 mid-supply)

so f_{CLK} = 200kHz (pin 12 mid-supply)
f_{CLK} = 100kHz with pin 12 high.

3) $Q = \frac{R3}{R2}$;

so R3 = Q x R2 = 0.541 x 100kΩ = 54.1kΩ.

Picking the nearest 1% resistor value, R3 = 53.6 kΩ

Using similar calculations for the second filter section, R2=100kΩ and R3 = 130kΩ.

The output of the first section, LP_A (pin 1), is the input for the second stage, at $S1_B$ (pin 16). The filter output is at LP_B (pin 20). With ±5V supplies and the Level Shift pin connected to ground, the digital input threshold of the CLK inputs is about 1.6V. The CLK inputs can therefore be driven by either TTL or CMOS logic levels. The 50/100/CL pin is grounded, which selects a 100:1 ratio between the clock frequency and the lowpass cutoff frequency.

4th Order Chebyshev Lowpass Filter

Figure 19 shows a 4th order Chebyshev lowpass filter with the following specifications:

Passband Ripple = 2dB (nominal)
Cutoff Frequency = 5kHz

The filter uses a 200kHz clock for both sections.

Table 3 shows that for a 2dB ripple, 4th order Chebyshev filter the parameters of the two sections are:

f_n = 0.471 , Q = 0.929
and
f_n = 0.964 , Q = 4.594

Either mode 3 or mode 2 is suitable for this filter. The resistors for mode 2 can be calculated as follows:

1) Let R2 = 10kΩ.

2) For the first section f_n = 0.471, so for a 5kHz cutoff
f_0 = 0.471 x 5kHz = 2.355kHz

Using the mode 2 equation for f_0,

$$f_0 = \frac{f_{CLK}}{100} \times \sqrt{1 + \frac{R2}{R4}}$$

and using 200kHz for f_{CLK}, R4 is calculated as 25.87kΩ. The closest 1% resistor value of 26.1kΩ is chosen.

3) The mode 2 formula for Q is

$$Q = \frac{R3}{R2} \times \sqrt{1 + \frac{R2}{R4}}$$

Using Q= 0.929 and the previously determined values for R2 and R4, R3 is calculated as 7.9kΩ. The closest 1% value, 7.87kΩ is used.

4) Choose R1 for the desired filter gain. In this example R1 is 10kΩ.

Repeat the above steps for the second section, with f_n = 0.964 and Q = 4.594. If R2 is chosen to be 10kΩ, the value of R4 will be 2.1kΩ and the value of R3 will be 19.1kΩ.

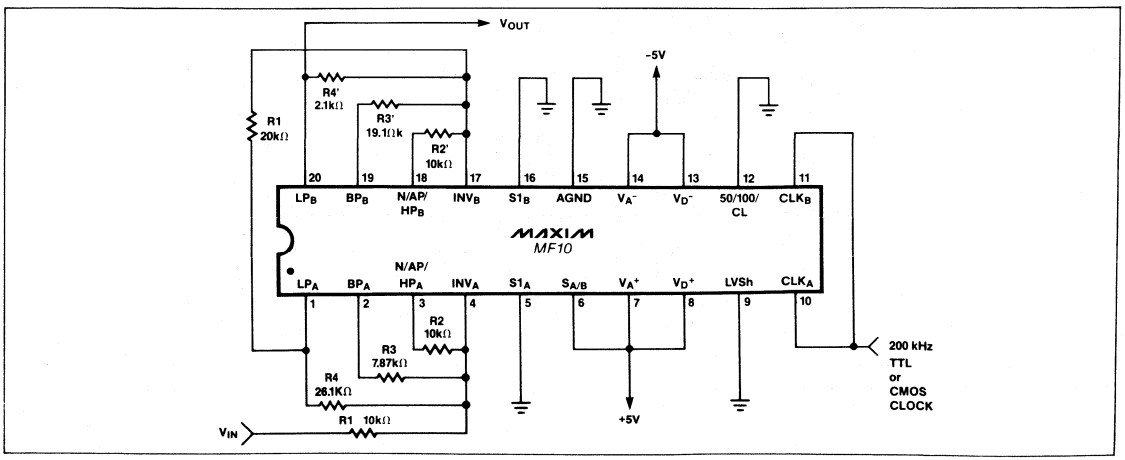


Figure 19. 4th Order Chebyshev 5kHz Lowpass Filter

Switched Capacitor Filter Fundamentals

While it is not necessary to understand the internal operation of the MF10 in order to use it, a basic understanding of switched capacitor operation may help in optimizing designs.

Figure 20 shows a standard integrator using an op amp. The time constant is determined by the passive components, R and C. When a positive input voltage is applied, the integrator output will ramp downward at a rate determined by the input voltage and the time constant, RC. This ramp has a slope of

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN}}{RC}$$

Figure 21 is a simple inverting switched capacitor integrator, where the R of the standard integrator has been replaced by a capacitor and two analog switches, S1 and S2. As S1 and S2 alternately open and close at the rate set by the clock input, first C1 is charged to the input voltage, then C1 transfers its charge into the capacitor C2. This creates a series of voltage steps on the integrator output, with each voltage step having a value of $-V_{IN} \times C1/C2$. If the value of C1 is small compared to C2, the series of steps at the integrator output approximates a ramp with the slope

$$\frac{\Delta V}{\Delta T} = -\frac{V_{IN} \times f_{CLK} \times C1}{C2}$$

where f_{CLK} is the frequency of the clock input.

This equation is similar to that of the standard integrator, but with the sampled capacitors time constant of

$$\frac{C2}{C1 \times f_{CLK}}$$

replacing the standard integrators time constant of RC. The center frequency of an RC based 2nd order state variable filter is

$$f_0 = \frac{1}{2\pi RC}$$

The center frequency of a switched capacitor 2nd order state variable filter is approximately

$$f_0 = \frac{f_{CLK} \times C1}{2\pi C2}$$

The ratio of C2/C1 in the MF10 is approximately 8 when the 50/100/CL input selects a 50:1 clock to center frequency ratio, and the ratio of C2/C1 is approximately 16 when the 50/100/CL input selects a 100:1 clock to center frequency ratio. Substituting these C2/C1 ratios in the above formula, the MF10 f_0 equation (for modes 1 and 6) results:

$$f_0 = \frac{f_{CLK}}{50} \text{ (50/100/CL Input High)}$$

or

$$f_0 = \frac{f_{CLK}}{100} \text{ (50/100/CL Input Mid-supply)}$$

The integrators used in the MF10 are non-inverting, and use the basic switching scheme of Figure 22. The switches ground one side of the input capacitor C1 when it is connected to the input; and connect the other side to ground while it is connected to the op amp's input. By changing the polarity of C1 in this manner, an additional inversion is added, and overall operation is non-inverting. This means the direction of the voltage ramp at the output of the integrator has the same polarity as V_{IN}.

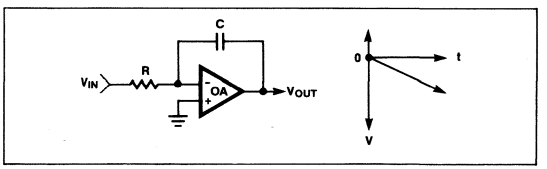


Figure 20. Typical RC integrator

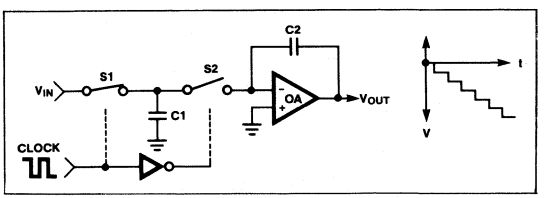


Figure 21. Simple Inverting Switched Capacitor Integrator

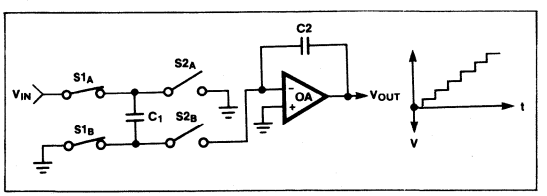
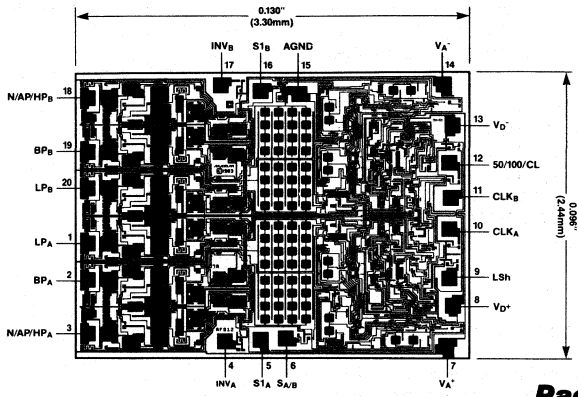


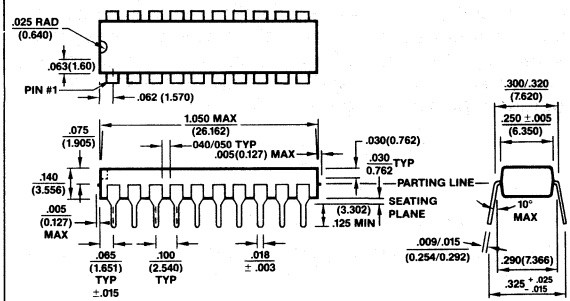
Figure 22. The Non-Inverting Integrator Used in the MF10

Dual Universal Switched Capacitor Filter

Chip Topography



Package Information



20 Lead Plastic DIP (N)
θ_{JA} = 125°C/W, θ_{JC} = 60°C/W

Small Outline (SO)

20 Lead CERDIP (D)

New Products

10 Volt Precision References

General Description

The AD2700 series of precision 10 volt reference sources offers excellent accuracy and stability. Laser trimming of both initial accuracy and temperature drift ensures high precision over the commercial (0°C to +70°C), industrial (-25°C to +85°C) and military (-55°C to +125°C) temperature ranges. The guaranteed absolute accuracy allows the user to configure systems without the need for ovens or chip heaters for temperature regulation. The AD2700 is a +10 volt output reference while the AD2701 is a -10 volt output. Both devices are guaranteed to 3ppm/°C max with 2.5mV initial accuracy. The AD2710, with a +10 volt output, is guaranteed to 1ppm/°C max with 1mV initial accuracy. These products are designed to interface with high accuracy, high resolution A to D and D to A converters, precision instrumentation, and data acquisition systems.

Applications

Precision D/A and A/D Converter Reference
Digital Voltmeters
Precision Test and Measurement Systems
Precision Calibrated Voltage Reference Standard
High Accuracy Transducers

Features

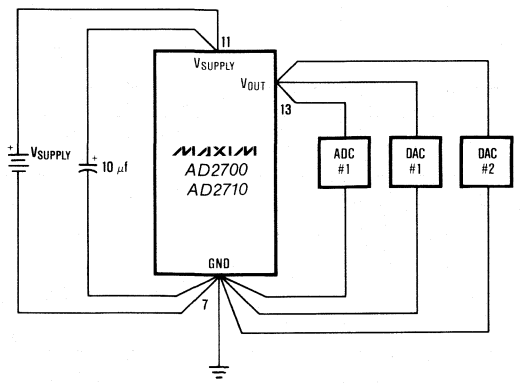
- **Pin-for-Pin 2nd Source!**
- **Excellent Initial Accuracy**
- **Low Temperature Coefficient**
- **Excellent Long-Term Stability, 50ppm/1000hrs.**
- **10mA Output Current Capability**
- **Superior Line Regulation: 100μV/V max.**
- **Standard Ceramic Side Brazed DIP**

Ordering Information

PART	OUTPUT VOLTAGE	TEMP. RANGE
AD2700JD	+10V, 10 ppm/°C	-25°C to +85°C
AD2700LD	+10V, 3 ppm/°C	-25°C to +85°C
AD2700SD	+10V, 3 ppm/°C	-55°C to +125°C
AD2700UD	+10V, 3 ppm/°C	-55°C to +125°C
AD2701JD	-10V, 10 ppm/°C	-25°C to +85°C
AD2701LD	-10V, 3 ppm/°C	-25°C to +85°C
AD2701SD	-10V, 3 ppm/°C	-55°C to +125°C
AD2701UD	-10V, 3 ppm/°C	-55°C to +125°C
AD2710LD	+10V, 1 ppm/°C	0°C to +70°C
AD2710KD	+10V, 2 ppm/°C	0°C to +70°C

All devices are available in a 14 lead ceramic side brazed DIP.

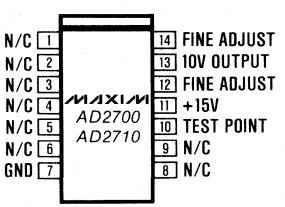
Typical Operating Circuit

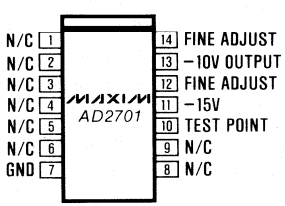


Precision +10V System Reference

Pin Configuration

Top View





10 Volt Precision References

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... +20V
Power Dissipation 400mW
Operating Temperature Range
AD2700JD, LD, AD2701JD, LD ..... -25°C to +85°C
AD2700SD, UD, AD2701SD, UD ..... -55°C to +125°C
AD2710KD, LD ..... 0°C to +70°C

Storage Temperature ..... -65°C to +160°C
Lead Temperature ..... +300°C
(soldering, 10 seconds)
Short Circuit to GND ..... Continuous

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +15V for AD2700 and AD2710, V_{IN} = -15V for AD2701, T_A = +25°C, R_L = 2kΩ, unless otherwise noted)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Initial Output Voltage	AD2700JD, SD	9.9950	10.0000	10.0050	V
	AD2700LD, UD	9.9975	10.0000	10.0025	V
	AD2701JD, SD	-10.0050	-10.0000	-9.9950	V
	AD2701LD, UD	-10.0025	-10.0000	-9.9975	V
	AD2710KD, LD	9.9990	10.0000	10.0010	V
Output Voltage Drift	AD2700,01JD $T_A = T_{MIN}$ to T_{MAX}			10	ppm/°C
	AD2700,01LD, SD, UD $T_A = T_{MIN}$ to T_{MAX}			3	ppm/°C
	AD2710KD T_A = +25°C to +70°C			2	ppm/°C
	AD2710LD T_A = +25°C to +70°C			1	ppm/°C
	AD2710KD T_A = 0°C to +25°C			5	ppm/°C
	AD2710LD T_A = 15°C to +25°C			2	ppm/°C
	AD2710LD T_A = 0°C to +15°C			5	ppm/°C
Output Voltage Range	AD2700JD, AD2701JD $T_A = T_{MIN}$ to T_{MAX}			±11.0	mV
	AD2700LD, AD2701LD $T_A = T_{MIN}$ to T_{MAX}			±4.3	mV
	AD2700SD, AD2701SD $T_A = T_{MIN}$ to T_{MAX}			±8.0	mV
	AD2700UD, AD2701UD $T_A = T_{MIN}$ to T_{MAX}			±5.5	mV
Output Current	For Specified Load Regulation T_A = 25°C $T_A = T_{MIN}$ to T_{MAX} V_{IN} = +13V to +18V (2700, 2710) V_{IN} = -13V to -18V (2701)			10 5	mA mA
Line Regulation	V_{IN} = +13.5V to +16.5V (2700, 2710)			100	μV/V
	V_{IN} = -13.5V to -16.5V (2701)			100	μV/V
Load Regulation	0 to 10mA to GND			50	μV/mA
Output Resistance	0 to 10mA to GND			0.05	Ω
Input Voltage Range	AD2700, AD2710	+13		+18	V
	AD2701	-13		-18	V
Quiescent Current	No Load		9	14	mA
Noise (Note 1)	0.1 to 10Hz		6	50	μV_{P-P}
Long Term Stability	T_A = +55°C		50		ppm/1000 hrs.
Output Adjust Range	See Figure 1 and 2		±20		mV
Output Adjust Temperature Drift Effect			±4		μV/°C per mV of adjust

Note 1: QA sample tested.

Theory of Operation

A zener voltage of approximately 6.3V is applied to the non-inverting input of an operational amplifier. This voltage is accurately amplified to produce a precise 10.000V output. The amplifier's gain setting resistors are actively laser-trimmed to produce the desired output voltage. The zener operating current is derived from the regulated output voltage, and actively laser-trimmed to produce the lowest drift over temperature at the output of the amplifier.

Discussion of Performance

The Maxim AD2700 and AD2701 are designed for applications requiring a precision voltage reference, where initial accuracy at room temperature and drift over temperature are of prime importance.

The drift specification of the AD2700 and AD2701 are guaranteed by making precise voltage measurements at -55°C, -25°C, +25°C, +85°C, and -125°C, while maintaining unit identity. In this way, three key specifications are guaranteed: initial accuracy, absolute accuracy over temperature, and drift. The upper and lower bound limits of absolute accuracy over temperature are established by the sum of the maximum initial output voltage error and the maximum drift from +25°C to T_{MAX}. For example, the AD2700LD limit of 4.3mV is calculated from the addition of 2.5mV initial output voltage error plus the temperature drift error of 1.8mV [3ppm/°C x 10V x (85°C - 25°C)].

The drift specification is defined using the "box method" (Fig. 3). The "box" is formed by the T_{MAX} and T_{MIN} temperatures and a diagonal with a slope equal to the maximum specified drift. The maximum and minimum output voltages must meet the following conditions:

$$\frac{(V_{OUTMAX} - V_{OUTMIN})/10V}{T_{MAX} - T_{MIN}} \times 10^6 \leq \text{drift specification}$$

This assures that the output voltage variation over the temperature change is contained within the box with V_{OUTMAX} and V_{OUTMIN} limits.

For example, the AD2700LD maximum drift specification of 3ppm/°C from -25°C to +85°C restricts ($V_{OUTMAX} - V_{OUTMIN}$) to less than 3.3mV.

The AD2710 drift specification is defined over the temperature range of 0°C to +70°C using the "butterfly" method (Fig. 4), where endpoint measurements are tested for temperature coefficient from 25°C independent of the nominal voltage. Each device is tested at 0°C, +15°C, +25°C, and +70°C with the output voltage data recorded at each temperature. After the initial accuracy is checked for 1mV deviation from +10.000V at +25°C, the devices are graded according to temperature coefficient (TC). The AD2710K has a temperature coefficient less than or equal to 2ppm/°C from +25°C to +70°C and 5ppm/°C from 0°C to +25°C. These temperature coefficients correspond to a maximum change of 0.45mV and 1.25mV respectively (see Fig. 4a).

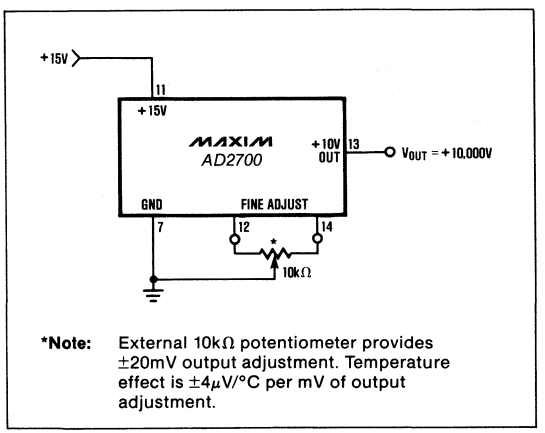
$$10V \times (V_{70°C} - V_{25°C}) \times 2x10^{-6} = 0.45mV$$
$$10V \times (V_{25°C} - V_{0°C}) \times 5x10^{-6} = 1.25mV$$

Similarly, the AD2710L is tested for 1ppm/°C from +25°C to +70°C, 2ppm/°C from +15°C to +25°C, and 5ppm/°C from 0°C to +15°C (see Fig. 4b). The corresponding voltage limits are 0.45mV from 25°C to +70°C, 0.2mV from +15°C to +25°C, and 0.75mV from 0°C to +15°C which, when added to the 0.2mV at +15°C, allows for 0.95mV change at 0°C.

Application Information

The Typical Operating Circuit shown on the front page shows the proper connection for the AD2700/2710. Special attention to layout is required to achieve the specified performance. A low resistance star configuration will reduce voltage errors, noise pickup, and noise coupled from the power supply.

The output voltage of the AD2700 and AD2710 can be trimmed, as shown in Figure 1, by connecting an external potentiometer between pins 12 and 14 with the wiper connected to ground. This external potentiometer provides typically ±20mV of output adjustment. The voltage drift will change by approximately 0.4ppm/°C (or 4μV/°C) per mV of adjustment.



*Note: External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.

Figure 1. Fine Trim Connection, AD2700 and AD2710

10 Volt Precision References

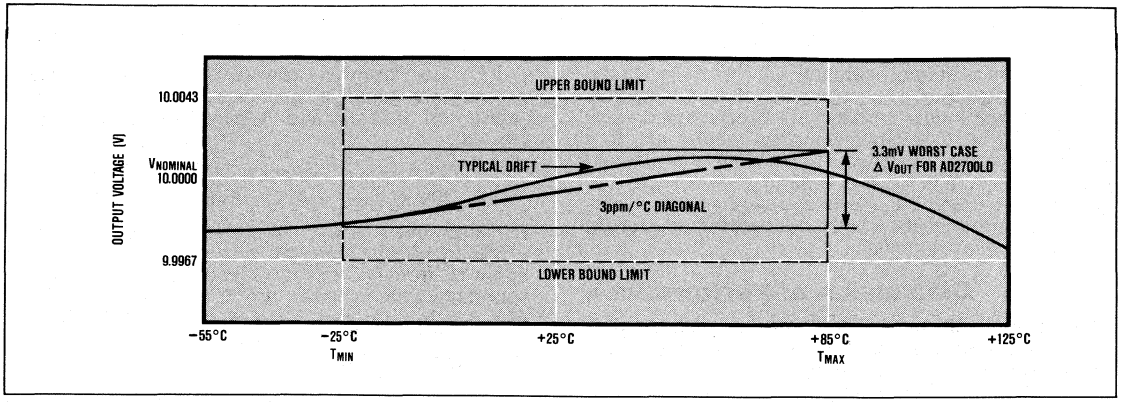
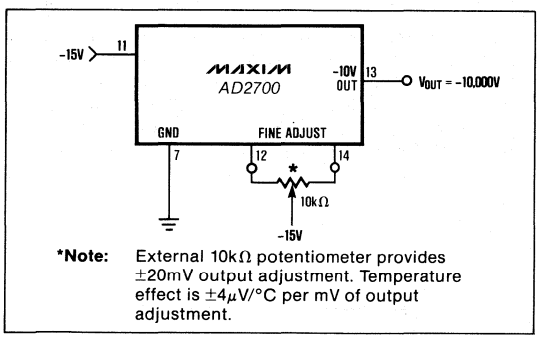


Figure 3. AD2700 Output Voltage Drift

The fine trim adjustment of the AD2701 is achieved by connecting the wiper of the potentiometer to V⁻, as shown in Figure 2.



***Note:** External 10kΩ potentiometer provides ±20mV output adjustment. Temperature effect is ±4μV/°C per mV of output adjustment.*

Figure 2. Fine Trim Connection, AD2701

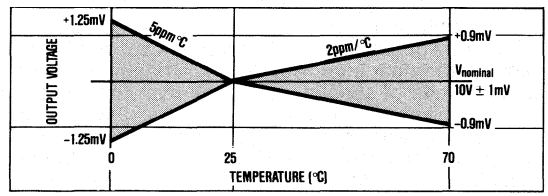


Figure 4a. AD2710K Output Voltage Drift

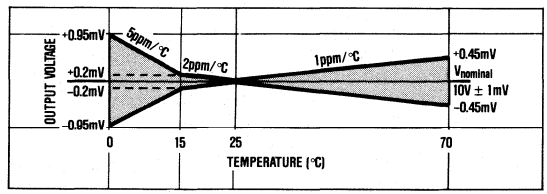
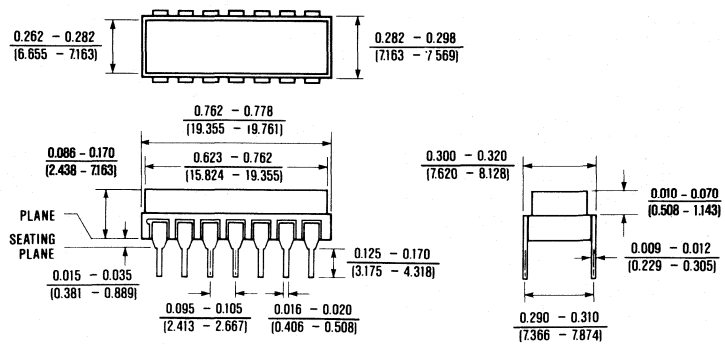


Figure 4b. AD2710L Output Voltage Drift

Packaging Information



14 Lead Ceramic

General Description

The BB3553 and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to 300MHz. Both devices are similar in their slew rate; up to 6000 volts per microsecond with light loads and 2000 volts per microsecond with a 50 ohm load. The LH0063 is not internally current limited, giving added versatility and higher transient drive capability.

Applications

High Speed Line Drivers
Video Drivers/Impedance Transformation
Nuclear Instrumentation Amplifiers
Operational Amplifier Isolation
High Speed A to D Input Buffers
Video Cross Point Switches

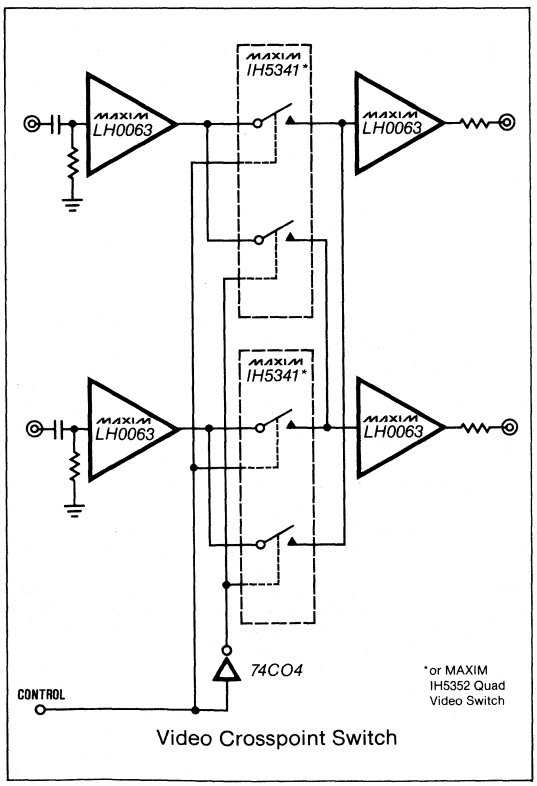
Features

- **Pin for Pin 2nd Source**
- **6000V/μSec Slew Rate**
- **DC to 300MHz Bandwidth**
- **±10V Output Drive Into 50Ω**
- **2ns Rise and Fall Times**
- **Wide Range Single or Dual Supply Operation**
- **10GΩ Input Resistance**

Ordering Information

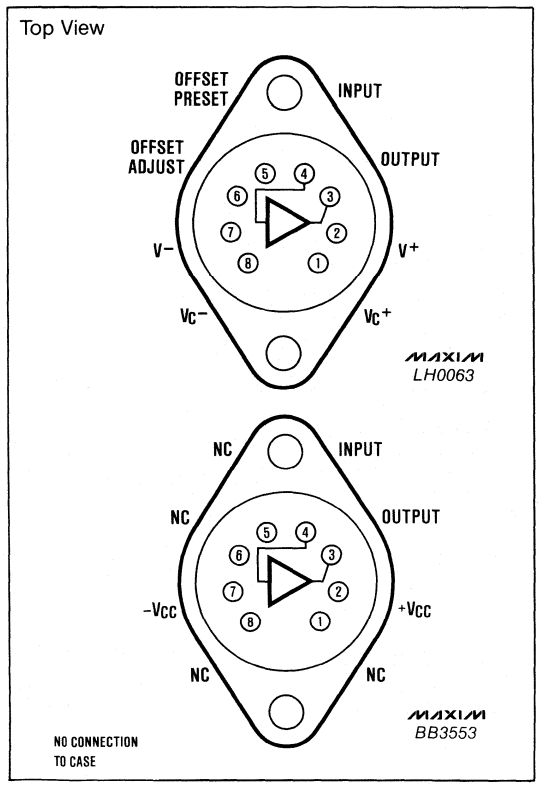
PART	TEMP. RANGE	PACKAGE
LH0063CK	-25°C to +85°C	8 Lead TO-3
LH0063K	-55°C to +125°C	8 Lead TO-3
BB3553AM	-25°C to +85°C	8 Lead TO-3

Typical Operating Circuit



Video Crosspoint Switch

Pin Configurations



Very Fast Buffer Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$) 40V
Maximum Power Dissipation (See Curves) 5W
Maximum Junction Temperature ..... 175°C
Input Voltage ..... V^+ to V^-
Continuous Output Current ..... ±250mA
Peak Output Current ..... ±500mA
Operating Temperature Range
LH0063 ..... -55°C to +125°C
LH0063C and BB3553AM ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_s = ±15V, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified) (Note 1)

PARAMETER	CONDITIONS	LH0063			LH0063C			BB3553AM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Offset Voltage	$R_S \leq 100k\Omega$, T_J = 25°C $R_L = 100\Omega$		10	25 100		10	50 100			50	mV mV
Average Temperature Coefficient of Output Offset Voltage	$R_S \leq 100k\Omega$ (Note 3)		300			300			300		µV/°C
Input Bias Current	T_J = 25°C (Note 2)		0.1	0.5		0.1	0.5			0.2	nA
Voltage Gain	V_{IN} = ±10V, $R_S \leq 100k\Omega$ $R_L = 1k\Omega$	0.94	0.96	1.00	0.94	0.96	1.00				V/V
Voltage Gain	V_{IN} = ±10V, $R_S \leq 100k\Omega$ $R_L = 50\Omega$, T_J = 25°C	0.92	0.93	0.98	0.91	0.93	0.98	0.92	0.93	0.98	V/V
Input Capacitance	T_A = 25°C (Note 3)		8.0			8.0			8.0		pF
Input Resistance	V_{IN} = ±1V, T_A = 25°C	10^{10}	10^{11}		10^{10}	10^{11}		10^{10}	10^{11}		Ω
Output Impedance	V_{OUT} = ±10V, $R_S \leq 100k\Omega$, $R_L = 50\Omega$		1.0	4.0		1.0	4.0		1.0	4.0	Ω
Output Current Swing	V_{IN} = ±10V, $R_S \leq 100k\Omega$	0.2	0.6		0.2	0.6		0.2	0.4		A
Output Voltage Swing	$R_L = 50\Omega$	10	13		10	13		10			V
Output Voltage Swing	V_S = ±5V, $R_L = 50\Omega$, T_J = 25°C	5.0	7.0		5.0	7.0					V
Supply Current	T_J = 25°C, $R_L = \infty$, V_S = ±15V (Note 4)		35	65		35	65		50	80	mA
Supply Current	V_S = ±5V (Note 4)		50			50					mA
Power Consumption	T_J = 25°C, $R_L = \infty$, V_S = ±15V (Note 4)		1.05	1.95		1.05	1.95		1.5	2.4	W
Power Consumption	V_S = ±5V (Note 4)		500			500					mW
External Offset Resistance	V_{OS} = 0mV, T_A = 25°C (Note 5)	0	300	1000	0	300	1000				Ω

Note 1: All devices are 100% tested at 25°C only. Specifications at temperature extremes are sample tested to 10% LTPD. These limits are not used to calculate outgoing quality level.
Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25°C. When supply voltages are ±15V, no-load operating junction temperature without a heat sink may rise 20-30°C above ambient, and more under heavy load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs. temperature graph for expected values.
Note 3: QA sample tested only.
Note 4: Guaranteed through correlated automatic pulse testing at T_J = 25°C.
Note 5: Offset adjust resistor for LH0063 connects between device pin 6 and V^-.

AC ELECTRICAL CHARACTERISTICS

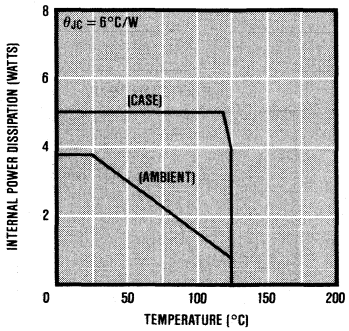
(V_S = ±15V, T_A = 25°C, R_S = 50Ω, R_L = 50Ω (Note 6))

PARAMETER	CONDITIONS	LH0063			LH0063C			BB3553AM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Slew rate	R_L = 1kΩ, V_{IN} = ±10V		6000			6000			6000		V/μS
Slew rate	R_L = 50Ω, V_{IN} = ±10V, T_J = 25°C	2000	2400		2000	2400		2000	2400		V/μS
Bandwidth	V_{IN} = 1.0V_{rms}		300			300			300		MHz
Bandwidth	Full Power, V_{IN} = 10V_{p-p}	32			32			32			MHz

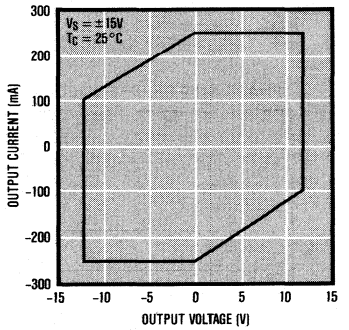
Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Typical Operating Characteristics

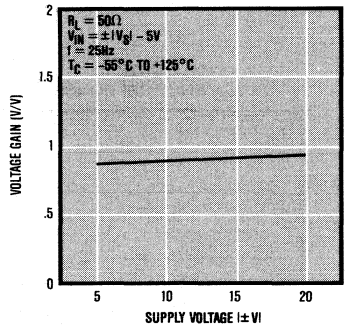
POWER DISSIPATION



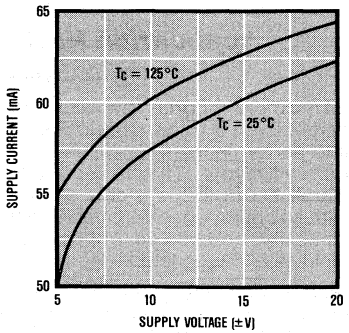
DC SAFE OPERATING AREA



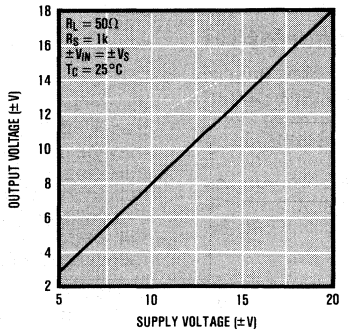
GAIN vs SUPPLY VOLTAGE



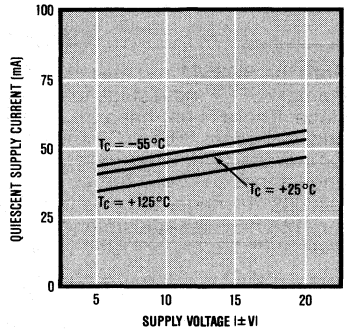
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT VOLTAGE vs SUPPLY VOLTAGE



QUIESCENT POWER SUPPLY CURRENT vs SUPPLY VOLTAGE

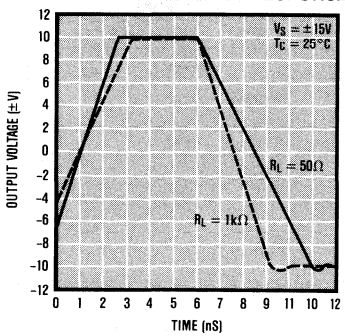


6

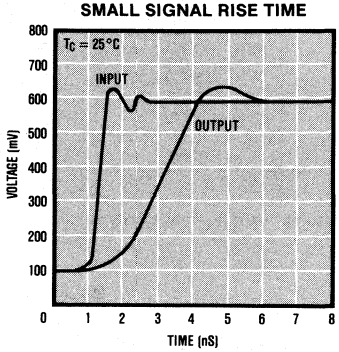
Very Fast Buffer Amplifiers

Typical Operating Characteristics

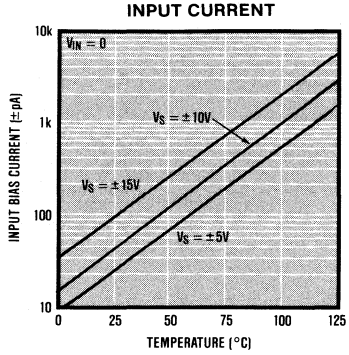
LARGE SIGNAL PULSE RESPONSE



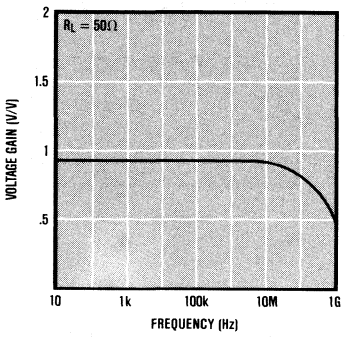
SMALL SIGNAL RISE TIME



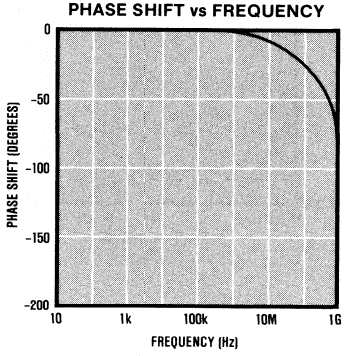
INPUT CURRENT



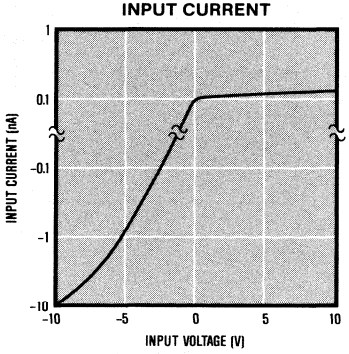
SMALL SIGNAL FREQUENCY RESPONSE



PHASE SHIFT vs FREQUENCY



INPUT CURRENT



Circuit Description

Both the BB3553 and the LH0063 consist of a complementary JFET input stage followed by a bipolar output stage. There is an inherent imbalance between the P and N channel JFETs (Q1 and Q2). Transistors Q3 and Q4 are laser trimmed current sources that correct circuit imbalances to make the offset voltage zero. On the LH0063, the negative current source is made available for optional user adjustment; the BB3553 can only be used at its factory adjusted value.

The BB3553 is internally current limited to 400mA at room temperature. This current limit is based on the V_{BE} of Q8 and Q9, so the limit point will be reduced at high temperatures. The LH0063 has no internal current limit, but has the output stage collectors brought out separately so that external current limiting can be implemented. This has the advantage that more output current is available with the LH0063, as long as the maximum power dissipation limit is not exceeded.

Application Hints

Circuit Layout

Circuit layout is one of the most important areas of high frequency circuit design. Even a good circuit design may yield only marginal performance when insufficient attention is paid to circuit layout. This is especially important with very high bandwidth systems or in a closed loop system with an operational amplifier. To get full performance capability from these buffers the following circuit guidelines are suggested:

1. **Use a ground plane.** It provides a shielded, low-resistance, low-inductance ground reference and reduces undesirable high-frequency coupling.
2. **Avoid IC sockets.** The increased inter-lead capacitance can degrade bandwidth and increase feedback capacitance. Contact resistance can cause offset errors that are difficult to account for.

3. **Keep input and output connections short.** This results in a more compact physical layout and minimizes parasitic coupling.
4. **Minimize capacitance.** When used with an op amp, minimize capacitance from output to feedback point and from feedback summing junction to ground.
5. **Keep wide traces.** Supply and output signal traces should be as wide as practical to minimize inductance and resistance.

Power Supply Decoupling

The positive and negative power supply terminals of the devices must be bypassed to ground with solid tantalum capacitors of about 4.7μF. A somewhat larger aluminum electrolytic can be used if shunted by a high frequency capacitor with good performance at 100 MHz. In any case, the high frequency decoupling capacitors should be placed no more than ¼ to ½ inch from the device pins. These capacitors must be returned to the same ground point on the ground plane or connected by a short, wide circuit board trace of low inductance and resistance.

Compensation

Buffer amplifiers are inherently stable in applications with resistive loads and adequate supply bypassing. However, there may be some tendency towards ringing or oscillation with capacitive loads of 100 pF or greater.

When a buffer amplifier is placed within the feedback loop of a high-gain op amp, the phase margin of the operational amplifier is reduced by an amount equal to the phase lag of the buffer at the amplifier's unity gain frequency. With most monolithic amplifiers, this will be a very small effect, but it should be considered for amplifiers active above 10MHz.

Power Dissipation and Device Rating

The maximum junction temperature of the BB3553 or the LH0063 is 150°C. This is the basic limitation that, in conjunction with the total thermal resistance, sets the maximum allowable power dissipation for either device. Specifically,

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where

$T_{J(MAX)}$ is the maximum allowable junction temperature of the device, e.g. 150°C

T_A is the ambient temperature

θ_{JC} is the junction to case thermal resistance, 6°C/W

θ_{CS} is the thermal resistance between the device case and the heatsink in °C/W

θ_{SA} is the thermal resistance for the heatsink to ambient in °C/W.

The θ_{JC} of the BB3553 and the LH0063 is typically 6°C/W; a conservative design should use a value of 10°C/W to allow for device-to-device variaitons in θ_{JC}. The actual power dissipation in a specific application is the sum of the quiescent power dissipation (1.5W typical for the BB3553; 1.05W typical for the LH0063 assuming ±15V power supplies) and the power dissipation in the output transistors. The dissipation in the output stage is the time average of the instantaneous product of the output current times the voltage difference between the output and the supply voltages.

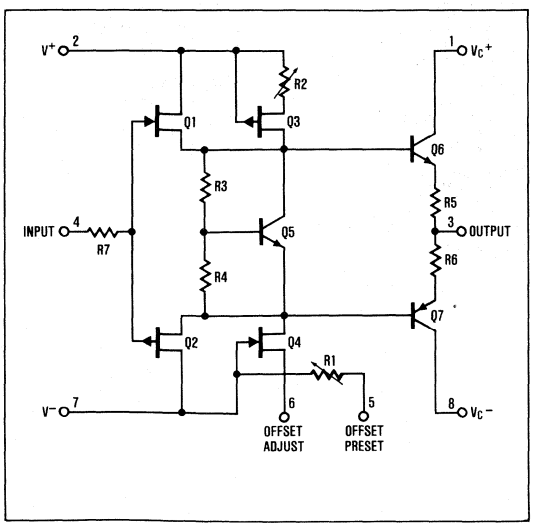


Figure 1. LH0063 Internal Structure

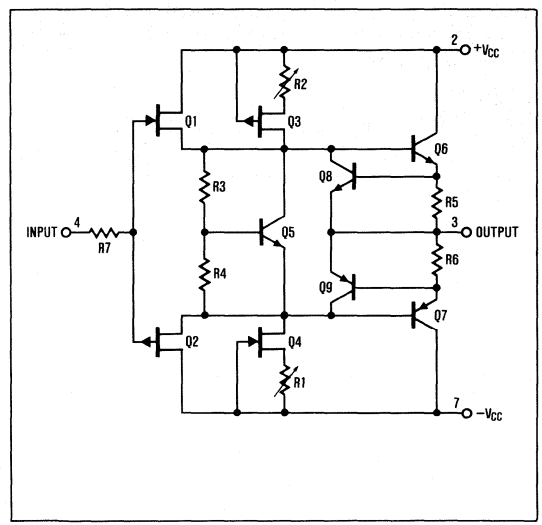


Figure 2. BB3553 Internal Structure

Very Fast Buffer Amplifiers

Operation from Single or Asymmetrical Power Supplies

Buffer amplifiers may be readily operated from single or asymmetrical power supplies with only a few precautions. Since the device has no ground pin and a gain of slightly less than one, an imbalance in the supplies appears to the buffer as a DC signal. It will amplify this DC signal by its gain, and will thus develop an apparent offset voltage different than the one specified in the Electrical Characteristics table. The additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.02(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.96

V^+ = Positive supply voltage

V^- = Negative supply voltage

Offset Voltage Adjustment

The normal definition of an amplifier's offset voltage is that voltage which must be applied to the input to produce zero volts at the output. This definition also applies to a buffer, but there are some other effects to consider. Most important is gain. A device that has a gain of 0.96 will develop nearly a volt of error when the input is taken to plus or minus 10V. In many applications the absolute value of the gain can be compensated.

The LH0063 has provisions for external offset voltage adjustment while the BB3553 is internally committed to its factory trimmed value. When not required, the offset adjust pins of the LH0063 must be shorted together. The external adjustment uses a 1kΩ potentiometer between pin 6 of the LH0063 and V^-. The table of DC electrical characteristics guarantees the MAXIM device to be adjustable to zero volts offset with the specified 1kΩ potentiometer.

TABLE 1. HEATSINKS FOR LH0063/BB3553

MANUFACTURER	PART #
Thermalloy	6002-19
IERC	LAIC3B4CB HPI-TO3-33CB

Short Circuit Protection

The BB3553 has internal current limiting set at 400mA to protect the output stage against transient overloads. Prolonged overloads can still potentially destroy the device, depending on heat sinking and ambient conditions. The LH0063 is capable of considerably higher peak currents because it does not have the internal current limiting, but it should be externally protected if even a momentary overload is possible.

Input Bias Current vs Input Voltage

The data sheet guarantee for input bias current and input resistance on both devices assumes an input voltage of zero volts. This is the most reasonable condition for small signal applications, but increases dramatically when the input signal swings negative. The curve of typical input current vs. input voltage illustrates the problem. In many applications, the situation can be improved by reducing the positive supply voltage.

TABLE 2. SOCKETS FOR LH0063/BB3553

MANUFACTURER	PART #	COMMENTS
Robinson Nugent, Inc.	0002011	Chassis or heat-sink mounted socket
Midland-Ross Hypertronics	450-3716-01-03-00 YSK0102-004	Low cost socket pins for PCB mounting. 8 socket pins are required to mount one device.

Hypertronics
16 Brent Dr.
Hudson, MA 01749
(617) 568-0451

IERC
135 W. Magnolia Bl.
Burbank, CA 91502
(818) 786-1182

Midland-Ross
Cambion Div.
445 Concord Ave.
Cambridge, MA 02238
(617) 491-5400

Robinson-Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(812) 945-0211

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

MAXIM
Power Operational Amplifier

General Description

The Maxim LH0101 Power Operational Amplifier delivers up to 5 Amp peak output current. Packaged in a rugged TO-3 case, the LH0101 combines the ease of use and performance of a FET input op amp with the power handling capabilities of a 5 Amp output stage. The output short circuit protection makes this device ideal for driving AC and DC motors, large capacitive loads, and electromagnetic actuators. The output stage virtually eliminates crossover distortion while using little quiescent power.

The LH0101 is a wideband amplifier, with a full power bandwidth of 300kHz and a gain bandwidth of 5MHz. To simplify connection to the LH0101, the output of Maxim's LH0101 is connected to both the case and to pin 4.

Features

- **Pin for Pin 2nd Source!**
- **5 Amp Peak, 2 Amp Continuous Output Current**
- **Virtually No Crossover Distortion**
- **300 kHz Power Bandwidth**
- **300 pA Input Bias Current**
- **10 V/μs Slew Rate**
- **5 MHz Gain Bandwidth**
- **2 μs Settling Time to 0.01%**
- **Adjustable Current Limit**

Applications

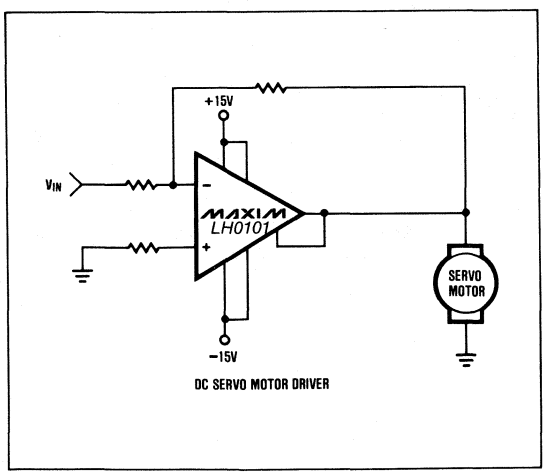
The LH0101 is well suited for applications requiring both standard op amp performance and high current output capability:

DC Motors
AC Motors
Actuators
Coaxial Cable Drivers
Programmable Power Supplies

Ordering Information

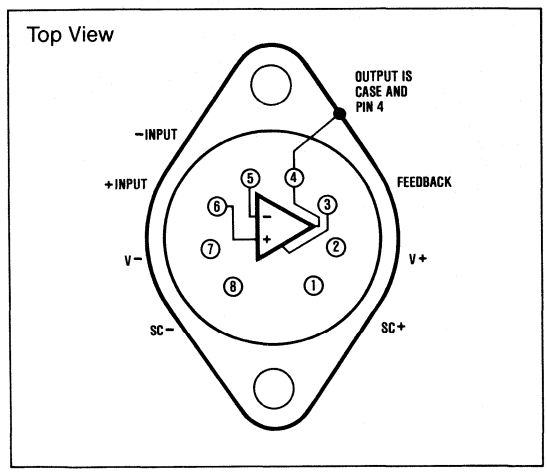
PART	TEMP. RANGE	PACKAGE
LH0101CK	-25°C to +85°C	8 Lead TO-3
LH0101K	-55°C to +125°C	8 Lead TO-3
LH0101ACK	-25°C to +85°C	8 Lead TO-3
LH0101AK	-55°C to +125°C	8 Lead TO-3

Typical Operating Circuit



DC SERVO MOTOR DRIVER

Pin Configuration



Power Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_S ..... ±22V
Power Dissipation at T_A = 25°C 5W
  Derate linearly at 25°C/W to zero at 150°C
Power Dissipation at T_C = 25°C 62W
  Derate linearly at 2°C/W to zero at 150°C
Differential Input Voltage, V_{IN} ..... ±40V but < $\pm V_S$
Input Voltage Range, V_{CM} ..... ±20V but < $\pm V_S$
Peak Output Current (50ms pulse) 5A
Output Short Circuit Duration (within rated power dissipation, R_{SC} = 0.35Ω, T_A = 25°C) ..... Continuous
Operating Temperature Range
  LH0101AC, LH0101C ..... -25°C to +85°C
  LH0101A, LH0101 ..... -55°C to +125°C
Storage Temperature ..... -65°C to +160°C
Maximum Junction Temperature ..... 150°C
Lead Temperature (Soldering, < 10 seconds) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C unless otherwise noted, see Note 1)

PARAMETER	SYMBOL	CONDITIONS		LH0101AC, LH0101A			LH0101C, LH0101			UNITS
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_{OS}	T_A = 25°C			1	3		5	10	mV
		$T_{MIN} \le T_A \le T_{MAX}$ (Note 4)				7			15	mV
Change in Input Offset Voltage with dissipated power	$\frac{\Delta V_{OS}}{\Delta P_D}$	(Note 2)			150			300		μV/W
Change in Input Offset Voltage with temperature	$\frac{\Delta V_{OS}}{\Delta T}$	V_{CM} = 0			10			10		μV/°C
Input Bias Current	I_B	T_A = 25°C				300			1000	pA
		$T_A \le T_{MAX}$ (Note 4)	LH0101C/AC			60			60	nA
			LH0101/A			300			1000	nA
Input Offset Current	I_{OS}	T_A = 25°C				75			250	pA
		$T_A \le T_{MAX}$ (Note 4)	LH0101C/AC			15			15	nA
			LH0101/A			75			250	nA
Large Signal Voltage Gain	A_{VOL}	V_O = ±10V, R_L = 10Ω		50	200		50	200		V/mV
Output Voltage Swing	V_O	R_{SC} = 0Ω, A_V = +1 (Note 3)	R_L = 100Ω	±11.7	±12.5		±11.7	±12.5		V
			R_L = 10Ω	±11	±11.6		±11	±11.6		V
			R_L = 5Ω	±10.5	±11		±10.5	±11		V
Common Mode Rejection Ratio	CMRR	ΔV_{IN} = ±10V		85	100		85	100		dB
Power Supply Rejection Ratio	PSRR	ΔV_S = ±5V to ±15V		85	100		85	100		dB
Quiescent Supply Current	I_S				28	35		28	35	mA

AC ELECTRICAL CHARACTERISTICS

(V_S = ±15V, T_A = 25°C, see Note 1)

PARAMETER	SYMBOL	CONDITIONS		LH0101AC, LH0101A			LH0101C, LH0101			UNITS
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Equivalent Input Noise Voltage	e_n	f = 1kHz			25			25		$nV/\sqrt{Hz}$
Input Capacitance	C_{IN}	f = 1MHz			3.0			3.0		pF
Power Bandwidth, -3dB		R_L = 10Ω	A_V = +1		300			300		kHz
Slew Rate (Note 4)	SR			7.5	10			10		V/μs
Small Signal Rise or Fall Time	t_r, t_f				200			200		ns
Small Signal Overshoot					10			10		%
Gain-Bandwidth Product (Note 4)	GBW	R_L = ∞		4.0	5.0			5.0		MHz
Large Signal Settling Time to 0.01%	t_s				2.0			2.0		μs
Total Harmonic Distortion	THD	P_O = 0.5W, f = 1kHz R_L = 10Ω			0.008			0.008		%

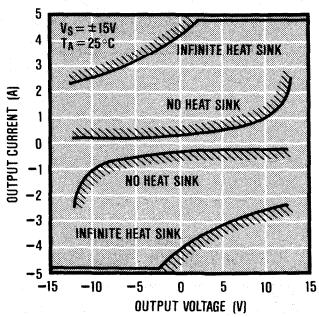
Note 1: Specification is at T_J = 25°C. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heat sinking. Accordingly, V_{OS} may change 0.5mV and I_B and I_{OS} will change significantly during warmup. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

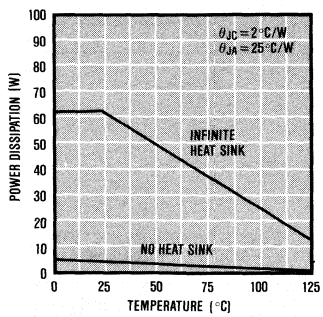
Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

Note 4: These parameters are sample tested to 10% LTPD.

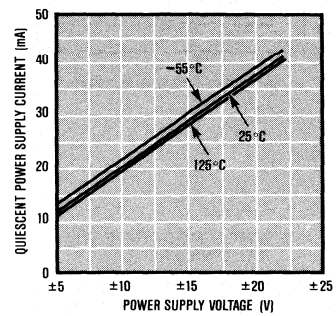
SAFE OPERATING AREA



MAXIMUM POWER DISSIPATION

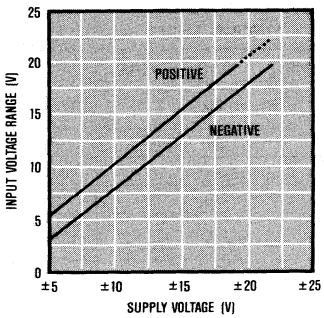


QUIESCENT POWER SUPPLY CURRENT

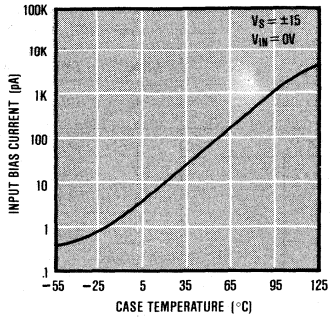


Power Operational Amplifier

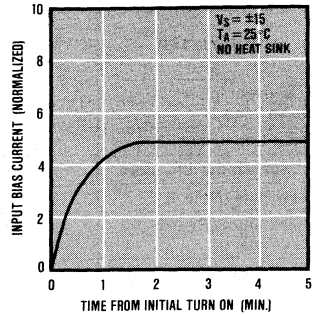
INPUT COMMON-MODE VOLTAGE RANGE



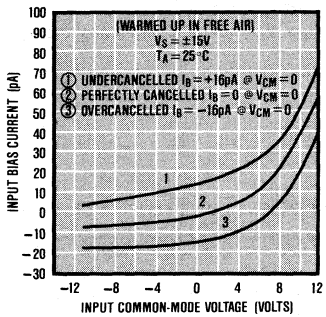
INPUT BIAS CURRENT



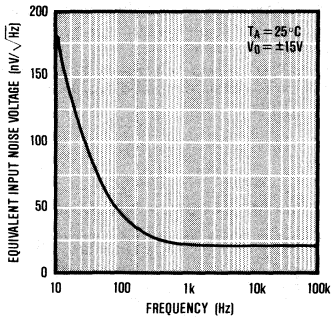
INPUT BIAS CURRENT AFTER WARM-UP



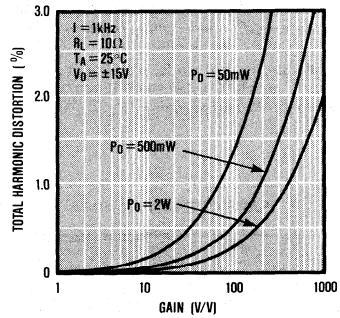
INPUT BIAS CURRENT VS. COMMON-MODE VOLTAGE



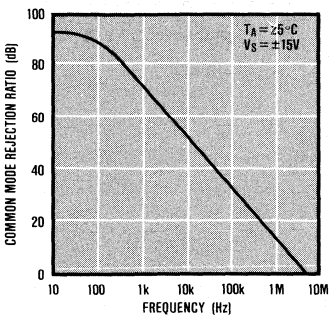
EQUIVALENT INPUT NOISE VOLTAGE



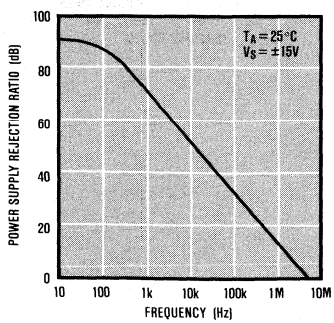
TOTAL HARMONIC DISTORTION VS. GAIN



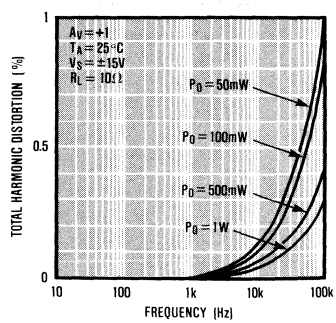
COMMON-MODE REJECTION RATIO VS. FREQUENCY



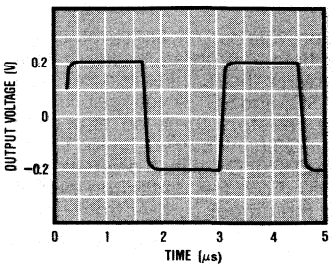
POWER SUPPLY REJECTION RATIO VS. FREQUENCY



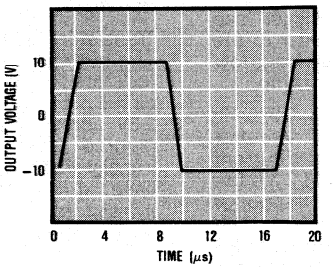
TOTAL HARMONIC DISTORTION VS. FREQUENCY



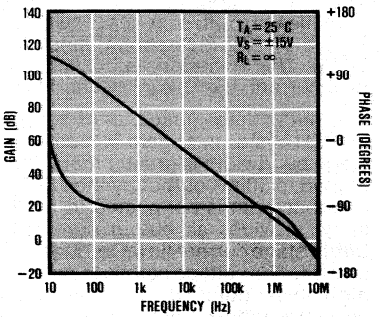
SMALL SIGNAL PULSE RESPONSE (NO LOAD)



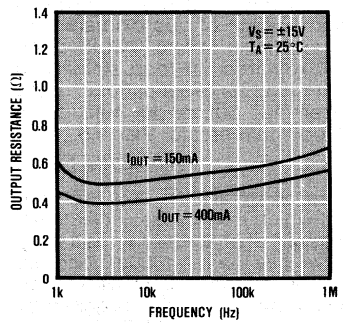
LARGE SIGNAL PULSE RESPONSE (R_L = 10Ω)



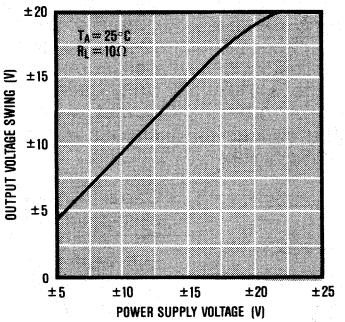
SMALL SIGNAL FREQUENCY RESPONSE (OPEN LOOP)



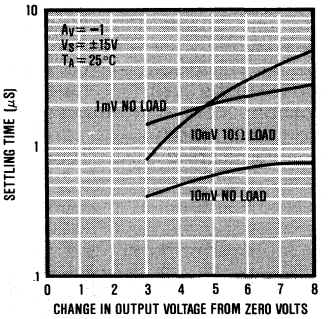
OPEN-LOOP OUTPUT RESISTANCE VS. FREQUENCY



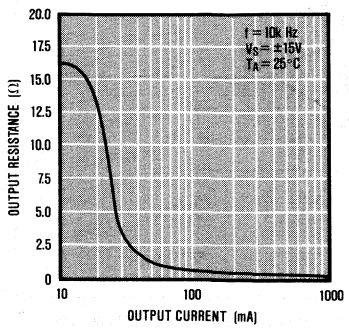
OUTPUT VOLTAGE SWING WITH SWING ENHANCEMENT



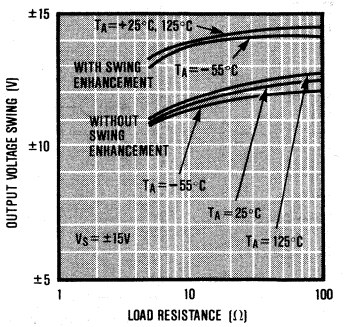
SETTING TIME



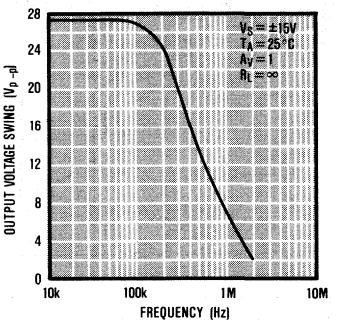
OPEN-LOOP OUTPUT RESISTANCE



OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



OUTPUT VOLTAGE SWING VS. FREQUENCY



Power Operational Amplifier

Detailed Description

The LH0101 consists of three stages: an operational amplifier, a buffer, and a power output stage, (see Figure 1). The operational amplifier is similar to the LF156. This operational amplifier was chosen for its low bias current, high slew rate, and fast settling time.

The buffer stage, made up of transistors Q3, Q5, Q10, and Q11, is a unity gain current amplifier. The buffer stage bandwidth is greater than 50MHz, and is current limited to 50mA output by the JFETs Q8 and Q7. If the Feedback pin is connected to the Output, the buffer stage provides all output current up to 25mA. The buffer stage current flows through the 50Ω resistors, R3 and R4. The voltage across these resistors turns on the high power output stage when the buffer stage output current is approximately 25mA. The buffer stage continues to supply current up to its 50mA current limit during the turn-on delay of the output stage. Only in driving low resistance or high capacitance loads at high frequencies will there be any noticeable distortion during the period when the output stage is turning on.

The high power output stage consists of the power darlingtons, Q1 and Q2, and the current limit protection circuit. The power darlington transistors are die attached directly to the case, minimizing thermal resistance. This electrically connects the collectors of Q1 and Q2 to the case, therefore the case is the LH0101 Output connection. The output of the Maxim LH0101 is also connected to pin 4. This additional output connection enables users to make all connections directly via a socket or printed circuit board, without having to make the output connection through heatsink mounting hardware.

Transistors Q6 and Q9 provide current limit protection. The current limit threshold is programmed by sense resistors connected between the supplies and the short circuit protection pins, SC^+ and SC^-. A voltage of about 0.6V across the sense resistors turns on either Q6 (source current limit) or Q9 (sink current limit). These transistors then turn on Q12 or Q4, which divert excess base current drive away from the darlington output transistors, preventing the output current from rising beyond the preset limit.

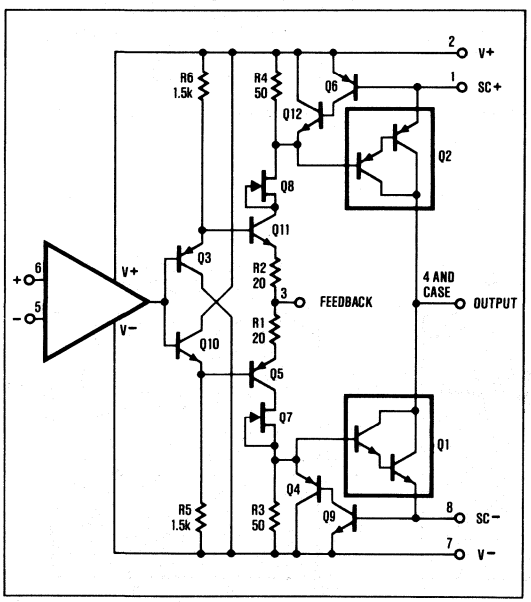


Figure. 1. Maxim LH0101 Schematic.

Application Hints

Output Swing Enhancement

When the Feedback terminal is directly connected to the Output, the buffer stage clips and limits the output voltage swing before the output stage saturates. The output swing is 11V to 12.5V with the Feedback terminal connected to the Output. The output swing can be increased by using the circuit of Figure 2. In this circuit the output stage operates with a gain of 1.5 and the output stage saturation voltage of approximately 1V limits the output voltage swing. The 0.01μF compensation capacitor is required for loop stability in unity gain non-inverting buffer applications using output swing enhancement, but is not needed in circuits with a closed loop gain greater than 1.5.

Capacitive Loads

Capacitive loads create an additional pole with the associated phase shift, which may cause oscillations. The LH0101 typically has 60° of phase margin as a unity gain buffer with no capacitive load. A 1000pF load will reduce this phase margin to 40° and 0.01μF will reduce it to only 22°. A phase margin of only 22° is generally considered unacceptably low and the LH0101 should

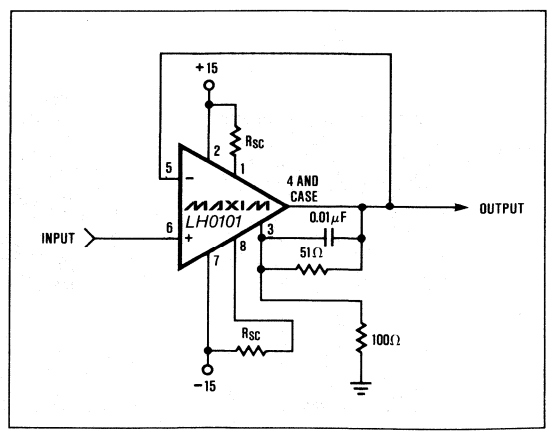


Figure 2. High Power Voltage Follower with Swing Enhancement.

be compensated as shown in Figure 3 when driving capacitive loads in the 0.01 μF range. Figure 4 shows an alternative method of compensation which can easily be used with the output swing enhancement circuit discussed below.

As with most amplifiers, there is a value of load capacitance above which oscillation will not occur. For the LH0101 this value is approximately 0.1 μF. The pole formed by the LH0101 output impedance and capacitive loads greater than 0.1 μF becomes the dominant pole and oscillation will not occur. In summary, if the load capacitance is less than 1000pF or greater than 0.1 μF the circuit should be stable, otherwise use the compensation techniques of Figure 3 or 4.

Inductive Loads

Inductive loads present three potential problems: inductive kickback or back EMF, stability, and safe operating area (SOA) violations. The LH0101 is suitable for driving inductive loads such as voice coil actuators and motors, but many circuits will require protection from the harmful effects of the energy stored in the inductor. The inductive kickback problem occurs when the power to the circuit is removed while high current is still flowing through the inductor. The back EMF or inductive kickback may have enough energy to destroy the LH0101 as current flows from the inductive load, through the output stage, back into the internal circuitry of the LH0101. The clamp diodes shown in Figure 5 will steer the inductive kickback currents directly to the power supplies, thus protecting the LH0101.

Some inductive loads, particularly those with high Q, may cause spurious oscillations. The damping circuit shown in Figure 6, a series combination of 10Ω and 0.01 μF or 0.1 μF, usually cures this type of problem.

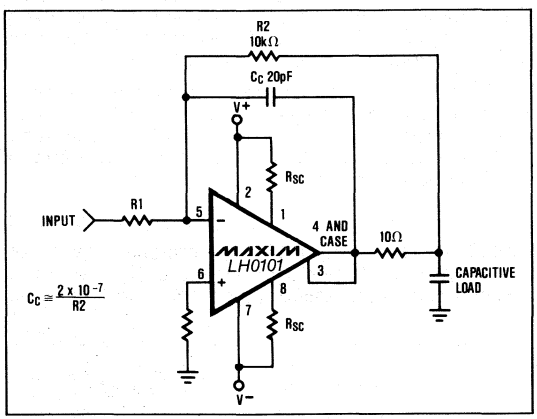


Figure 3. Compensation for Capacitive Load.

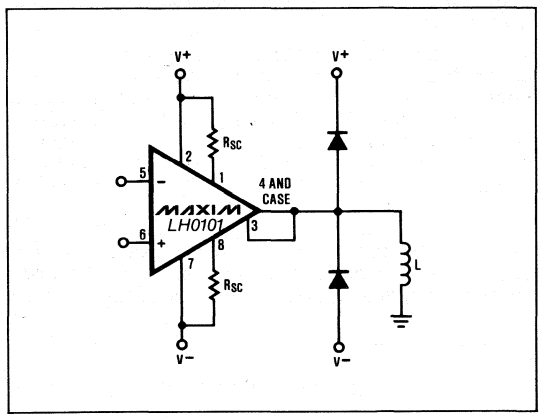


Figure 5. Back EMF Suppression.

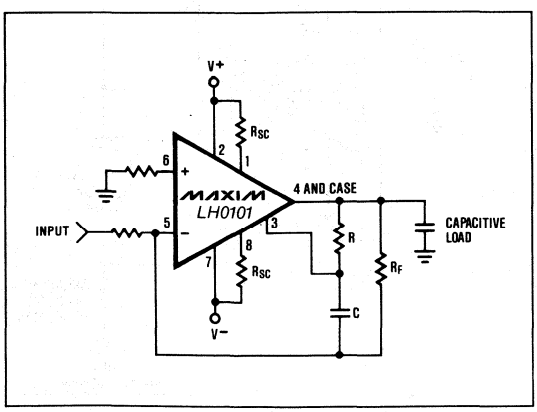


Figure 4. Alternate Compensation for Capacitive Load.

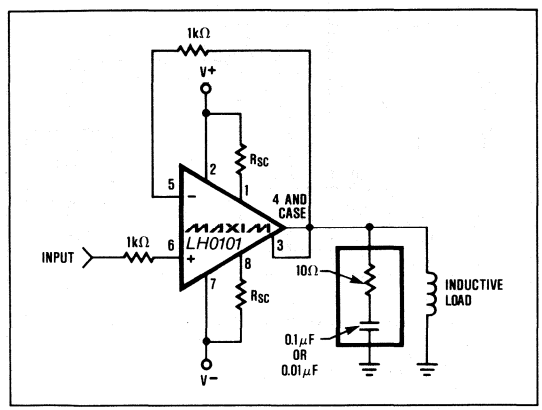


Figure 6. Damping of High Q Inductive Load.

Power Operational Amplifier

Printed Circuit Board Layout and Kelvin Connections or Remote Sensing

Printed circuit board traces which carry high currents must be carefully designed. High current traces must of course be wide enough to handle the current without excessive heating. A 0.030" wide trace on 2oz./ft^2 copper clad board will have a 10°C rise when carrying 3 Amp. Even when the printed circuit board traces are large enough to carry the current, the voltage drops may cause errors in the output. For example, a 0.030" wide trace on a 2oz. copper clad board will have a resistance of 10mΩ per inch of length and will have a voltage drop of 20mV/inch when carrying 2 Amp. Errors due to voltage drops can be avoided by using one trace or conductor for high current output connections and a second trace or conductor for the low current feedback sensing connection. Figure 7 shows the proper configuration of supply and feedback connections. The 470Ω resistor completes the feedback path if the remote sense connection is inadvertently disconnected.

In some cases signal ground and the power ground are connected together elsewhere and cannot be connected as shown in Figure 7. In this case the circuit of Figure 8 can be used. If $R_{SG}/R_{PG} = R_I/R_F$, voltage drops across R_G are turned into a common mode voltage at the input of the LH0101 and are rejected by the 100dB common mode rejection ratio (CMRR) of the LH0101.

Supply Bypassing

The LH0101 must be adequately bypassed to avoid oscillation and stability problems caused by the power supply impedance. The higher currents and lower impedance levels associated with the LH0101 require more bypassing than is normally required for lower power op amps. A 0.1μF ceramic capacitor in parallel with at least 47μF is recommended. The minimum acceptable bypassing is 0.01μF in parallel with 4.7μF between ground and each power supply.

Common Mode Voltage Range

While the common mode rejection ratio (CMRR) is guaranteed only over the ±10V input voltage range, the actual input common mode voltage range (CMVR) is typically -12V to +15.1V with ±15V power supplies.

Exceeding the negative common mode limit on either input will cause a phase reversal: if the inverting input exceeds the negative common mode limit the output will be forced low; if the non-inverting input exceeds the negative common mode limit the output will be forced high.

Exceeding the positive common mode limit on only one input will not cause a phase reversal. Exceeding either the positive or the negative common mode limit with both inputs will force the output high.

The LH0101 does not latch-up when the inputs exceed the common mode voltage range provided the absolute maximum ratings are not exceeded; normal operation resumes when the inputs return to within the common mode voltage range limits.

Input Protection

While the very low input bias current specification of the LH0101 might appear to eliminate the need for a bias compensation resistor at the non-inverting input,

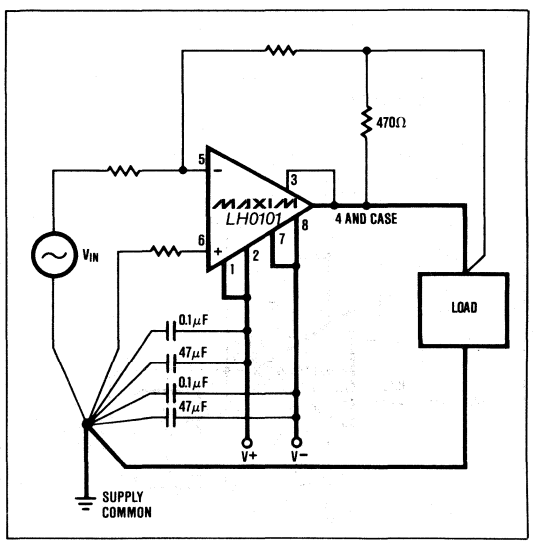


Figure 7. Power Supply Connections.

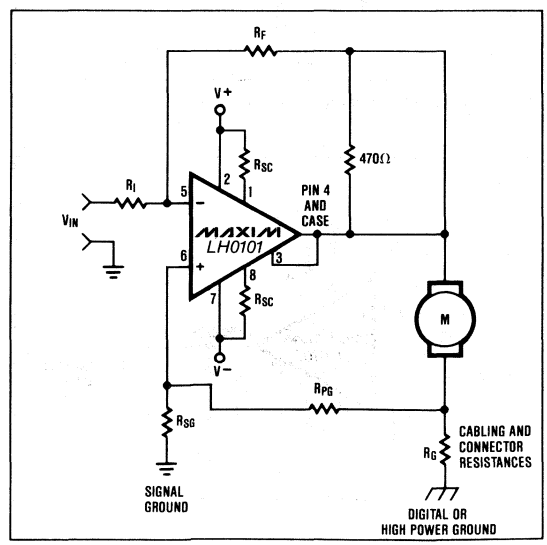


Figure 8. Correcting for Voltage Difference between Signal and Power Grounds.

the bias compensation resistor also protects this input. Direct connection of the inputs to ground should be avoided since excessive fault currents might flow if one of the power supplies were to be interrupted. A 1kΩ or greater resistor in series with the inputs will avoid this potential problem.

Heatsinks and Power Dissipation Limits

The maximum junction temperature of the LH0101 is 150°C. This is the basic limitation that, in conjunction with the thermal resistance, sets the maximum allowable power dissipation for the LH0101. Specifically,

$$P_{DISS(MAX)} = \frac{T_{J\,(MAX)} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

Where

$T_{J(MAX)}$ is the maximum allowable junction temperature of the LH0101, 150°C.

T_A is the ambient temperature.

θ_{JC} is the LH0101 junction to case thermal resistance, 2°C/W.

θ_{CS} is the thermal resistance between the LH0101 case and the heatsink in °C/W.

θ_{SA} is the thermal resistance from the heatsink to ambient.

The θ_{JC} of the LH0101 is typically 2°C/W; a conservative design should use a value of 2.5°C/W to allow for device-to-device variations in θ_{JC}. The actual power dissipation in a given application is the sum of the quiescent power dissipation (850mW typical with ±15V power supplies) and the power dissipation in the output transistors. The dissipation in the output transistors is the time average of the instantaneous product of the output current times the voltage difference between the output and the supply voltage.

Short Circuit Current Limiting

The source and sink current limits are individually set by the current sense resistors connected between the power supplies and the short circuit current limit pins, SC^+ and SC^-. Calculate the resistor values from the formula:

$$I_{SHORT\ CIRCUIT} = \frac{0.6V}{R_{SC}}$$

This equation is only an approximation, and it is not unusual for the actual current limit to vary as much as 25% from the expected value. The 0.6V in the above formula is the V_{BE} of Q6 and Q9, which may vary as much as 10% from device to device. This V_{BE} also has a temperature coefficient of about −2mV/°C. A second error source is the exact value of R_{SC}. Remember that R_{SC} includes all resistance between the power supply and the SC terminal, including printed circuit board trace resistance, solder joints, and if a socket is used, the socket contact resistance. Since R_{SC} may be as low as 0.12Ω, these extra resistances can be a significant fraction of the total R_{SC}. The power dissipation of the current limit resistor is:

$$P_{DISS} = \frac{(0.6V)^2}{R_{SC}\ (\text{in}\ \Omega)} = \frac{0.36}{R_{SC}}\ \text{Watts}$$

When the LH0101 is used without a heatsink, set the current limit to 250mA with 2.7Ω resistors for R_{SC}.

Safe Operating Area

The Safe Operating Area curve shown in the typical characteristics section must not be exceeded. This curve is for a case temperature of 25°C, and must be further derated for operation at elevated case temperatures.

There are two basic limits that must be observed; the maximum current limit and the maximum power dissipation limit. The SOA curve does not have any limits set by secondary breakdown in the output transistors, the power dissipation limit is reached before the transistors approach their secondary breakdown limits.

Table 1. HEATSINKS FOR LH0101

Manufacturer	Part #
Thermalloy	6002-19
IERC	LAIC3B4CB HPI-TO3-33CB

Table 2. SOCKETS FOR LH0101

Manufacturer	Part #	Comments
Robinson Nugent Inc.	0002011	Chassis or heatsink mounted socket
Midland-Ross	450-3716-01-03-00	Low cost socket pins for PCB mounting. 8 socket pins are required to mount one LH0101
Hypertronics	YSK0102-004	

Hypertronics
16 Brent Dr.
Hudson, MA 01749
(617) 568-0451

IERC
135 W. Magnolia Bl.
Burbank, CA 91502
(818) 786-1182

Midland-Ross
Cambion Div.
445 Concord Ave.
Cambridge, MA 02238
(617) 491-5400

Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
(812) 945-0211

Thermalloy
P.O. Box 34829
Dallas, TX 75234
(214) 243-4321

Power Operational Amplifier

Typical Applications

DC Servomotor Amplifiers

Figure 10 shows a voltage feedback DC servomotor amplifier. This type of control loop is normally used when the speed control is achieved by controlling the motor voltage. With the resistor values shown, the voltage at the motor will be $-5 \times V_{IN}$. The output voltage is sensed at the motor, therefore voltage drops in the cable between the LH0101 and the motor will not affect the voltage applied to the motor. The 10Ω resistor and 0.01μF capacitor may be required to prevent oscillations.

Figure 11 shows a current feedback DC servomotor amplifier. This type of control loop is normally used to develop a torque approximately proportional to the input voltage. Like Figure 9 this circuit delivers a constant current that is proportional to the input voltage.

Figure 12 combines both current and voltage feedback to achieve better open loop speed regulation than can be achieved by either Figure 10 or 11. The specific values of R_S, R_{FI} and R_{GI} are chosen to best approximate the Speed/Current/Torque characteristic of the motor. Capacitor C_C may be required for stability if the

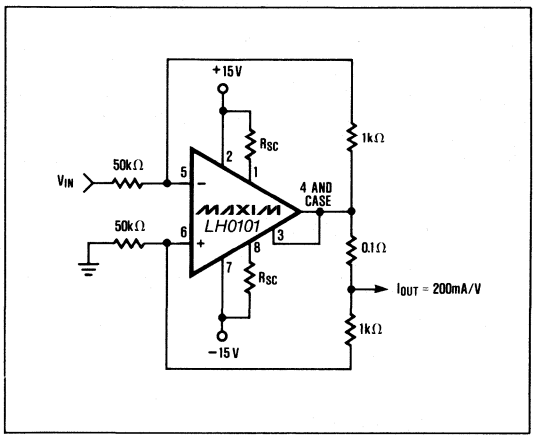


Figure 9. High Current Source/Sink.

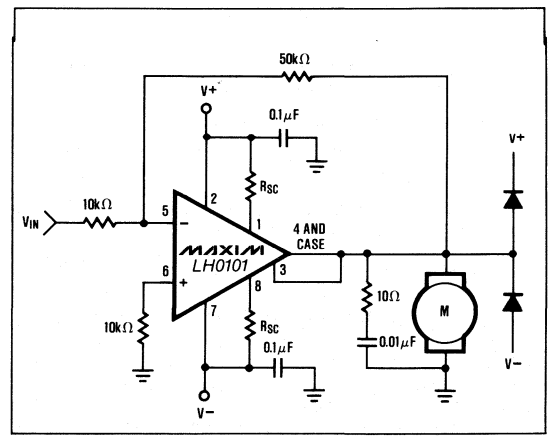


Figure 10. Servo Motor Amplifier.

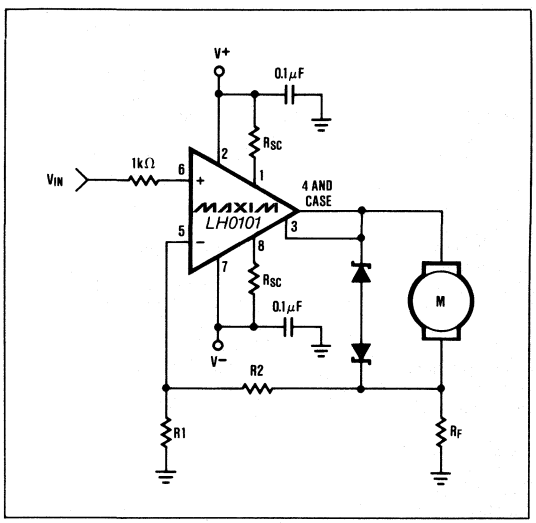


Figure 11. Torque Feedback Servo Motor Amplifier.

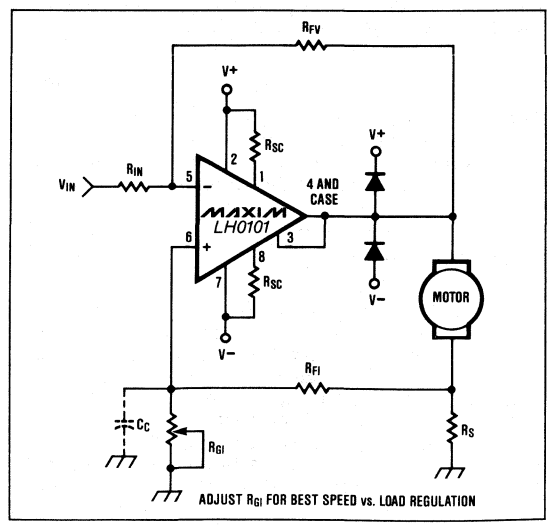


Figure 12. Constant Speed Motor Driver.

positive feedback is such that the motor speed increases with increased torque load.

These circuits will either source or sink current, depending on the polarity of the input voltage, and can drive DC motors in both directions.

Low Distortion Audio Amplifier

The hermetically packaged LH0101 is well suited for use as an audio amplifier for severe environments. Figure 13 shows two LH0101s used in a bridge audio power amplifier. The bridge configuration doubles the voltage that can be delivered to the load, in this case delivering 50V peak-peak to an 8Ω speaker. This means that a 40 Watts RMS can be delivered to the 8Ω speaker while using only ±18V power supplies. The harmonic distortion is a respectable 0.1%, which should suffice for all but the most demanding applications.

CRT Yoke Driver Circuit

The 300kHz power bandwidth and 5 Amp peak output current capability of the LH0101 make it well suited for CRT yoke driver circuits such as Figure 14. This circuit is basically a constant current source/sink with a transconductance of 435 mA/V (reciprocal of the 2.3Ω current sense resistor). The resistor R_{DAMP} lowers the Q of the inductive yoke; the value of R_{DAMP} is chosen empirically for the least distortion at the operating frequency. At low frequencies R_{DAMP} is not required.

DC Servomotor Phase Locked Loop

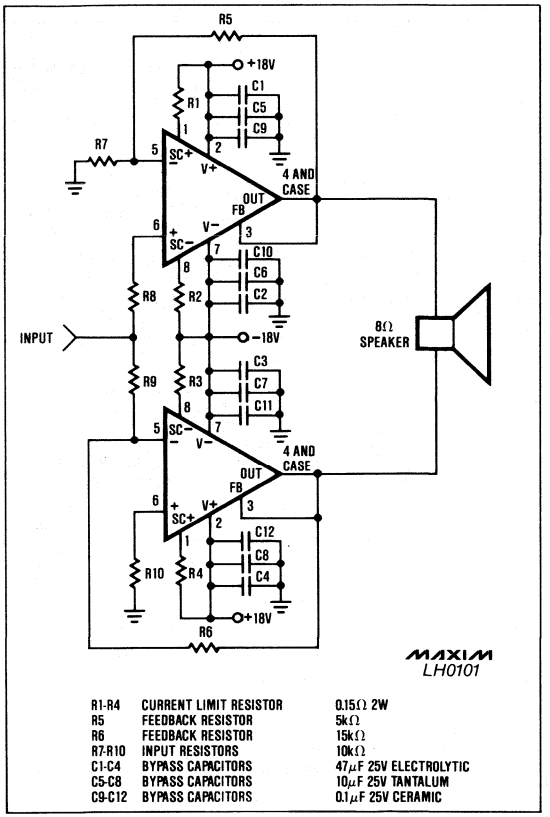
In the circuit of Figure 15, the shaft encoder produces 600 pulses per revolution. These pulses are compared to a reference frequency by the digital phase comparator of the CD4046. The output of the phase comparator passes through a low pass filter and drives the input of the LH0101. The LH0101 amplifies this signal and drives the DC servomotor. The phase-frequency comparator of the CD4046 increases or decreases the input voltage to the LH0101 until the shaft encoder output is the same frequency as the reference input.

$$\text{Motor Speed (in RPM)} = \frac{F_{IN} \times 60}{N}$$

Where F_{IN} is the frequency of the reference input and N is the number of shaft encoder pulses per revolution.

A single-pulse-per-revolution speed pickup can be used in place of the shaft encoder, but the PLL low pass filter time constant must be greatly increased.

Note that this circuit is similar to a standard phase locked loop except that the LH0101, the motor, and the shaft encoder replace the internal VCO of the CD4046. Unlike the VCO of the CD4046, the motor adds another pole to the system response and loop stability must be carefully analyzed, particularly if the motor and its load has significant inertia. As with most feedback systems, the loop will be stable when there is only one dominant pole. The loop filter time constant should preferably be at least 1 decade higher or lower than the constant of the motor and its load.



R1-R4	CURRENT LIMIT RESISTOR	0.15Ω 2W
R5	FEEDBACK RESISTOR	5kΩ
R6	FEEDBACK RESISTOR	15kΩ
R7-R10	INPUT RESISTORS	10kΩ
C1-C4	BYPASS CAPACITORS	47μF 25V ELECTROLYTIC
C5-C8	BYPASS CAPACITORS	10μF 25V TANTALUM
C9-C12	BYPASS CAPACITORS	0.1μF 25V CERAMIC

Figure 13. LH0101 Bridge Audio Power Amplifier.

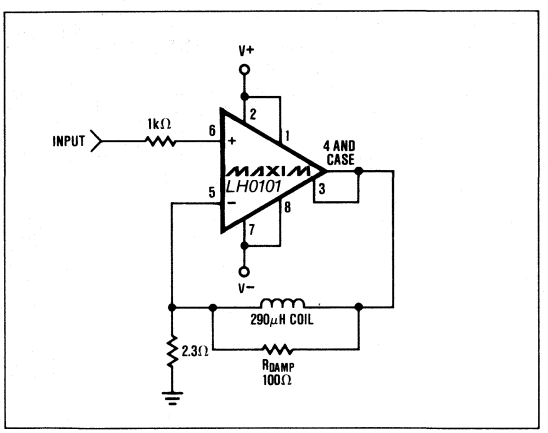


Figure 14. CRT Yoke Driver Circuit.

Power Operational Amplifier

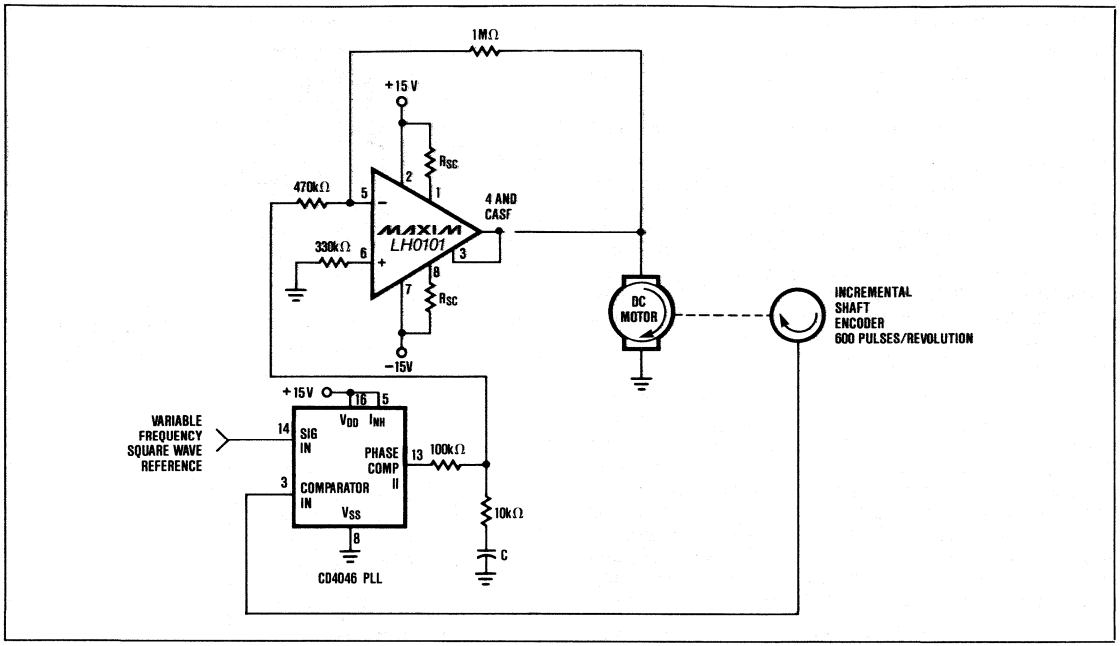
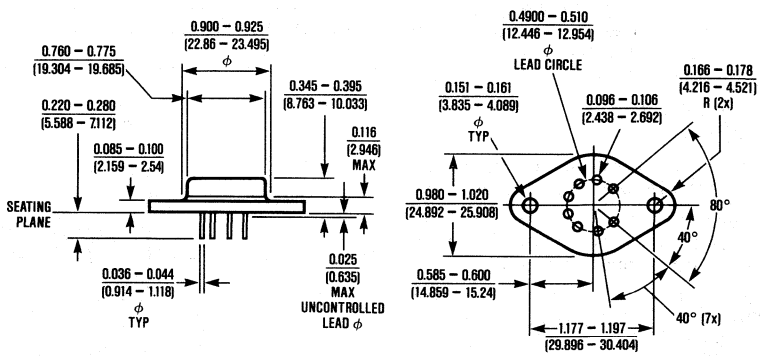


Figure 15. Servomotor Phase Locked Loop.

Package Information



8-Lead TO-3 Metal Can Package (K)

θ_{JA} = 25°C/W θ_{JC} = 2°C/W

3½ Digit A/D Converter With Display Hold

General Description

The Maxim ICL7116 and ICL7117 are 3½ digit monolithic analog to digital converters. They differ from the Maxim ICL7106 and ICL7107 in that the ICL7116 and ICL7117 have a Hold pin which makes it possible to hold or "freeze" a reading. These integrating A/D converters have very high input impedances and directly drive LCD (ICL7116) and LED (ICL7117) displays.

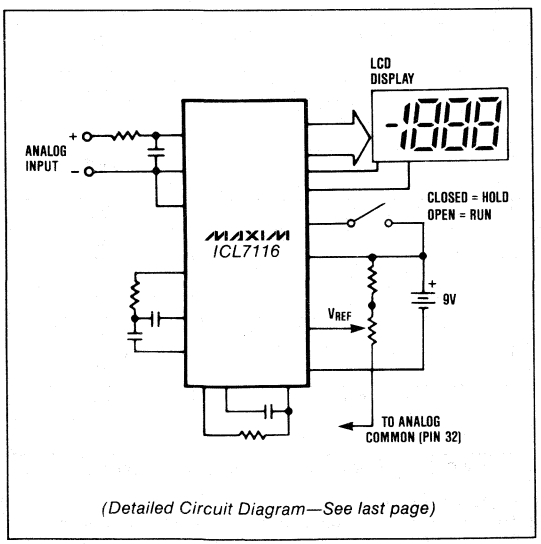
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input is particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7116 and ICL7117, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

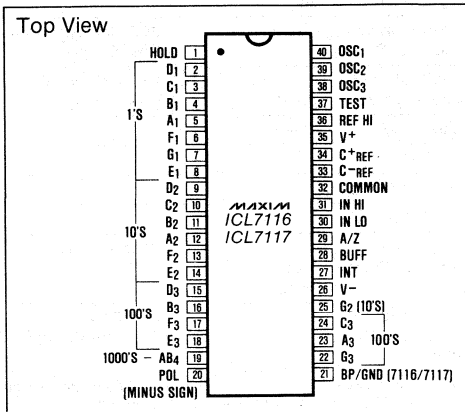
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **Hold Pin Allows Indefinite Display Hold**
- **Guaranteed First Reading Recovery from Overrange**
- **On Board Display Drive Capability — No External Circuitry Required: LCD-ICL7116, LED-ICL7117**
- **High Impedance CMOS Differential Inputs**
- **Low Noise (< 15μV p-p) Without Hysteresis or Overrange Hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7116CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7116CJL	0°C to +70°C	40 Lead Cerdip
ICL7116CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7116C/D	0°C to +70°C	Dice
ICL7117CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7117CJL	0°C to +70°C	40 Lead Cerdip
ICL7117CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7117C/D	0°C to +70°C	Dice

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7116, V^+ to V^- 15V
- ICL7117, V^+ to GND ..... +6V
- ICL7117, V^- to GND ..... -9V

Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7116 ..... Test to V^+
- ICL7117 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Cerdip Package 800mW
- Plastic Package 800mW

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 60 sec.) ..... +300°C

Note 1: Input voltage may exceed supply voltages, provided the input current is limited to ±100μA
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Postive and Negative Reading Near Full Scale	$-V_{IN} = +V_{IN} \cong$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation from Best Straight Line Fit)	Full Scale = 200mV or Full Scale = 2.000mV	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV	50		μV/V	
Noise (Pk-Pk Value Not Exceeded 95% of the Time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does Not Include LED Current for 7117)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current 7117 Only			0.6	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25Ω Between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25Ω Between Common & Pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 Only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 Only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4 4	5 5	6 6	V V
7117 Only (Except Pin 19) Segment Sinking Current (Pin 19 Only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{Clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.
Note 4: Refer to "Differential input" discussion. (See Maxim's ICL7106/ICL7107 data sheet)
Note 5: Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin1, to GROUND, pin 21.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

3½ Digit A/D Converter With Display Hold

- ♦ Guaranteed Overload Recovery Time
- ♦ Significantly Improved ESD Protection (Note 8)
- ♦ Low Noise
- ♦ Key Parameters Guaranteed Over Temperature
- ♦ Negligible Hysteresis
- ♦ Maxim Quality and Reliability
- ♦ Increased Maximum Rating for Input Current (Note 9)

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C, f_{CLOCK} = 48kHz; test circuit - Figure 1 (ICL7116), Figure 2 (ICL7117) unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 7)	-000.0	±000.0	+000.0	Digital Reading
	0°C ≤ T_A ≤ 70°C (Note 11)	**-000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF} = 100mV				
	T_A = 25°C (Note 7)	999	999/1000	1000	Digital Reading
	0°C ≤ T_A ≤ 70°C (Note 11)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in Reading for Equal Postive and Negative Reading Near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV				
	T_A = 25°C (Note 7)	-1	±0.2	+1	Counts
	0°C ≤ T_A ≤ 70°C (Note 11)		±0.2		
Linearity (Max. Deviation from Best Straight Line Fit)	Full Scale = 200mV or Full Scale = 2.000mV	-1	±0.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk Value Not Exceeded 95% of the Time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0V, T_A = 25°C (Note 7)		1	10	pA
	0°C ≤ T_A ≤ 70°C		**20**	**200**	
Zero Reading Drift	V_{IN} = 0V 0°C ≤ T_A ≤ 70°C (Note 7)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does Not Include LED Current for 7117)	V_{IN} = 0V		0.8	1.8	mA
	T_A = 25°C				
	0°C ≤ T_A ≤ 70°C			**2**	
V^- Supply Current 7117 Only			0.6	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25kΩ Between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25kΩ Between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 Only)				TEST +1.5	V
V_{IL}, Pin 1 (7117 Only)				GND +1.5	V
V_{IH}, Pin 1 (Both)		V^+ -1.5			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V	4	5	6	V
7117 Only (Except Pin 19) Segment Sinking Current	V^+ = 5.0V	5	8.0		mA
(Pin 19 Only)	Segment Voltage = 3V	10	16		mA
7116 Only — Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 10)	**V_{IN} changing from ±10V to 0V**		**0**	**1**	Measuement Cycles

Note 7: Test condition is V_{IN} applied between pins IN-HI and IN-LO. i.e., 1MΩ resistor in Figures 1 and 2.
Note 8: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per MIL. Std. 883C, Method 3015.2)
Note 9: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on the adjacent page).
Note 10: Number of measurement cycles for display to give accurate reading.
Note 11: 1MΩ resistor is removed in Figures 1 and 2.

3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim ICL7116 and ICL7117 3½ digit A/D converter are similar to the Maxim ICL7106 and ICL7107, except for the addition of a Hold pin. For a detailed product description, package dimensions, and applications information (other than the operation of the Hold pin described below) refer to Maxim's ICL7106 and ICL7107 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test (ICL7116) or V^+ and Ground (ICL7117). The ICL7116/7117 continuously performs conversions, independent of the Hold input. When the Hold input is connected to V^+, however, the display latch pulse is inhibited, and the the display latches are not updated. The Hold input has a 70 kilohm pulldown resistor to Test (ICL7116) or Ground (ICL7117) and the Hold input will be pulled low if it is left open. When Hold is low the ICL7116/ICL7117 updates the display at the end of each conversion. The Hold input is CMOS compatible, and can also be driven by a switch connected to V^+ (Figure 1 and 2) or by a PNP transistor.

Unlike the ICL7106 and the ICL7107, the ICL7116 and ICL7117 do not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

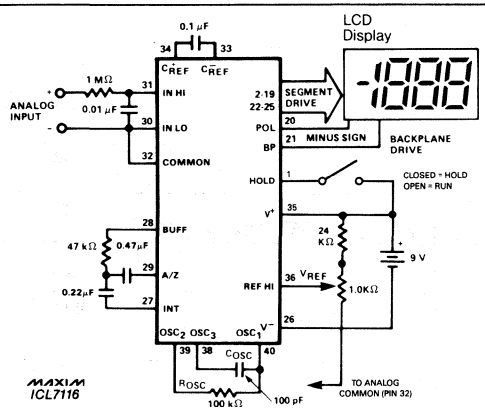


Figure 1. Maxim ICL7116 Typical Operating Circuit, 200mV Reference

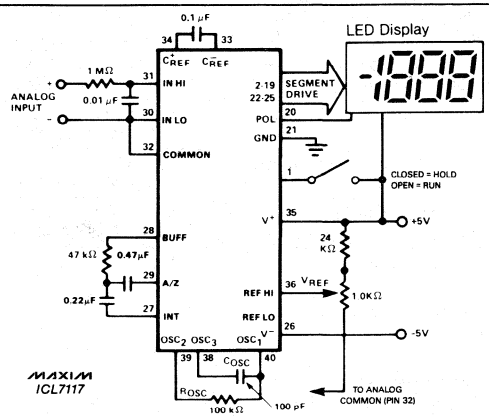
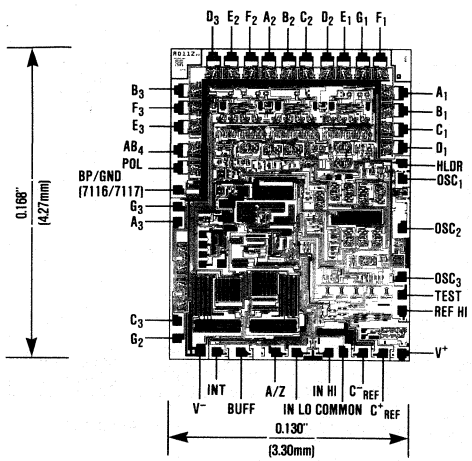
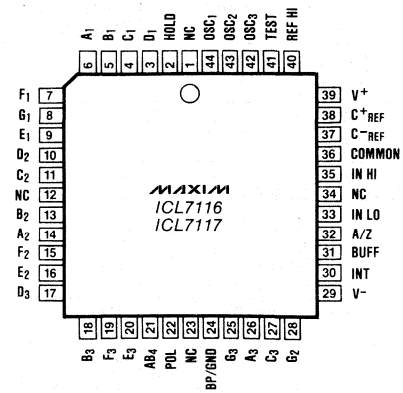


Figure 2. Maxim ICL7117 Typical Operating Circuit, 200mV Reference

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7137 is a monolithic analog to digital converter with all the necessary active devices to directly interface with a light emitting diode (LED) display. Excluding the LED display current, the ICL7137 supply current is under 200μA, making it suitable for battery operation.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7137 eliminates overrange hangover and hysteresis effects. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

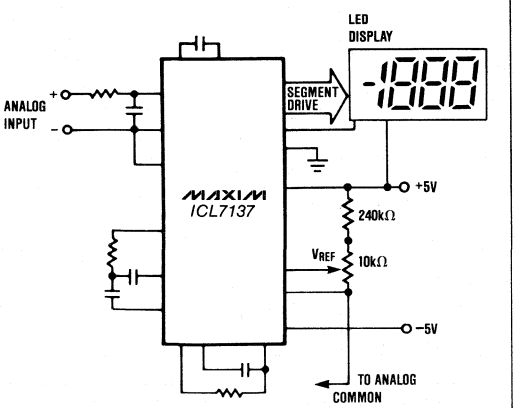
Features

- **Improved 2nd Source! (see 3rd page for "Maxim Advantage™")**
- **Guaranteed first reading recovery from overrange**
- **Zero Input Gives Zero Reading**
- **Drives LED Displays Directly**
- **Low Noise (15μV p-p) without hysteresis or overrange hangover**
- **True Differential Reference and Input**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7137CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7137CJL	0°C to +70°C	40 Lead CERDIP
ICL7137CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7137C/D	0°C to +70°C	Dice

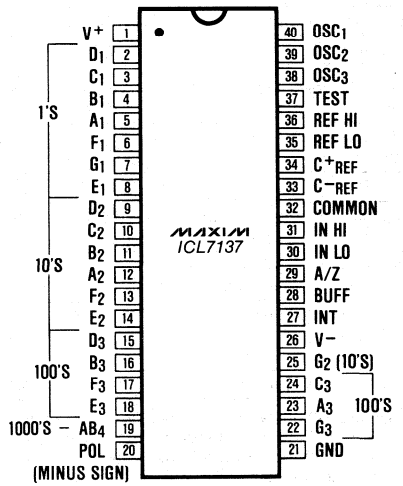
Typical Operating Circuit



(Detailed Circuit Diagram—See last page)

Pin Configuration

Top View



See last page for Plastic Chip Carrier Pin Configuration

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... -9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near full scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0° < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply Current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.6	3.0	3.2	V
Temp. Coeff. of Analog COMMON (with respect to Positive Supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Segment Sinking Current (Except Pin 19) (Pin 19 only)	V^+ = 5.0V Segment Voltage = 3V	5 10	8.0 16		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at T_A=25°C, f_{CLOCK}=16kHz and are tested in the circuit of Figure 1.
Note 4: Refer to "Differential Input" discussion in the ICL7136 data sheet.
Note 5: 48kHz oscillator, Figure 2, increases current by 35μA (typ).
Note 6: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

Low Power, 3½ Digit A/D Converter

- **Low Noise**
- **Key Parameters Guaranteed Over Temperature**
- **Guaranteed Overload Recovery Time**
- **Negligible Hysteresis**
- **Increased Maximum Rating for Input Current (Note 8)**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 7)**

ABSOLUTE MAXIMUM RATINGS

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

Specifications below satisfy or exceed all "tested" parameters on adjacent page.
(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1 unless noted.)

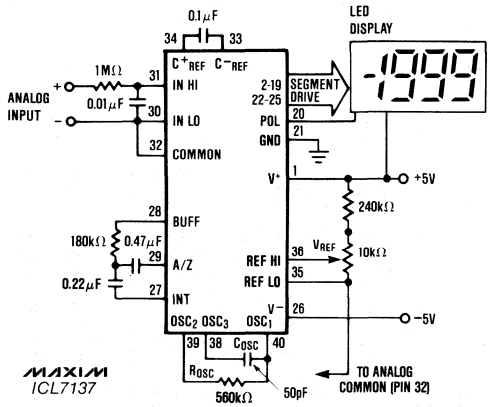
PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV				
	T_A = 25°C (Note 9)	-000.0	±000.0	+000.0	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**-000.0**	**±000.0**	**+000.0**	
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV				
	T_A = 25°C (Note 9)	999	999/1000	1000	Digital Reading
	0° ≤ T_A ≤ 70°C (Note 10)	**998**	**999/1000**	**1001**	
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	-V_{IN} = +V_{IN} ≅ 200mV				
	T_A = 25°C (Note 9)	-1	±0.2	+1	Counts
	0° ≤ T_A ≤ +70°C (Note 10)		±0.2		
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio	**V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV**	**-100**	**±30**	**+100**	μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Input Leakage Current	V_{IN} = 0,				
	T_A = 25°C (Note 9)		1	10	pA
	0° ≤ T_A ≤ +70°C			**200**	
Zero Reading Drift	V_{IN} = 0V, 0° ≤ T_A ≤ 70°C (Note 9)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C)(Note 9)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0V				
	T_A = 25°C		60	200	μA
	0° ≤ T_A ≤ 70°C			**240**	
V^- Supply Current	**V_{IN} = 0V,**		**60**	**200**	μA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Segment Sinking Current (Except Pin 19)	V^+ = 5.0V Segment Voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
Test Pin Voltage	**With Respect to V^+**	**4**	**5**	**6**	V
Overload Recovery Time (Note 11)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015.2)
Note 8: Input voltages may exceed the supply voltage provided the input current is limited to ±1mA (This revises Note 1 on adjacent page).
Note 9: Test condition is V_{IN} applied between the "Analog Input" pins (Figure 1).
Note 10: 1MΩ resistor is removed in Figures 1 and 2.
Note 11: Number of measurement cycles for display to give accurate reading.

Low Power, 3½ Digit A/D Converter

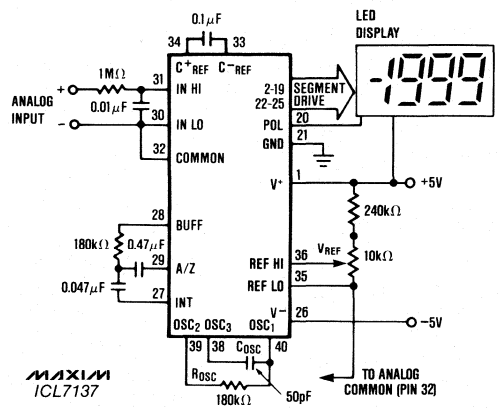
Detailed Description

The Maxim ICL7137 3½ digit A/D converter is similar to the Maxim ICL7136 except for the LED segment driver outputs, and is similar to the ICL7107 except for much reduced power supply currents (exclusive of the LED currents.) For a detailed product description, component value selection, and package dimensions, refer to Maxim's ICL7136 data sheets; for applications information refer to Maxim's ICL7107 data sheets.



FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

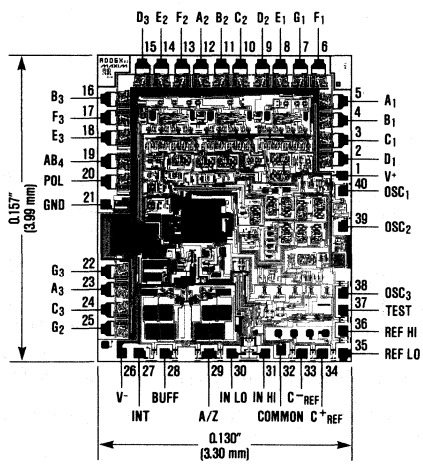
Figure 1. Maxim ICL7137 Typical Operating Circuit Clock Frequency 16kHz (1 reading/sec)



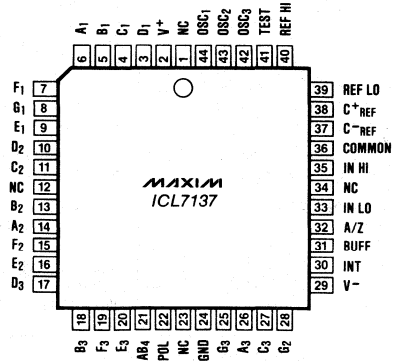
FULL SCALE INPUT	V_{REF}
200.0 mV	100.0mV

Figure 2. Maxim ICL7137 Typical Operating Circuit Clock Frequency 48kHz (3 reading/sec)

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

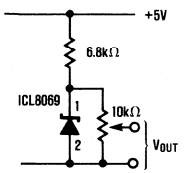
General Description

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Maxim's ICL8069 also features excellent stability (freedom from oscillation) for all capacitance loads from zero to greater than 50μF.

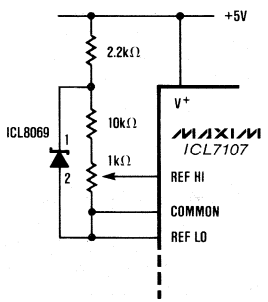
Applications

Analog to Digital Converters
Digital to Analog Converters
Threshold Detectors
Voltage Regulators
Portable Instruments

Typical Operating Circuits



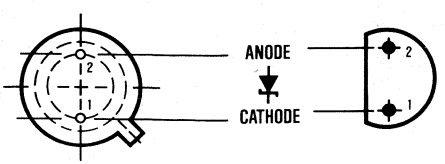
(a) Simple Reference (1.2 Volts or Less)



(b) Double Regulated 100mV Reference for ICL7107 One-Chip DPM Circuit.

Pin Configuration

Bottom View



TO-52 | TO-92 Plastic

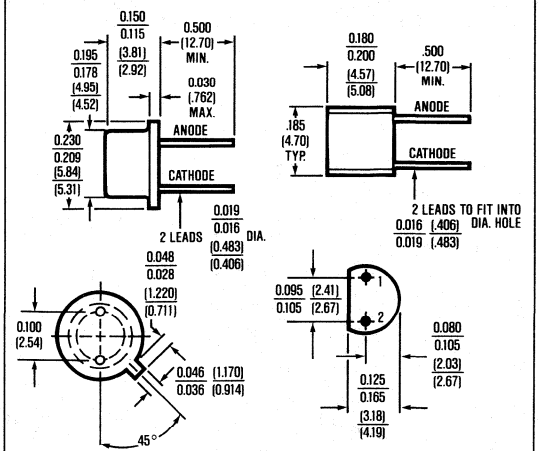
Features

- **Temperature Coefficient Guaranteed to 10ppm/°C Max.**
- **Low Bias Current . . . 50 μA Min.**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

Ordering Information

PART	TEMP. STABILITY	TEMP. RANGE
TO-92 Plastic:		
ICL8069CCZQ2	0.005%/°C	0°C to +70°C
ICL8069DCZQ2	0.01%/°C	0°C to +70°C
TO-52 Can:		
ICL8069ACSQ2	0.001%/°C	0°C to +70°C
ICL8069BCSQ2	0.0025%/°C	0°C to +70°C
ICL8069CCSQ2	0.005%/°C	0°C to +70°C
ICL8069DCSQ2	0.01%/°C	0°C to +70°C
ICL8069CMSQ2	0.005%/°C	-55°C to +125°C
ICL8069DMSQ2	0.01%/°C	-55°C to +125°C

Package Information



2 Lead TO-52 Can (SQ) | 2 Lead TO-92 Plastic (ZQ)

Low Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 1
Forward Current 10mA
Reverse Current 10mA
Power Dissipation .... Limited by Max Forward/Reverse Current
Storage Temperature Range ..... -65°C to +150°C

Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... -55°C to +125°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(@ 25°C unless otherwise noted)

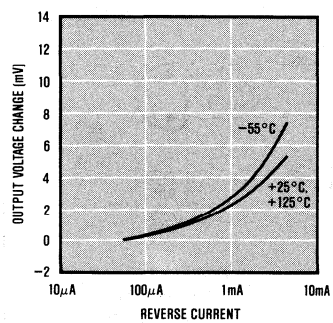
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	I_R = 500μA	1.20	1.23	1.25	V
Reverse Breakdown Voltage Change	50μA ≤ I_R ≤ 5mA		15	20	mV
Reverse Dynamic Impedance	I_R = 50μA I_R = 500μA		1 0.6	2 2	Ω
Forward Voltage Drop	I_F = 500μA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500μA		5		μV
Breakdown Voltage Temperature Coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	I_R = 500μA T_A = Operating Temperature Range (Note 2)			 .001 .0025 .005 .01	%/°C
Reverse Current Range		.050		5	mA

Note 1: In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.

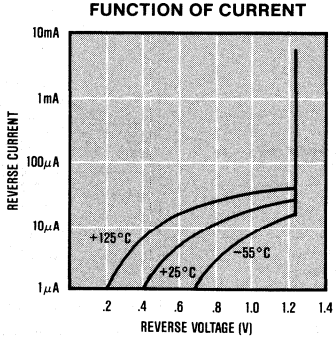
Note 2: For the military part, measurements are made at 25°C, -55°C, and 125°C. The unit is then classified as a function of the worst case T.C. from 25°C to -55°C, or 25°C to 125°C.

Typical Operating Characteristics

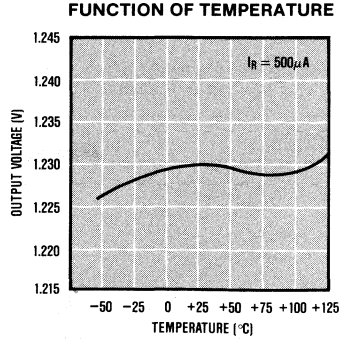
VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



REVERSE VOLTAGE AS A FUNCTION OF CURRENT



REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



MAXIM
4 Digit (LED) Presettable Up/Down Counter

General Description

The Maxim ICM7217 family of 4 digit presettable up/down counters contain a 4 digit, 7 segment LED display driver and a presettable comparison (predetermining) register. The counter and comparison register can be preset using either thumbwheel switches, jumpers, or external digital logic.

The ICM7217 (common anode) and ICM7217A (common cathode) are decade counters with a maximum count of 9999. The ICM7217B (common anode) and ICM7217C (common cathode) are modulo 60 counters intended for hours/minutes or minute/seconds timing applications, and have a maximum count of 5959.

These devices also provide multiplexed BCD outputs, a Carry/Borrow output allowing ICM7217s to be cascaded, a Zero output which indicates when the count is equal to zero, and an Equal output which indicates when the count is equal to the value contained in the comparison register. The ICM7217 also has a Reset input and a display latch with store input.

Applications

The Maxim ICM7217 significantly reduces the number of components required in many timing, counting and frequency counter applications.

Typical applications include:

Predetermining Batch Counter
Tachometer
Over/Under Speed Detector
Count Down/Elapsed Timer
Unit Counter
Frequency Counter

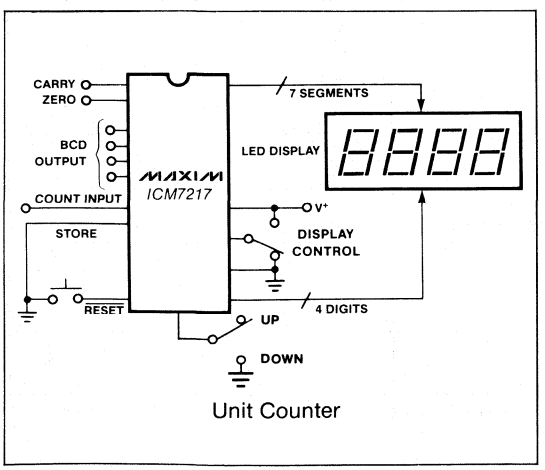
Features

- **Pin for Pin Second Source!**
- **4 Digit Up/Down Counter**
- **Directly Drives LED Display**
- **Presettable Counter and Compare Register**
- **Interfaces with Thumbwheel Switches or Digital Logic**
- **Can Be Cascaded**
- **Multiplexed BCD I/O**
- **Up/Down, Store and Reset Inputs**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7217IJI	-20°C to +85°C	28 Lead CERDIP
ICM7217IPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7217CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7217CIPI	-20°C to +85°C	28 Lead Plastic DIP

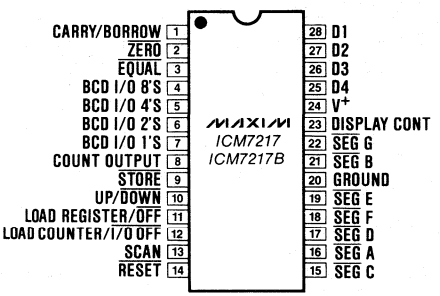
Typical Operating Circuit



Unit Counter

Pin Configuration

Top View



4 Digit (LED) Presettable Up/Down Counter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 500mA
Power Dissipation
28 Pin CERDIP 1.0W
derate 25mW/°C above 50°C
28 Pin Plastic (copper leadframe) 1.0W
derate 25mW/°C above 50°C

Temperature Range
Operating ..... -20°C to +85°C
Plastic Chip Carrier (Quad) Package (Q) ..... 0°C to +70°C
Storage ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C
Segment Output Current 100mA
Input Voltage (any terminal) (Note 1) ..... -0.3V to (V^+ +0.3V)

Note 1: The maximum input voltage may be exceeded if the maximum input current is limited to 1mA.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (Lowest Power Mode)	I^+ (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 2)		350	500	µA
Supply Current OPERATING	I^+_{ON}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+		4.5	5	5.5	V
Digit Driver Output Current	I_{DIG}	Common Anode, V_{OUT} = V^+ - 2.0V	140	200		mA peak
SEGment Driver Output Current	I_{SEG}	Common Anode, V_{OUT} = +1.5V	-20	-30		mA peak
Digit Driver Output Current	I_{DIG}	Common Cathode, V_{OUT} = +1.0	-50	-70		mA peak
SEGment Driver Output Current	I_{SEG}	Common Cathode, V_{OUT} = V^+ - 2V	10	12.5		mA peak
Digit and Segment Leakage Current	I_{LK}	LR Low	-100		+100	µA
ST, RS, UP/DN Input Low Voltage	V_{IL}				0.8	V
ST, RS, UP/DN Input High Voltage	V_{IH}		2.4			V
ST, RS, UP/DN Input Pullup Current	I_P	V_{OUT} = V^+ -2V (Note 2)	5	25	100	µA
Three Level Input Voltages Input High Input Floating Input Low	 V_{INH} V_{INF} V_{INL}	LR, LC, DC, V^+ = 5V	 4.2 2.0		 2.7 0.8	V
Three Level Impedance	Z_{IN}			100		kΩ
BCD I/O Input High Voltage	V_{BIH}	Common Anode V^+ = 5.0V	1.8			V
		Common Cathode V^+ = 5.0V	V^+ -0.6			V
BCD I/O Input Low Voltage	V_{BIL}	Common Anode V^+ = 5.0V			0.8	V
		Common Cathode V^+ = 5.0V			V^+ -1.8	V
BCD I/O Pullup Current	V_{BPU}	Common Cathode V_{IN} = V^+ - 2V (Note 2)	5	25	300	µA
BCD I/O Pulldown Current	V_{BPD}	Common Anode V_{IN} = +1.3V (Note 2)	5	25	300	µA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output High Current	I_{BOH}	V_{OH} = V^+ - 1.5V	1			mA
BCD I/O, CARRY/BORROW, ZERO, EQUAL Outputs Output Low Current	I_{BOL}	V_{OH} = +0.4V	-2			mA

Note 2: The Up/Down, Store, Reset and BCD I/O as inputs have pullup or pulldown devices which typically draw 50µA each when connected to the opposite supply.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C, test circuit, display diode drop = 1.7V, unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Count Input Frequency	f_{IN}	V^+ = 5V ± 10%, -20°C < T_A < +70°C	0	5	2	MHz
Count Input Threshold	V_{TH}	V^+ = 5V	0.8	2	3.5	V
Count Input Hysteresis	V_{HYS}	V^+ = 5V		0.5		V
Count Input Leakage	I_{IN}		-1		+1	µA
Display Multiplex Rate	f_{MUX}	Not Loading	100	625		Hz
		Loading	200	—	5000	
Display Scan Oscillator Frequency	f_{DS}	Free-running (SCAN Terminal Open Circuit)		2.5		kHz
Interdigit Blanking Time	t_{idb}		750	3000		ns
Operating Temperature Range	T_A	Industrial Temperature Range	-20		+85	°C

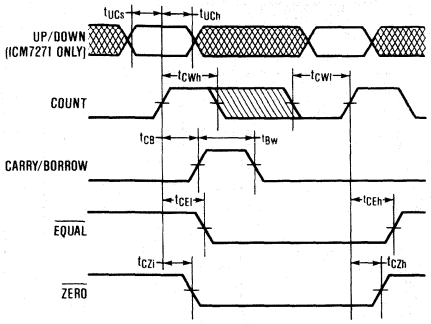
Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
24	24	V^+	Positive Power Supply. 5V ± 10%
20	19	GROUND	Ground.
28,27,26,25	18,17,16,15	D1,D2,D3,D4	These Digit Drive outputs directly drive the anodes (ICM7217 and ICM7217B) or the cathodes (ICM7217A and ICM7217C) of seven segment LED displays. D1 is the rightmost or least significant digit.
16,21,15,17, 19,18,22	23,27,25,28 22,26,21	Segments A-G	These Segment Drive outputs directly drive 7 segment LED displays. Current limiting resistors are NOT required.
7,6,5,4	7,6,5,4	BCD I/O 1,2,4,8	During normal operation these pins are BCD outputs, whose data corresponds to the count latched into the Store register. The data is multiplexed, digit by digit, going from the most significant digit (1000's) to the least significant digit (1's). The BCD data is valid approximately 6µs before the leading edge of each digit (rising edge of ICM7217/B digit outputs, falling edge of ICM7217A/C common Cathode outputs). During Load Counter and Load Register operations, the BCD I/O pins are inputs. BCD input data is latched by the trailing edge each digit period during Load Counter and Load register operations. The BCD input voltage levels are skewed to allow the use of thumbwheel switches connected to the digit driver to load BCD data. A positive voltage level is an input logic zero for the ICM7217A/C common cathode versions.
8	8	COUNT	Positive-going transitions of the COUNT input increment or decrement the counter, except when RESET is low or a load counter operation is in progress. The COUNT input is compatible with CMOS. TTL compatibility can be ensured by using a 4.7 kilohm pullup resistor on the TTL output. The COUNT input has 500mV of hysteresis, allowing the use of slow risetime input signals.
9	9	STORE	When STORE is low, the counter's contents appear at the LED digit and segment outputs, and at the BCD outputs. When STORE goes high, the current count is latched into the display latch, and that latched data appears at the LED drive and BCD outputs. Store has an internal 25µA pullup.
10	10	UP/DOWN	The counter counts up with each rising edge of Count when UP/DOWN is high. Conversely, the counter decrements with each rising edge of Count when UP/DOWN is low. UP/DOWN must be set up 300 nanoseconds before the rising edge of Count, and must be held stable for 750 nanoseconds after the rising edge of Count. Transitions on UP/DOWN during the 750 nanoseconds after the rising edge of Count may erroneously increment or decrement the upper counter stages.

4 Digit (LED) Presettable Up/Down Counter

Pin Descriptions

PIN NUMBER		PIN NAME	FUNCTION
COMMON ANODE ICM7217 ICM7271B	COMMON CATHODE ICM7217A ICM7217C		
14	14	RESET	Driving RESET low resets the counter to 0000. RESET does not clear the display latch unless both RESET and STORE are low. Since the RESET operation is performed by placing 0 on the internal BCD data bus and presetting all four counter stages, simultaneous RESET and Load register operations will load 0000 into the comparison registers. To avoid erroneous loading of zeroes into the comparison register, do not take RESET low unless LOAD REGISTER has been low or floating for at least 5 milliseconds. The RESET input has an internal 25μA pullup, but it should be actively driven or pulled up with an external 4.7 kilohm when the ICM7217 is used in electrically noisy environments.
1	1	CARRY/BORROW	The CARRY/BORROW output is a short positive going pulse (typically 1μs long) that occurs at the 9999 to 0000 transition when counting up, and the 0000 to 9999 transition when counting down. The CARRY/BORROW output is used to drive the COUNT input of a second ICM7217 in an 8 digit counter.
2	2	ZERO	This output is low whenever the counter's contents are 0000, independent of the display latch contents. The ZERO output is not valid during a load counter operation (while LOAD COUNTER is high and for 5 milliseconds after LOAD COUNTER was high).
3	3	EQUAL	This output is low whenever the counter's contents equals the contents of the comparison register. This output is not valid during Load Counter and Load Register operations (while LOAD COUNTER or LOAD REGISTER is high, and for 5 milliseconds after either LOAD COUNTER or LOAD REGISTER was high).
13	13	SCAN	In most applications, the scan pin is left floating and the internal multiplex scan frequency of 2500Hz is used. Connecting a capacitor between V^+ and the SCAN pin lowers the multiplex oscillator frequency. If desired, the SCAN pin can be externally driven. The internal digit multiplex counter advances with each positive-going edge at SCAN, and the digit outputs are enabled only while the SCAN pin is low. LED display brightness can be controlled by varying the duty cycle at the SCAN input. The SCAN pin is internally disconnected and the internal oscillator is used during Load Counter and Load Register operations. This increases the scan frequency to 8kHz, reducing the time required for a load counter or load register operation.
23	20	DISPLAY CONTROL	This is a three-level input with internal 100 kilohm resistors which bias the pin to 2.5V when it is floating. Leading Zero Blanking is enabled when this pin is floated or driven to 2.5V. Leading Zero Blanking is inhibited when this pin is connected to Ground. The segment drivers are disabled and the LED display is blanked when this pin is connected to V^+. BCD outputs and digit outputs remain active.
11	11	LOAD REGISTER/OFF	This is a three-level input. Leave the pin floating or drive it to 2.5V for normal operation. Connect the LOAD REGISTER/OFF pin to ground to put the ICM7217 into the shutdown mode. This puts the segments drivers, the digit drivers, and the BCD I/O into a high impedance state. The ICM7217 will continue to count normally while in the shutdown mode. A high pulse (100ns minimum) starts the LOAD REGISTER operation. The SCAN pin is disconnected from external circuitry and the multiplex counter is reset to D4. The digits are then scanned in the sequence D4, D3, D2, D1; and the internal comparison register is loaded with the data present at the BCD I/O pins at the end of each digit period. At the end of the D1 digit period, the LOAD REGISTER is still high. If thumbwheel switches are connected as shown in Figure 1, the value on the thumbwheel switches is loaded into the comparison register.
12	12	LOAD COUNTER/ I/O OFF	The LOAD COUNTER/I/O OFF pin is a three-level input. Leave it floating or drive it to 2.5V for normal operation. Connecting LOAD COUNTER/I/O OFF to ground puts the BCD output into a high impedance state, but does not affect the LED drive outputs. A high pulse (100ns minimum) starts the LOAD COUNTER operation. The LOAD COUNTER operation presets counter contents to the value on the thumbwheel switches (Figure 1), in the same manner as the load register operation described above.



ICM7217/COUNT and Output Timing

SYM.	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{UCs}	UP/$\overline{DOWN}$ setup time (min.)		300		ns
t_{UCh}	UP/$\overline{DOWN}$ hold time (min.)		750		ns
t_{CUh}	COUNT pulse high (min.)		100	250	ns
t_{CUl}	COUNT pulse low (min.)		100	250	ns
t_{CB}	COUNT to CARRY/ BORROW delay		750		ns
t_{Bw}	CARRY/ BORROW pulse width		100		ns
t_{CEl}	$\overline{COUNT}$ to EQUAL delay		500		ns
t_{CZl}	$\overline{COUNT}$ to $\overline{ZERO}$ delay		300		ns

Typical Applications

Four Digit, Preset and Predetermining Counter

The test circuits, Figures 1 and 2, are complete four digit up/down counters with preset and predetermining (comparison) capability. Momentarily pressing the Load Counter switch will preset the counter to the number set into the thumbwheel switches. Similarly, momentarily pressing the Load Register switch will load the predetermining or comparison register with the number set into the thumbwheel switches.

When the Store switch is closed, the displayed count follows the counter. Opening the Store switch "freezes" the display at the current count. Closing the Reset switch at any time clears the counter to 0000.

The ZERO output goes low whenever the counter content is 0000, and the EQUAL output goes low whenever the count reaches the value in the predetermining or comparison register.

Eight Digit Counter

The CARRY/BORROW output is used to cascade two 4 digit counter sections to form an eight digit counter. If leading zero blanking is desired, drive the Display Control pin of the least significant ICM7217 with an NPN transistor whose base is connected to the Zero output of the most significant ICM7217.

Multiple Setpoints

Analog switches such as the CD4066 can drive the BCD I/O pins. In Figure 3, the number set on thumbwheel switch A is loaded into the comparison register, the number on thumbwheel switch B presets the counter.

Trailing Zero Display

In some applications leading zero blanking is desired, but a count of 0000 must result in a display of a single 0 in the rightmost digit. Figure 4 performs this task by driving Display Control to the "disable leading zero blanking" state whenever digit D1 is active.

Batch Counter or Divide by N Counter

The circuit of Figure 5A will put out a pulse each time the count reaches the number loaded into the comparison register.

RESET is taken low each time the count reaches the preset number, resetting the counter to 0000. The AND gate is used for feedback to RESET, since a simple RC circuit can "lockup" if the comparison register is loaded with 0000.

Figure 5B is a similar circuit, except that the counter counts down, and is preset each time the count reaches zero. Since the Load Counter (preset) operation may take as long as 5 milliseconds, this circuit should be used only with signals of 12,000 counts per minute (200Hz) or less.

4 Digit (LED) Presettable Up/Down Counter

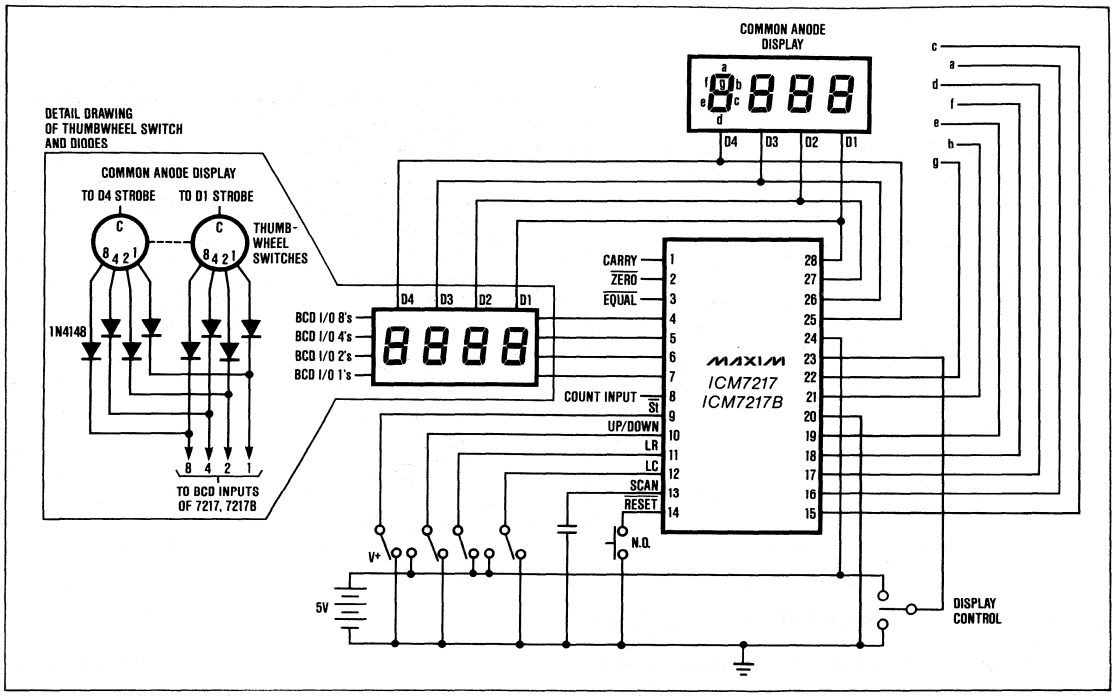


Figure 1. Basic Up/Down Counter with Common Anode LED Display.

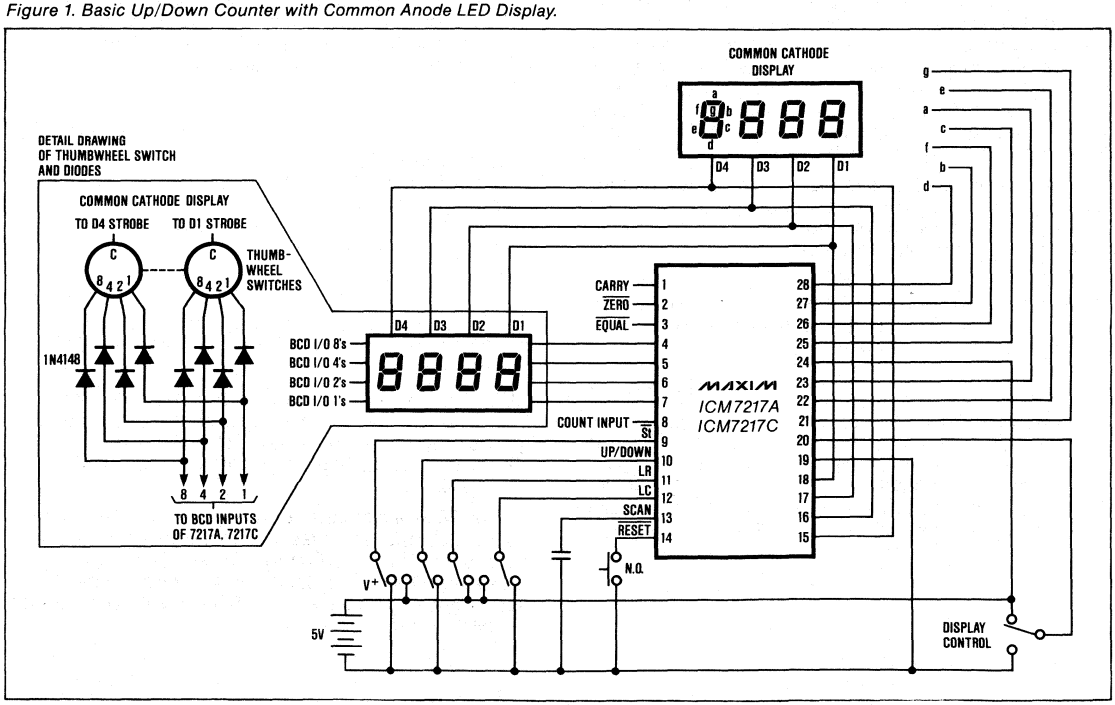


Figure 2. Basic Up/Down Counter with Common Cathode LED Display.

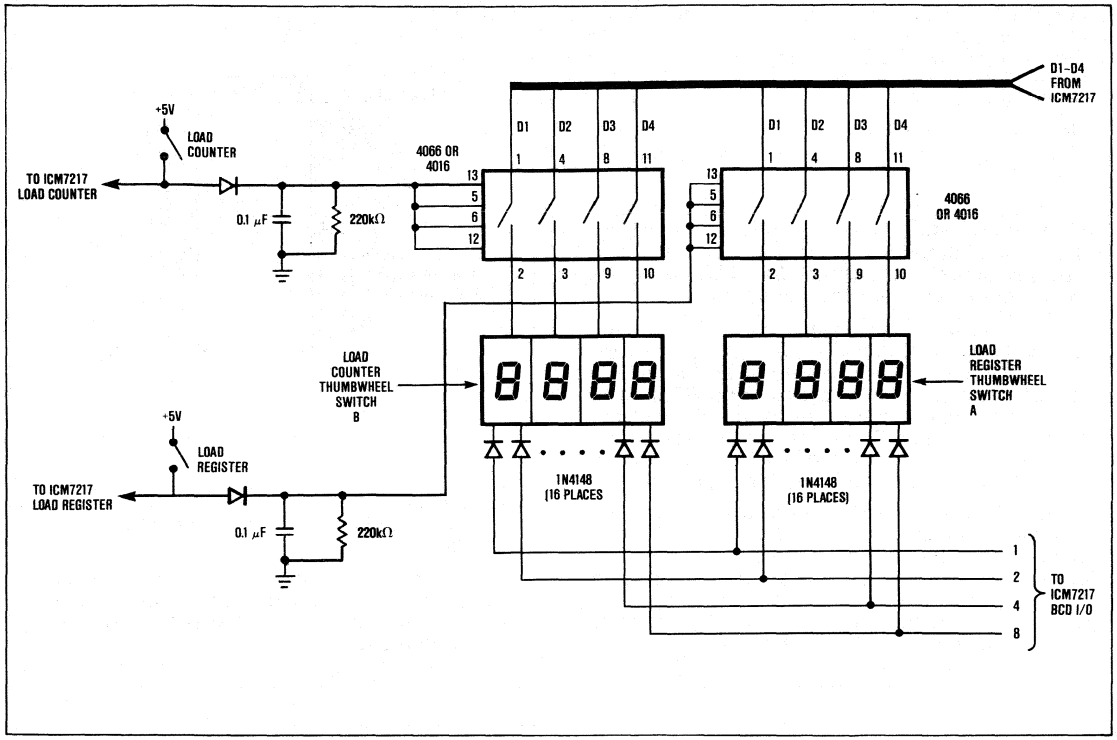


Figure 3. Multiple Thumbwheel Switches

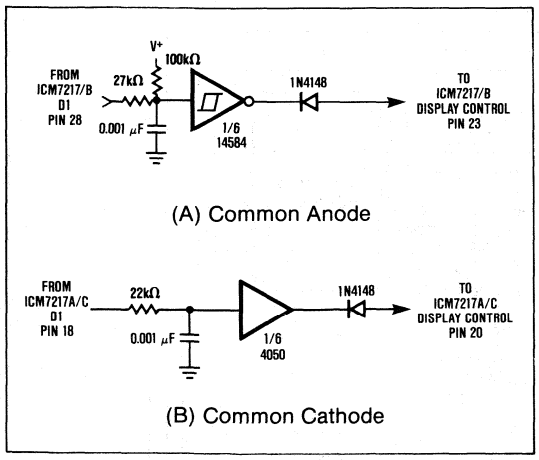


Figure 4. Trailing Zero Display

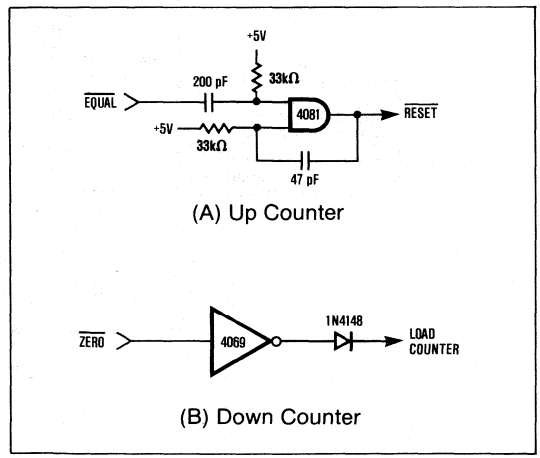


Figure 5. Connections for Divide-By-N Batch Counters.

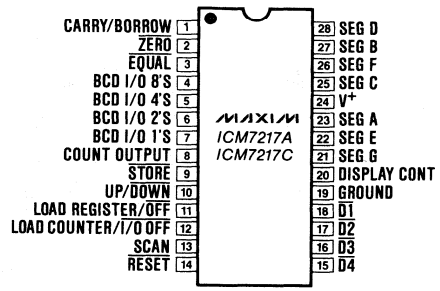
4 Digit (LED) Presettable Up/Down Counter

Application Hints

1. Use a minimum of 47μF in parallel with a 0.1μF ceramic bypass capacitor between V^+ and ground, in the immediate vicinity of the ICM7217. This bypassing is required to reduce the power supply ripple created by the high current multiplexed LED drive signals.
2. Use the Common Anode versions (ICM7217 and ICM7217B) where the brightest LED display is desired.
3. The SCAN pin can be used to control digit sequencing while reading BCD output data with a microprocessor, but the SCAN pin is disconnected and the multiplex rate is increased to 2kHz during the load register and load counter operations.
4. Load counter and load register operations continue for up to 5 milliseconds after the LOAD COUNTER or LOAD REGISTER pin has returned to the floating state. During this 5 millisecond period, RESET will load a zero into some or all of the digits of the counter or register. EQUALS and ZERO are not valid during this loading period, and the counter is inhibited during the load counter operation.
5. If the UP/DOWN input changes state during the 750ns after a positive transition at COUNT, the upper digits of the counter may be erroneously incremented or decremented. This is caused by the transmission of erroneous carry/borrow signals to adjacent digits when major bit changes occur in a digit counter coincident with an up/down input transition.

Pin Configuration

Top View



6. If the 200ns STORE high to RESET low setup time is not met, RESET may clear some of the bits in the display latch.
7. Data cannot be transferred directly from the counter to the comparison register. Use a 74C915 7-segment-to-BCD reverse decoder between the segment outputs and the BCD inputs.

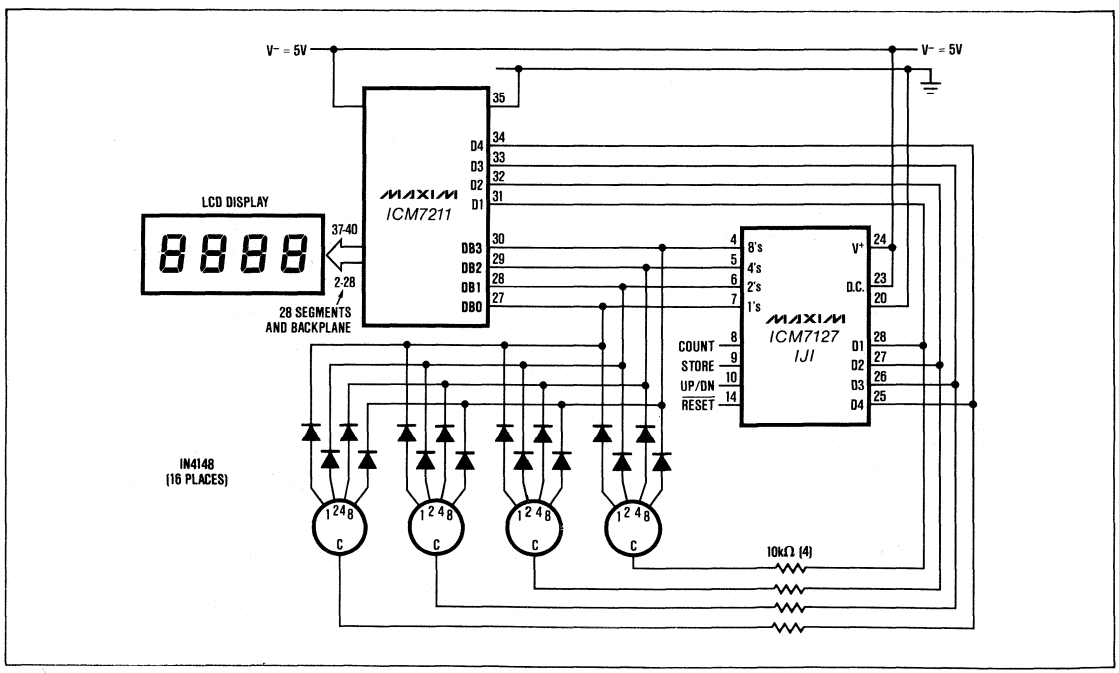


Figure 7. LCD Interface using ICM7211

MAXIM
8 Digit LED Display Driver

General Description

The Maxim ICM7218 display driver interfaces microprocessors to an 8 digit, 7 segment, numeric LED display. Included on chip are two types of 7 segment decoders, multiplex scan circuitry, segment and digit drivers, and an 8×8 static memory.

The ICM7218A and ICM7218B accept data in a serial format and drive common anode (ICM7218A) or common cathode (ICM7218B) displays. The ICM7218C and ICM7218D accept data in a parallel format and drive common anode (ICM7218C) or common cathode (ICM7218D) displays. All four versions can display the data in either hexadecimal or code B format. The ICM7218A and ICM7218B also feature a No Decode mode where each individual segment can be independently controlled. This is particularly useful in driving bar graphs.

Applications

Instrumentation
Test Equipment
Hand Held Instruments
Bargraph Displays
Panel Meters

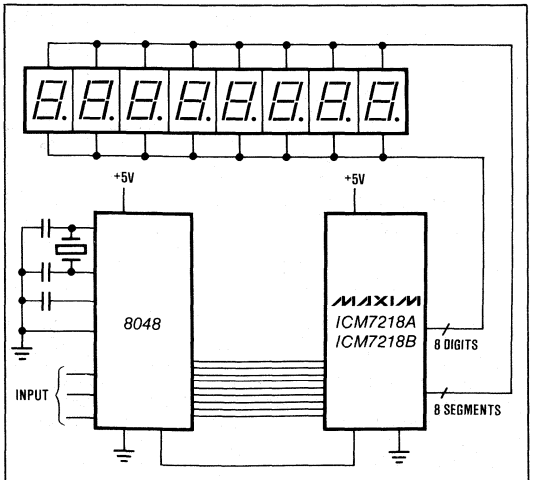
Features

- **Improved 2nd Source! See 3rd page of this data sheet for our "Maxim Advantage™"**
- **Faster Access Time: 200ns Write Pulse Width**
- **Microprocessor Compatible**
- **Hexadecimal and Code B Decoders**
- **Individual Segment Control with "No Decode" Feature**
- **Digit and Segment Drivers On-Chip**
- **Common Anode and Common Cathode LED versions available**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7218AIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218AIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218BIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218BIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218CIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218CIJI	-20°C to +85°C	28 Lead CERDIP
ICM7218DIPI	-20°C to +85°C	28 Lead Plastic DIP
ICM7218DIJI	-20°C to +85°C	28 Lead CERDIP

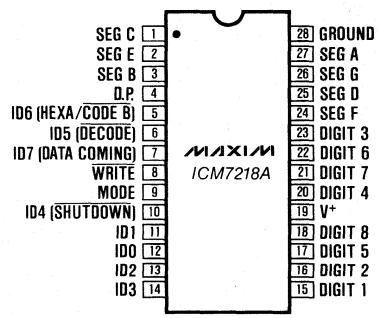
Typical Operating Circuit



8 Digit Microprocessor Display

Pin Configuration

Top View



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

8 Digit LED Display Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 500mA
Segment Output Current 100mA
Input Voltage (any terminal) ..... V^+ + 0.3V to GND -0.3V (Note 1)
Power Dissipation (28 Pin CERDIP) ..... 1.0W (Note 2)
Power Dissipation (28 Pin Plastic with Copper Leadframe) ..... 1.0W (Note 2)
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -65°C to 160°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V ± 10%, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V^+	Power Down Mode	4 2		6 6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	µA
Operating Supply Current	I_{OP}	Decoder On, Outputs Open Ckt No Decode, Outputs Open Ckt	250 200		950 450	µA µA
Digit Drive Current	I_{DIG}	Common Anode V_{OUT} = V^+ - 2.0V Common Cathode V_{OUT} = V^- + 1V	-170 50			mA mA
Digit Leakage Current	I_{DLK}				100	µA
Peak Segment Drive Current	I_{SEG}	Common Anode V_{OUT} = V^- + 1.5V Common Cathode V_{OUT} = V^+ - 2.0V	20 -10	25		mA mA
Segment Leakage Current	I_{SLK}				50	µA
Display Scan Rate	f_{MUX}	Per Digit		250		Hz
Three Level Input Logical "1" Input Voltage Floating Input Logical "0" Input Voltage	 V_{INH} V_{INF} V_{INL}	 Hexadecimal ICM7218C, D (Pin 9) Code B ICM7218C, D (Pin 9) Shutdown ICM7218C, D (Pin 9)	 4.0 2.0		 3.0 1.75	 V V V
Three Level Input Impedance	Z_{IN}	Note 3		100		kΩ
Logical "1" Input Voltage Logical "0" Input Voltage	V_{IH} V_{IL}		3.5		 0.8	V V
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	7218A, B	550 550	400 400		ns ns
Write Pulse Width (Negative) Write Pulse Width (Positive)	t_W $t_{\overline{W}}$	7218C, D	400 400	250 250		ns ns
Mode Hold Time	t_{mh}	7218A, B		150		ns
Mode Pulse Width	t_m	7218A, B	500			ns
Data Set Up Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		25			ns
Digit Address Set Up Time Digit Address Hold Time	t_{das} t_{dah}	ICM7218C, D ICM7218C, D	500 100			ns ns
Data Input Impedance	Z_{IN}	5-10pF Gate Capacitance		10^{10}		Ohms

Note 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than GROUND may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.

Note 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C

Note 3: In the ICM7218C and D (random access versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50µA. The ICM7218A and B devices do not have these biasing resistors and thus are not subject to this condition.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983, 1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The Electrical Characteristics Table along with the descriptive excerpts from manufacturer's data sheet have been included in this data sheet solely for comparative purposes

8 Digit LED Display Driver

- ♦ 200ns Write Pulse Width
- ♦ Zero Hold Time - Mode, Data and Address
- ♦ Single Digit Update Mode ICM7218A, B
- ♦ Guaranteed Interdigit Blanking Time
- ♦ Increased LED Display Drive Current
- ♦ Improved ESD Protection (Note 4)
- ♦ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $T_A = 25°C$

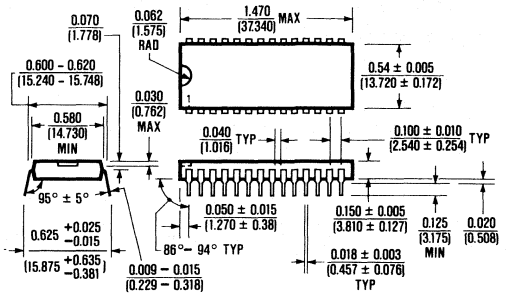
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	V^+	Data Retention	4 2		6	V V
Shutdown Supply Current	I_Q	ICM7218A, B ICM7218C, D (3 level input open)		5 25	300 300	µA µA
Operating Supply Current	I_{OP}	**Decoding all 8's, display outputs open** **No decode, display outputs open** **Display blank, driving display** Decoding all 8's and D.P's, driving display		**200** **200** **200** 240	**450** **450** **450**	**µA** **µA** **µA** mA
Digit Drive Current	I_{DIG}	**Common Anode, $V_{OUT} = V^+ - 2.0V$** Common Cathode, $V_{OUT} = 1.0V$	**-200** 50	**-300** 70		**mA** mA
Digit Leakage Current	I_{DLK}	Shutdown, $V^+ = 5V$ Common Anode, $V_{OUT} = 0V$ Common Cathode, $V_{OUT} = 5V$		 -10 10	 -100 100	 µA µA
Peak Segment Drive Current	I_{SEG}	Common Anode, $V_{OUT} = 1.5V$ Common Cathode, $V_{OUT} = V^+ - 2.0V$	20 -10	30 -20		mA mA
Segment Leakage Current	I_{SLK}	Shutdown, $V^+ = 5V$ Common Anode, $V_{OUT} = 5V$ Common Cathode, $V_{OUT} = 0V$		 -1 1	 -50 50	 µA µA
Input Leakage Current	I_{IL}	**All inputs except pin 9 of ICM7218C, D** **$V^+ = 5V$** **$V_{IN} = 0V$** **$V_{IN} = 5V$**		 **-0.01** **0.01**	 **-1** **1**	 **µA** **µA**
Display Scan Rate	f_{MUX}	**$V^+ = 5V$**	**75**	**250**		**Hz**
Interdigit Blanking Time	t_{idb}	**$V^+ = 5V$**	**2**	**10**		**µs**
Three Level Input	V_{INH} V_{INF} V_{INL}	Pin 9, ICM7218 C, D only, $V^+ = 5V$ Input "high" voltage Floating Input Input "low" voltage	 4.2 2.0		 3.0 0.8	 V V V
Three Level Input Impedance	Z_{IN}	**Pin 9, ICM7218 C, D only**	**50**	**100**		**kΩ**
Input High Voltage Input Low Voltage	V_{IH} V_{IL}	All inputs except pin 9 of ICM7218C, D	2.0		 0.8	V V
Write Pulse Width (Low)	t_{wl}		**200**	**100**		**ns**
Write Pulse Width (High)	t_{wh}		1.5			µs
Input Setup Time	t_{ids}	**All inputs except pin 9 of ICM7218 C, D (Note 5)**	**250**	**150**		**ns**
Input Hold Time	t_{idh}	**All inputs except pin 9 of ICM7218 C, D (Note 5)**	**0**	**-20**		**ns**

Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883B Method 3015.1 Test Circuit).

Note 5: This specification replaces the original manufacturer's separate specifications for data, address, and mode inputs.

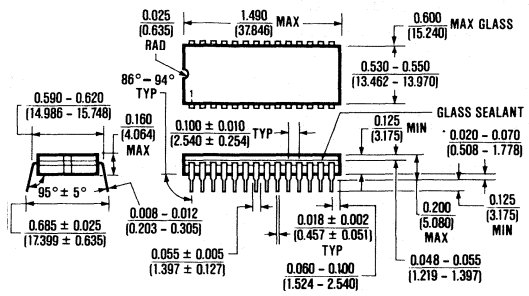
8 Digit LED Display Driver

Package Information



28 Lead Plastic (PI) with Copper Leadframe

θ_{JA} = 60°C/W



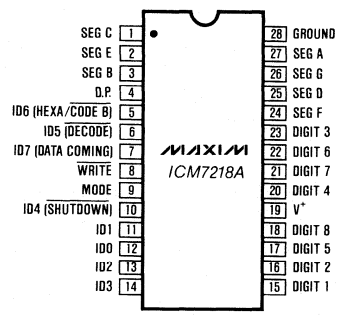
28 Lead Cerdip (JI)

θ_{JA} = 55°C/W

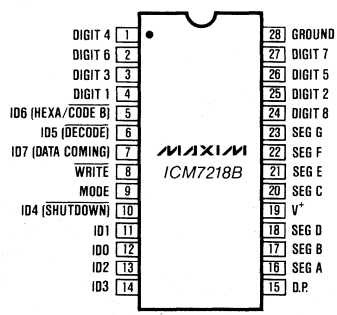
Pin Configurations

Top View

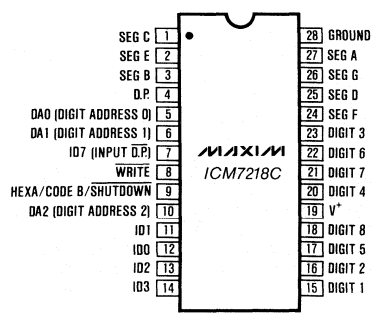
28 Pin DIP



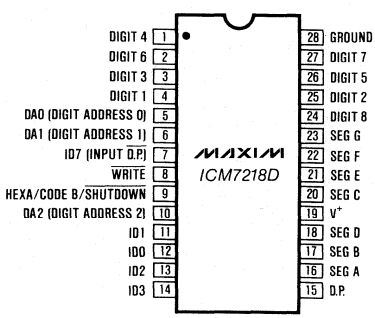
28 Pin DIP



28 Pin DIP



28 Pin DIP



4½ Digit Counter/Decoder/Driver

General Description

The Maxim ICM7224(LCD) and ICM7225(LED) are high speed 4½ digit counters, featuring segment decoders, leading zero blanking, store and reset inputs, and a carry output that allows cascading of 8 or more digits. The ICM7224 directly drives a non-multiplexed liquid crystal display(LCD). The ICM7225 has 29 constant current outputs for driving a non-multiplexed common anode LED display.

These counters operate with inputs from DC to 25MHz while using only 10μA of supply current. A Schmitt trigger on the count input ensures reliable operation in noisy environments and in applications with slowly varying inputs.

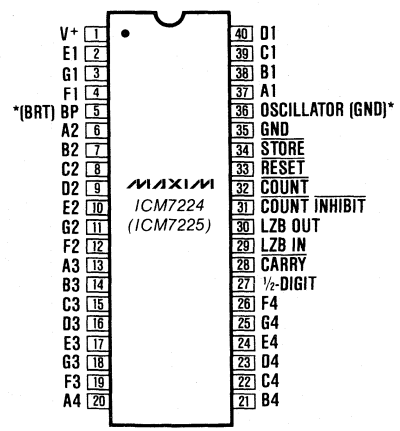
The ICM7224 and ICM7225 are available in a 44 lead plastic chip carrier package in addition to the standard 40 lead plastic DIP.

Applications

Unit Counter
Frequency Counter
Tachometer
Hour Meter
Totalizer

Pin Configuration

Top View



*Note:

PIN #	ICM7224 FUNCTION	ICM7225 FUNCTION
5	Backplane	Brightness
36	Oscillator	Ground

See Last Page for 44 Lead Chip Carrier Pin Configuration.

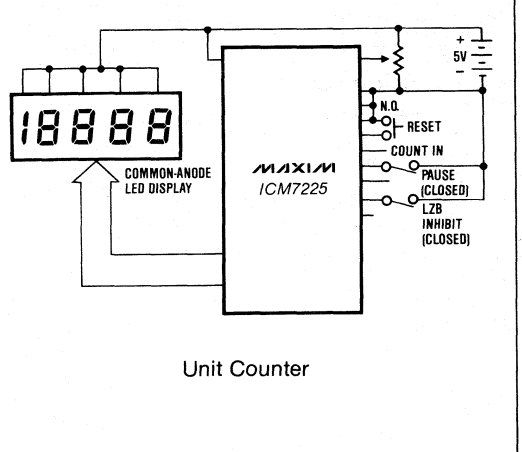
Features

- **Improved 2nd Source! (See 3rd page for "Maxim Advantage™").**
- **High Speed Up Counter: 25MHz Typ.**
- **Leading Zero Blanking**
- **Can Be Cascaded for 8 or More Digits**
- **STORE and RESET Inputs for Frequency Counter Applications**
- **On-Board Oscillator to Provide Backplane Frequency (ICM7224)**
- **Brightness Control Input (ICM7225)**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7224IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7224CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICM7224C/D	0°C to +70°C	Dice
ICM7225IPL	-20°C to +85°C	40 Lead Plastic DIP
ICM7225CQ	0°C to +70°C	44 Lead Plastic Chip Carrier
ICM7225C/D	0°C to +70°C	Dice

Typical Operating Circuit



Unit Counter

The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

4½ Digit Counter/Decoder/Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Input Voltage (any terminal, Note 1) ..... -0.3V to V^+ +0.3V
Power Dissipation
40 Lead Plastic Dip 1W
(derate 10mW/°C above 25°C.)
44 Lead Plastic Chip Carrier 1W
(derate 10mW/°C above 25°C.)

Operating Temperature Range
Plastic Package (IPL) ..... -20°C to +85°C
Plastic Chip Carrier (Quad) Package (Q) ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Note 1: The input voltage may exceed this rating if the input current is limited to 1mA. Connecting any terminal to a voltage greater than V^+ or less than Ground and exceeding 1mA input current may activate the parasitic SCR inherent in the junction isolated CMOS process, causing destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/25 be turned on first.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(All parameters measured with V^+ = 5V, unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	µA
Operating supply voltage range	V^+		3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	µA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		µs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		µs
Oscillator frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (BRighTness) at GROUND Pin 29, 31-34 at V^+		10	50	µA
Operating supply voltage range	V^+		4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	µA
Segment on current	I_{SEG}	Segment On, V_{out} = +3V	5	8		mA
Half-digit on current	I_H	Half-digit On, V_{out} = +3V	10	16		mA

FAMILY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-up Currents	I_P	Pins 29, 31, 33, 34 $V_{out} = V^+ - 3V$		10		µA
Input High Voltage	V_{IH}	Pin 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pin 29, 31, 33,			1	V
$\overline{COUNT}$ Input Threshold	V_{CT}			2		V
$\overline{COUNT}$ Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 $V_{out} = V^+ - 3V$	350	500		µA
Output Low Current	I_{OL}	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = +3V	350	500		µA
Count Frequency	f_{count}	$4.5V < V^+ < 6V$	0	DC-25	15	MHz
$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width	t_S, t_R		3			µs

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

4½ Digit Counter/Decoder/Driver

- **Key Parameters Guaranteed Over Temperature**
- **Increased Segment-On Current**
- **Low Power (Typically 25μW)**
- **Maxim Quality and Reliability**
- **Significantly Improved ESD Protection (Note 1)**

ABSOLUTE MAXIMUM RATINGS:

This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS:

Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+ = 5V, T_A = 25°C unless otherwise noted)

ICM7224 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	**Display blank**		5	25	μA
Operating supply voltage range	V^+	**-20°C ≤ T_A ≤ +85°C**	3	5	6	V
OSCILLATOR input current	I_{OSCI}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pF		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pF		1.5		μs
Oscillator frequency	f_{osc}	Pin 36 Floating		19		kHz
Backplane frequency	f_{bp}	Pin 36 Floating		150		Hz

ICM7225 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	**Pin 5 (BRighTness) at GROUND Pin 29, 31-34 at V^+**		10	25	μA
Operating supply voltage range	V^+	**-20°C ≤ T_A ≤ +85°C**	4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		275		mA
Segment leakage current	I_{SLK}	Segment Off		±0.01	±1	μA
Segment on current	I_{SEG}	**Segment On, V_{out} = +3V**	6	9		mA
Half-digit on current	I_H	**Half-digit On, V_{out} = +3V**	12	18		mA

FAMILY DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-up Currents	I_P	**Pins 29, 31, 33, 34 V_{out} = V^+ - 3V**	2	10	25	μA
Input High Voltage	V_{IH}	**Pin 29, 31, 33, 34, -20°C ≤ T_A ≤ +85°C**	3			V
Input Low Voltage	V_{IL}	**Pin 29, 31, 33, 34, -20°C ≤ T_A ≤ +85°C**			1	V
$\overline{\text{COUNT}}$ Input Threshold	V_{CT}		1.5	2	3.25	V
$\overline{\text{COUNT}}$ Input Hysteresis	V_{CH}		0.1	0.5	1.75	V
Output High Current	I_{OH}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = V^+ -3V	350	500		μA
Output Low Current	I_{OL}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{out} = +3V	350	500		μA

Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883C Method 3015.2 Test Circuit).

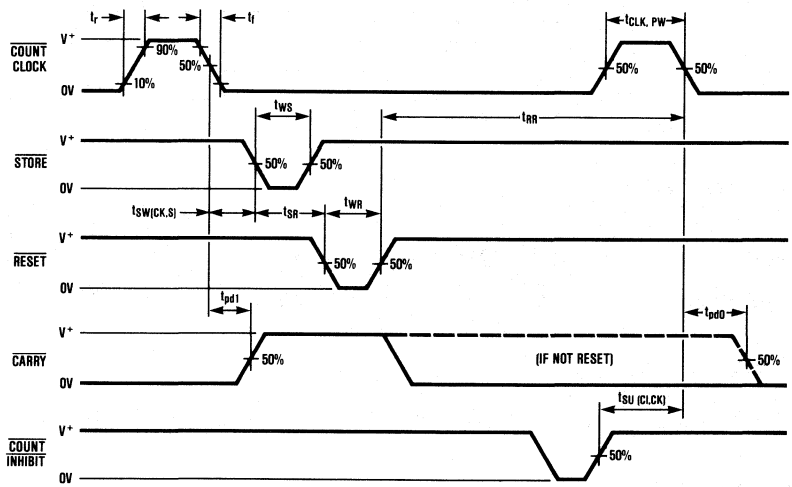
4½ Digit Counter/Decoder/Driver

FAMILY AC ELECTRICAL CHARACTERISTICS (C_L = 50pF unless noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Clock to Carry	t_{pd0}, t_{pd1}			0.6		µs
Maximum Clock Frequency	f_{CLK}		0	DC–25	15	MHz
Minimum Clock Pulse Width	$t_{CLK,PW}$			25		ns
Clock Input Rise or Fall Time	t_r, tf				No Limit	
Reset Pulse Width	t_{WR}			125		ns
Store Pulse Width	t_{WS}			1		µs
Clock to Store Set-Up Time	$t_{SU(CK,S)}$			0.4		µs
Store to Reset Wait Time	t_{SR}			1.3		µs
Inhibit to Clock Set-Up Time	$t_{SU(CI,CK)}$			0		ns
Reset Removal	t_{RR}			20		ns
Input Capacitance	C_{IN}	Logic Inputs (Note 1)		5		pF

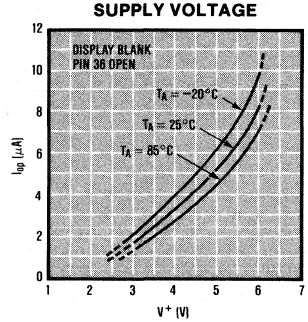
Note 1: Does not apply to backplane and oscillator pins.

Timing Diagram

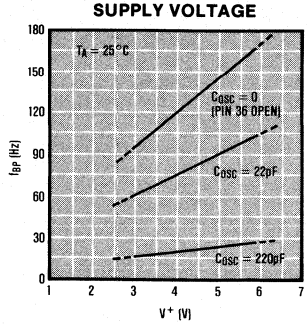


Typical Operating Characteristics

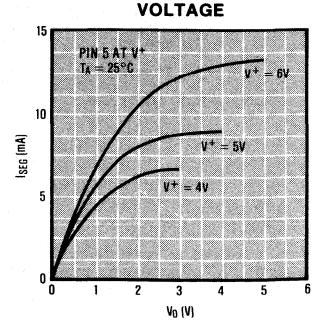
ICM 7224 OPERATING SUPPLY CURRENT VS. SUPPLY VOLTAGE



ICM 7224 BACKPLANE FREQUENCY VS. SUPPLY VOLTAGE



ICM 7225 LED SEGMENT CURRENT VS. OUTPUT VOLTAGE



MAXIM

TABLE 1. PIN DESCRIPTIONS

PIN	FUNCTION	DESCRIPTION
1	V^+	Positive power supply input.
2-4, 6-26, 37-40	Segment Outputs	These 28 pins directly drive LCD segments (ICM7224) or common anode LED segments (ICM7225). Segments A1-G1 drive the least significant digit, segments A4-G4 drive the 1000s digit.
27	½ Digit	This segment output drives both segments of the most significant half digit. This segment output turns on when the count reaches 10,000 and is reset only by a low level on the Reset input.
5 (ICM7224)	BP	The backplane pin is both an input and an output. As an output it drives the LCD backplane with an internally generated backplane signal. The backplane pin is an input when the slave mode is selected by grounding pin 36 (Oscillator).
5 (ICM7225)	BRT	An analog input voltage applied to the brightness (BRT) pin controls the output current of the LED segment drivers. Connecting this pin to ground shuts off the display. Connecting this pin to V^+ drives the display with the maximum available output current. Intermediate voltage levels will adjust the brightness to any level between full off and full brightness.
28	$\overline{\text{CARRY}}$	Connect this logic output to the Count input of another ICM7224/5 to make an 8 digit counter/display driver. The Carry output goes high at count 6000 and goes low on the transition between count 9999 and count 10,000. The Carry output repeats this cycle every 10,000 counts.
29	LZB IN	The ICM7224 displays leading zeroes when this pin is grounded. Connecting this pin to V^+ or leaving it floating enables leading zero blanking. The entire display will be blanked if this pin is high or floating, the count is 0000, and the half digit is reset. This pin has an internal 10μA pullup.
30	LZB OUT	This output allows the proper blanking of cascaded counters. The Leading Zero Blanking (LZB) output goes high when all digits are blanked.
31	$\overline{\text{COUNT INHIBIT}}$	A low level on this input pin disables the counter. Connecting this pin to V^+ or floating this pin enables the counter. This pin has an internal 10μA pullup.
32	$\overline{\text{COUNT}}$	Every negative-going transition at the Count input clocks the counter. This input has 500 mV of hysteresis to prevent multiple clocking with slow rate-of-fall inputs.
33	$\overline{\text{RESET}}$	A low level on Reset will reset the counter. Reset also clears the half-digit flip-flop and turns off the half-digit output. This input has an internal 10μA pullup and is inactive when either connected to V^+ or left floating.
34	$\overline{\text{STORE}}$	When the Store input is low, the latches are transparent and the counter contents are displayed. When Store is taken high or floated, the counter contents are latched and this latched data is displayed.
35	GND	The negative power supply input.
36 (ICM7225)	GND	An additional ground pin for the ICM7225. The ICM7225 has two ground pins to handle the high LED drive currents.
36 (ICM7224)	Oscillator	When this pin is left floating, the ICM7224 oscillates at approximately 19kHz. Connecting an external capacitor between this pin and either V^+ or GND lowers the oscillator frequency as shown in the Typical Characteristics graphs. The Oscillator can be externally driven using the circuit of Figure 4. Grounding this pin puts the ICM7224 into the slave mode, turning pin 5, BP, into an input.

Table 2. TYPICAL LCD DISPLAYS

Manufacturer	PART #	HEIGHT	# DIGITS
Epson	LD-H7924	0.350"	4½
(213) 534-0360	LD-H7916	0.500"	4
	LD-K7994	0.700"	4
LXD	44D3F-85	0.800"	4½
(216) 292-3300	44D3F-45	0.400"	4½
Hamlin	3909	0.400"	4½
(414) 648-2361	3912	0.800"	4½
AND	FE0202W-DU	0.500"	4
(415) 347-9916	FE0206W-DU	0.400"	4½

Table 3. TYPICAL LED DISPLAYS

Manufacturer	PART #	HEIGHT	COLOR
Hewlett Packard	5082-7731	0.3"	Red
(Contact local	5082-7611	0.3"	Red (Hi Eff.)
sales office)	5082-7621	0.3"	Yellow
	5082-7631	0.3"	Green
General Inst.	MAN 71A	0.3"	Red
(415) 493-0400	MAN 3910A	0.3"	Red (Hi Eff.)
	MAN 3810A	0.3"	Yellow
	MAN 3410A	0.3"	Green
Siemens Opto	HD1075R	0.3"	Red
(408) 257-7910	HD1075O	0.3"	Red (Hi Eff.)
	HD1075Y	0.3"	Yellow
	HD1075G	0.3"	Green

4½ Digit Counter/Decoder/Driver

Detailed Description

The ICM7224 and ICM7225 have identical counter and control sections, but have different display driver sections. The ICM7224 is designed to drive a non-multiplexed liquid crystal display (LCD). The ICM7225 is designed to drive a non-multiplexed, common anode LED display.

Counter and Control Logic

The counter in both the ICM7224 and ICM7225 is a 4 decade up counter with a Carry output. An overflow flip-flop, which is clocked by Carry, controls the half-digit output. This half-digit output can be used as an overflow indicator or as a half-digit to extend the count range to 19,999. Once set by Carry, the overflow flip-flop will remain set until the counter is reset by taking the Reset pin low.

The counter advances with each negative going transition on the Count input, provided the Count Inhibit and Reset inputs are high.

The Count Inhibit input disables the counter when it is low. The Count Inhibit input is similar to the J-K inputs of a J-K flip-flop; transitions on Count Inhibit do not increment the counter.

Reset is an active low input that resets the 4 digit counter and the overflow (½ digit) flip-flop. Reset does not clear the data in the display latches unless Store is low.

Store controls the flow of data into the display latches. When Store is low the latches are transparent and the counter data is displayed. When Store goes high the display latches go into the hold mode and the displayed count no longer follows the counter.

The LZB IN pin determines whether leading zeroes are blanked. Leading zeroes are displayed when LZB IN is low. Leading zeroes are blanked when LZB IN is high or floating. The LZB OUT allows proper leading zero blanking when cascading two ICM7224/ICM7225 devices to make an 8 digit counter/display driver (Figure 3). LZB OUT will go high only when LZB IN is high or floating, the count is 0000, and the overflow flip-flop is reset.

When the ICM7224/25 is used in electrically noisy environments (around solenoids, motor starters, etc.), do NOT rely upon the internal 10μA pullups on Reset, Count Inhibit, LZB IN and Store inputs. Stray pickup of transients may momentarily override the weak, 10μA pullup. Connect these pins directly to V^+, drive them with a logic gate, or parallel the internal pullup with a 4.7kΩ resistor to V^+.

ICM7224 LCD Driver Section

The LCD driver section of the ICM7224 is similar to the Maxim ICM7211 4 digit display driver. It includes an internal 19kHz oscillator with a backplane driver, and 29 segment drivers.

The 19kHz nominal output of the onboard oscillator is divided by 128 in the 7 stage divider chain to generate a 150Hz backplane frequency. The Backplane output, pin 5, is a low impedance (200Ω typical) output that swings from ground to V^+ at the backplane frequency with a 50% duty cycle. The 29 segment drivers also swing from ground to V^+ and have an output impedance of approximately 2kΩ. The ICM7224 drives an LCD segment in phase with the backplane to turn the

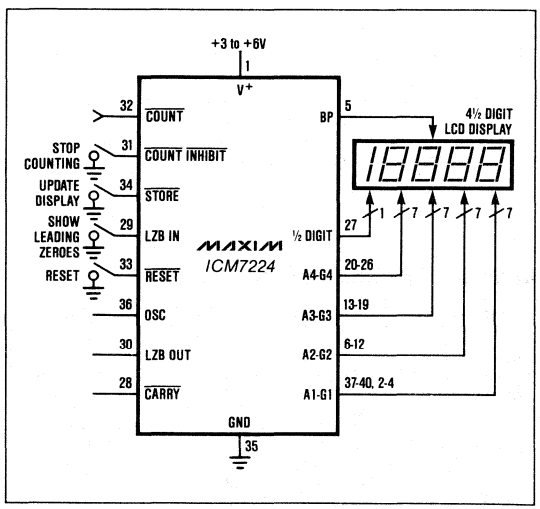


Figure 1. Simple 4½ Digit Event or Unit Counter with LCD Display

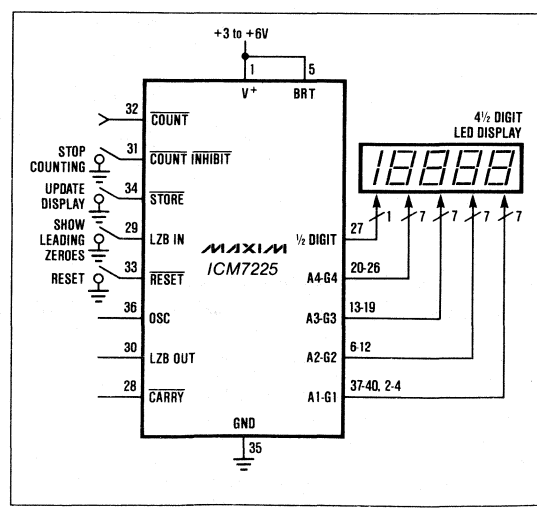


Figure 2. Simple 4½ Digit Event or Unit Counter with LED Display

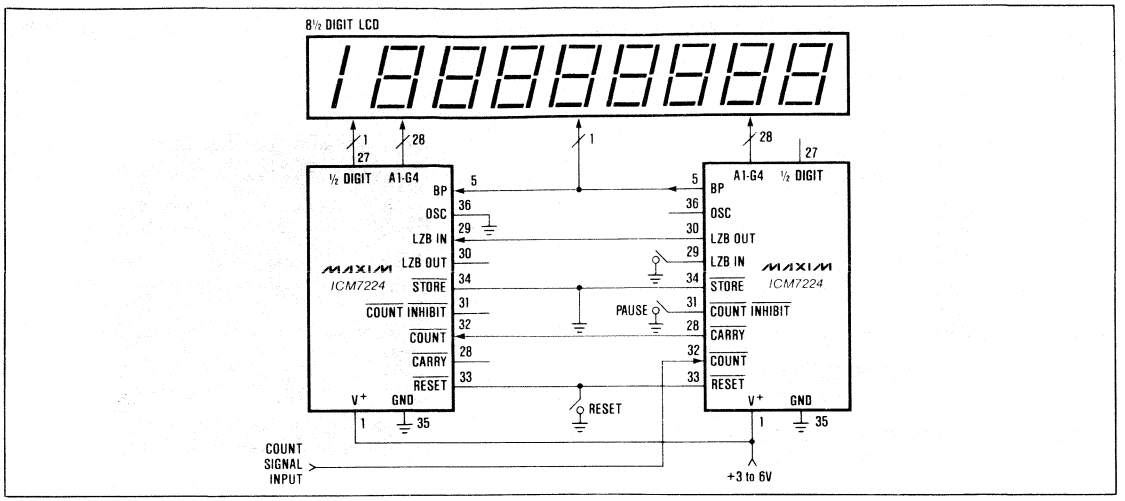


Figure 3. 8½ Digit Totalizer

segment off, and drives the LCD segment 180° out of phase with the backplane to turn the segment on.

The internal oscillator has a nominal oscillation frequency of 19kHz with no external components. This frequency can be lowered by connecting a capacitor from pin 36 (Oscillator) to either ground or V^+. See Typical Characteristics graph, Backplane Frequency vs. Supply Voltage. The oscillator can also be overdriven by an external source as shown in Figure 4. The two resistors connected from the driver to pin 36 keep the voltage at pin 36 (Oscillator) above the 1.5V threshold of the backplane slaving detector which is internally connected to pin 36.

When two or more ICM7224 counter/display drivers drive one LCD with a single backplane, the backplane outputs of the ICM7224 counter/display drivers must be synchronized. This is performed by grounding the Oscillator (pin 36) on all but one device; and connecting together the Backplanes (pin 5) of all devices. The one device with the Oscillator input not grounded will drive both its own Backplane pin and the Backplane pins of the other devices. The devices with the Oscillator input grounded disable their backplane drivers and use the Backplane pin as an input. See Figure 3.

ICM7225 LED Display Interface

The ICM7225 has 29 open drain N channel segment drivers. These drivers are constant current sinks, whose sink current varies from 0 to 9mA as the voltage on BRT (pin 5) varies from ground to V^+ (0 to 18mA for pin 27, the ½ digit output). Segment current limiting resistors are not needed.

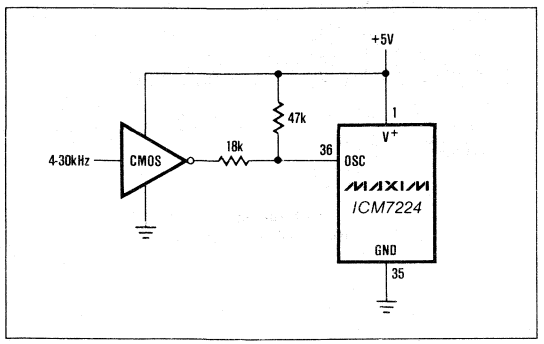


Figure 4. External Clock Drive.

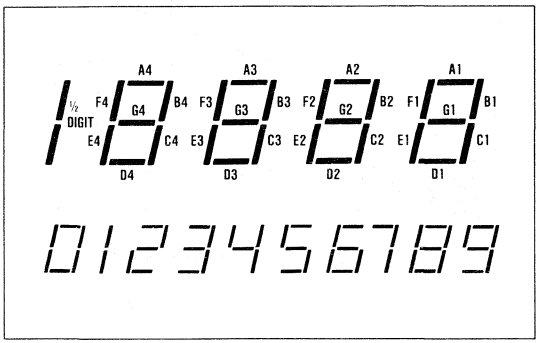
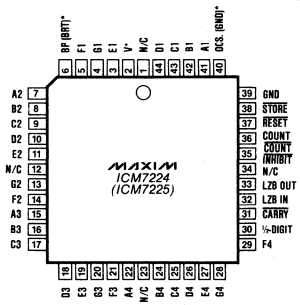


Figure 5. Segment Assignment and Display Font

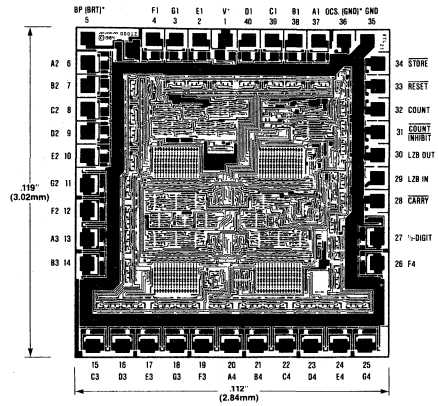
4½ Digit Counter/Decoder/Driver

Pin Configuration



44 Lead Plastic Chip Carrier
(Quad Pack) (Q)

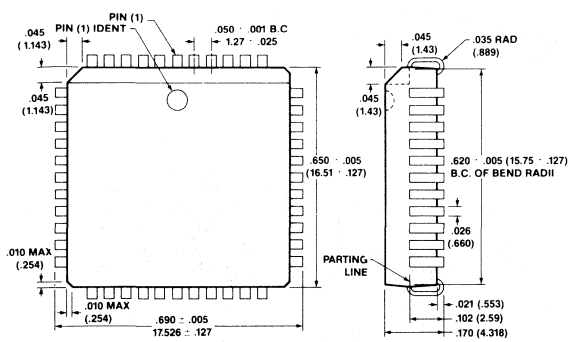
Chip Topography



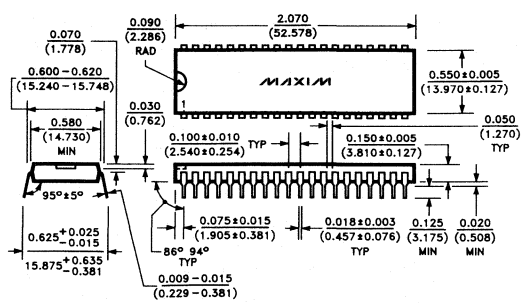
*Note:

PIN #	ICM7224 FUNCTION	ICM7225 FUNCTION
6	Backplane	Brightness
40	Oscillator	Ground

Package Information



44 Lead Plastic Chip Carrier (Quad Pack) (Q)



40 Lead Plastic (PL)
θ_{JA} = 100°C/W, θ_{JC} = 45°C/W

MAXIM

Fixed And Programmable Timer/Counters

General Description

The Maxim ICM7240/50/60 are programmable timer/counters and the Maxim ICM7242 is a fixed timer/counter. They require only 120μA of supply current, while generating delays from microseconds to days. Each device combines a counter with an internal oscillator whose period is controlled by an external resistor and capacitor. The oscillator can be inhibited and an external clock applied to the TB I/O terminal. The programmable counters in the ICM7240/50/60 can be programmed using thumbwheel switches, jumpers, and analog switches.

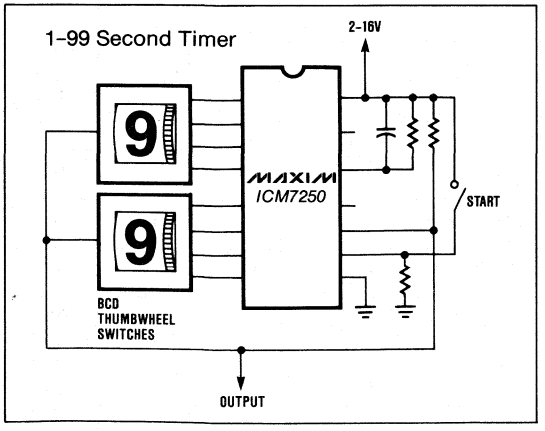
The ICM7240 has an 8 bit programmable counter and can generate time delays from 1 to 255 RC time constants. The ICM7250 has a two digit programmable BCD counter and can generate time delays from 1 to 99 RC time constants. The ICM7260 is used for "real time" applications and has a modulo 60 programmable divider, producing time delays from 1 to 59 RC time constants. The ICM7242 has an 8 bit fixed counter and can generate a time delay of 1 and 128 RC time constants. These four devices are easily cascaded and can operate in either astable or monostable configurations, using the on-chip control flip-flop with Trigger and Reset inputs.

Applications

The ICM7240/42/50/60 family is suitable for a wide variety of timing and control applications.

ON/OFF Delay Timers
Batch Timer/Sequencers
Cycle Timers
Programmable Timers
Frequency Synthesizers
Ultra-Long Time Delay Generators

Typical Operating Circuit



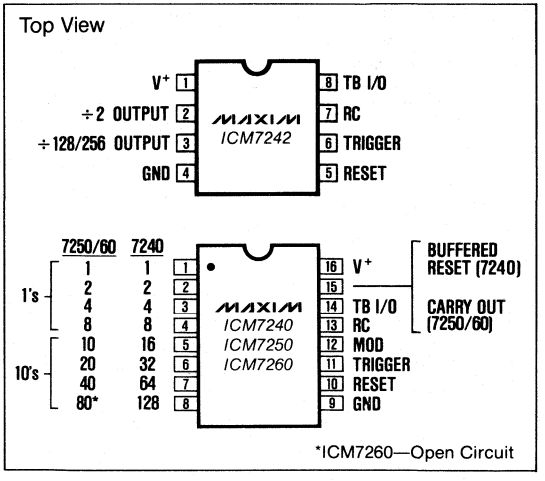
Features

- **Improved Second Source! (See 3rd page for "Maxim Advantage™.")**
- **Low Supply Current: 120μA**
- **Timing from μs to Days**
- **Shutdown Current less than 10μA**
- **Programmable Fixed Count**
- **Cascadable for Long Range Timing**
- **Monostable or Astable Operation**
- **Low Power CMOS**

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICM7240IPE	-20°C to +85°C	16 Lead PLASTIC DIP
ICM7240IJE	-20°C to +85°C	16 Lead CERDIP
ICM7240C/D	0°C to +70°C	Dice
ICM7242IPA	0°C to +85°C	8 Lead PLASTIC DIP
ICM7242IJA	-20°C to +85°C	8 Lead CERDIP
ICM7242C/D	0°C to +70°C	Dice
ICM7250IPE	-20°C to +85°C	16 Lead PLASTIC
ICM7250IJE	-20°C to +85°C	16 Lead CERDIP
ICM7250C/D	0°C to +70°C	Dice
ICM7260IPE	-20°C to +85°C	16 Lead PLASTIC
ICM7260IJE	-20°C to +85°C	16 Lead CERDIP
ICM7260C/D	0°C to +70°C	Dice

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Fixed and Programmable Timer/Counters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Input Voltage (Note 1)
ICM7240/50/60,
pins 10,11,12,13,14 ..... (Gnd-0.3V) to (V^+ +0.3V)
ICM7242
pins 5,6,7,8 ..... (Gnd-0.3V) to (V^+ +0.3V)
Output Voltage
ICM7240/50/60
pins 1,2,3,4,5,6,7,8 ..... (Gnd-0.3V) to +18V
pins 14,15 ..... (Gnd-0.3V) to (V^+ 0.3V)
Output Voltage
ICM7242
pins 2,3,8 ..... (Gnd-0.3V) to (V^+0.3V)
Maximum Continuous Output
Current (each output) 50mA
Power Dissipation 200mW
Derate at -2mW/°C above 25°C.
Operating Temperature Range ..... -20°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Due to the SCR structure inherent in the CMOS process, connecting any terminal (except pins 1 through 8 on the ICM7240/50/60) to voltages greater than V^+ or less than Ground may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources be applied to the device before the supply is established. In multiple supply systems, the supply to ICM7240/42/50/60 should be turned on first. Pins 1 through 8 in the ICM7240/50/60 are open drain devices and are rated to withstand 18Volts with respect to ground (pin 9).

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+=+5V, T_A=+25°C, R=10kΩ, C=0.1μF, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current 7240,50,60	I^+	Reset Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF		125 300 120	 700 500	μA μA μA
7242		TB Inhibited, RC Connected to GND Operating, R = 10kΩ, C = 0.1μF Operating, R = 1MΩ, C = 0.1μF TB Inhibited, RC Connected to GND		125 340 220 225	 800 600	μA μA μA μA
Timing Accuracy				5		%
RC Oscillator Frequency Temperature Drift	Δf/ΔT	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA I_{SINK} = 3.2 mA	3.5	4.2 0.25	 0.6	V V
Time Base Output Leakage Current	I_{TBLK}	RC = Ground			25	μA
Mod Voltage Level 7240/50/60	V_{MOD}	V^+ = 5V V^+ = 15V		3.5 11.0		V V
Trigger Input Voltage	V_{TRIG}	V^+ = 5V V^+ = 15V		1.6 3.5	2.0 4.5	V V
Reset Input Voltage	V_{RST}	V^+ = 5V V^+ = 15V		1.3 2.7	2.0 4.0	V V
Max Count Toggle Rate 7240, 7242	f_t	V = 2V V = 5V V = 15V —Counter/Divider Mode 50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND	2	1 6 13		MHz MHz MHz
Max Counter Toggle Rate, 7250, 7260	f_t	V^+ = 5V (Counter/Divider Mode)	1.5	5		MHz
Max Count Toggle Rate 7240, 7250, 7260	f_t	Programmed Timer — Divider Mode			100	kHz
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output V^+ = 5V, I_{OUT} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	V^+ = 5V, per Output			1	μA
Output Sourcing Current 7242	I_{SOURCE}	V^+ = 5V Terminals 2 & 3, V_{OUT} = 1V		300		μA
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	$V^+ \leq 5.5V$ $V^+ \leq 16V$			22M 22M	Ω Ω

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983, 1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The Electrical Characteristics Table along with the descriptive excerpts from the manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

Fixed And Programmable Timer/Counters

- **Synchronous High Speed Operation**
- **No False Clocking**
- **Increased Toggle Rate**
- **Supply Current Guaranteed Over Temperature**
- **Standby Current Less Than 10μA**
- **Significantly Improved ESD Protection (Note 1)**
- **Maxim Quality and Reliability**

ABSOLUTE MAXIMUM RATINGS: These devices conform to the Absolute Maximum ratings on the adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V^+=+5V, T_A=+25°C, Test circuit: R=10kΩ, C=0.1μF, unless otherwise specified).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Guaranteed Supply Voltage	V^+		2		16	V
Supply Current	I^+	**Reset, -20°C ≤ T_A ≤ +85°C** **Operating, R = 10kΩ, C = 0.1μF, T_A = 25°C** **-20°C ≤ T_A ≤ +85°C** **Operating, R = 1MΩ, C = 0.1μF (Note 2)** **TB Inhibited, RC Connected to GND** **-20°C ≤ T_A ≤ +85°C**		**125** **300** **120** **10**	**500** **700** **800** **500** **10**	**μA** **μA** **μA** **μA** **μA**
Timing Accuracy		V^+ = +5V, R = 10kΩ, C = 0.1μF		5		%
RC Oscillator Frequency Temperature Drift	Δf/ΔT	(Exclusive of RC Drift)		250		ppm/°C
Time Base Output Voltage	V_{OTB}	I_{SOURCE} = 1 mA I_{SINK} = 3.2 mA	3.5	4.2 0.25	 0.6	V V
Time Base Output Leakage Current	I_{TBLK}	**RC = Ground**			**5**	**μA**
Timebase Input Voltage	V_{IL} V_{IH}		 **3.5**		**0.8**	**V** **V**
Mod Voltage Level 7240,50,60	V_{MOD}	V^+ = 5V V^+ = 15V		4.0 12		V V
Trigger Input Voltage	V_{TRIG}	**V^+ = 5V** **V^+ = 15V**	**0.8** **0.8**	**1.6** **3.5**	**2.0** **4.5**	**V** **V**
Reset Input Voltage	V_{RST}	**V^+ = 5V** **V^+ = 15V**	**0.8** **0.8**	**1.3** **2.7**	**2.0** **4.0**	**V** **V**
Trigger/Reset Input Current	I_{TRIG} I_{RESET}	-20°C ≤ T_A ≤ +85°C		0.1	10	μA
Max Count Toggle Rate 7240, 7242 7250, 7260	f_t	**V^+ = 2V** **Fixed Counter/** **V^+ = 5V** **Divider Mode** **V^+ = 15V** **50% Duty Cycle Input with Peak to Peak Voltages Equal to V^+ and GND**	**3**	**1** **8** **15**		**MHz** **MHz** **MHz**
Max Count Toggle Rate 7240, 7250, 7260	f_t	**Programmable Divide Mode (Note 2)**	**200**			**kHz**
Carry Out Source **Source Output Current** **Sink Output Current**	I_{COH}	 **V_{OH} = V^+ - 1V** **V_{OL} = +0.4 Volts**	 **300** **3.2**			 **μA** **mA**
Output Saturation Voltage	V_{SAT}	All Outputs except TB Output V^+ = +5V, I_{SINK} = 3.2 mA		0.22	0.4	V
Output Leakage Current	I_{OLK}	V^+ = +5V, per Output			1	μA
Output Sourcing Current 7242	I_{SOURCE}	**V^+ = +5V terminals 2,8,3** **V_{OUT} = V^+ - 1V**	**300**			**μA**
MIN Timing Capacitor	C_t		10			pF
Timing Resistor Range	R_t	V^+ ≤ 5.5V V^+ ≤ 16V	1k 1k		22M 22M	Ω Ω
RC Input Leakage	I_{RC}	**RC = 2.5V**			**10**	**nA**

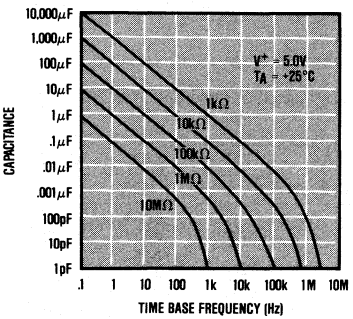
Note 1: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil STD 883C Method 3015.2 Test Circuit).

Note 2: Parameter is Q.A. sample tested.

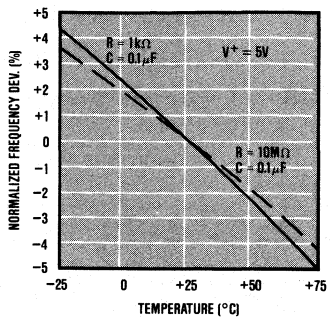
Fixed And Programmable Timer/Counters

Typical Operating Characteristics

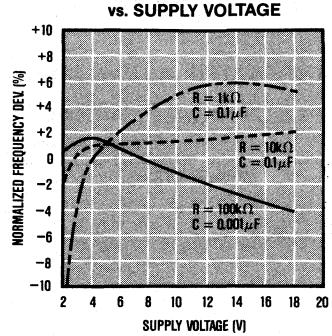
RC OSCILLATOR FREQUENCY vs. R AND C



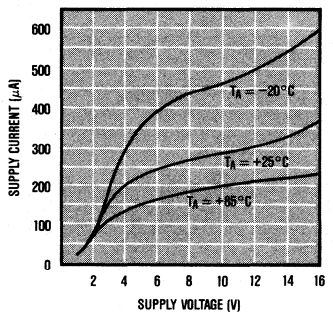
NORMALIZED FREQUENCY vs. TEMPERATURE



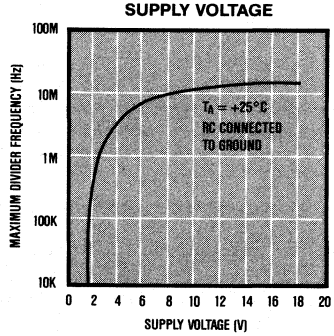
NORMALIZED FREQUENCY vs. SUPPLY VOLTAGE



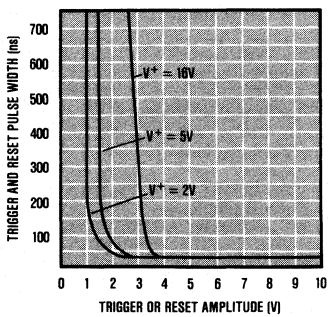
SUPPLY CURRENT vs. SUPPLY VOLTAGE OVER TEMPERATURE



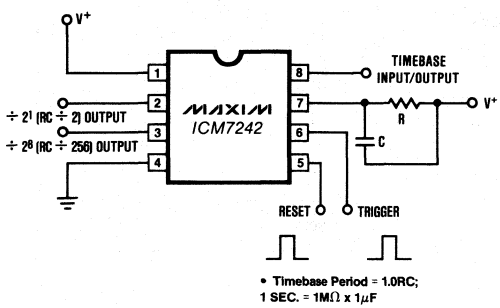
MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



MINIMUM RESET AND TRIGGER PULSE WIDTH vs. AMPLITUDE

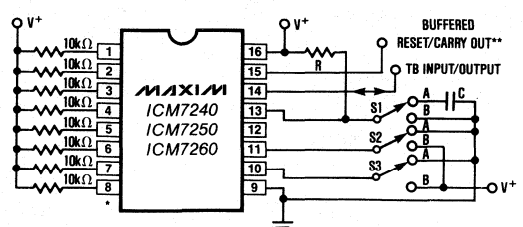


Test Circuits



Note: Outputs ÷ 2^1 and ÷ 2^8 are inverters and have active pullups.

ICM7240/50/60



S1—A = RC Run
B = T. B. Input Run

S2—A = Inactive
B = Trigger

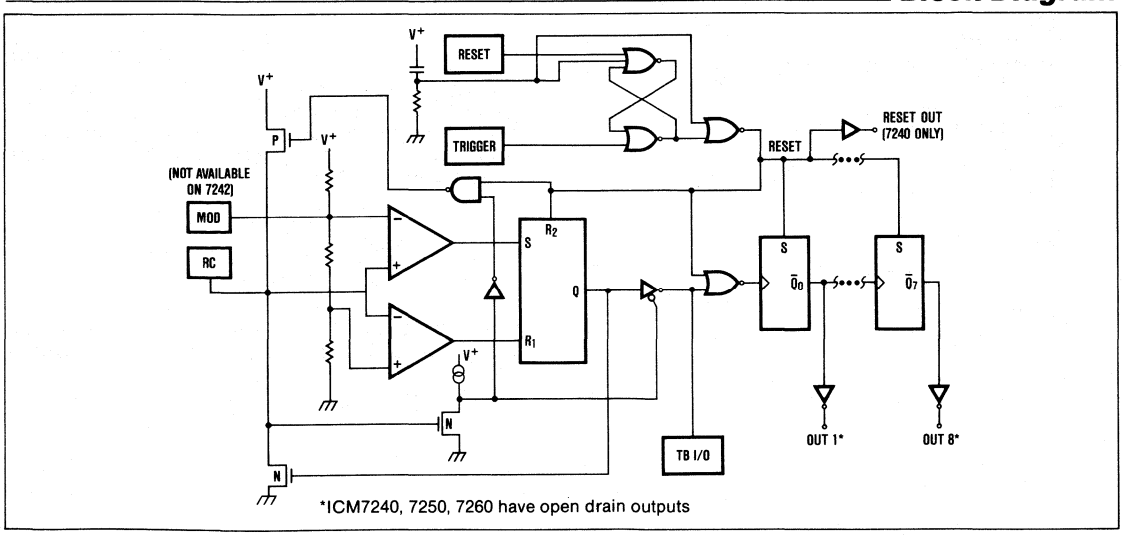
S3—A = Inactive
B = Reset

Note: S1-B inhibits the timebase section, allowing terminal 14 to become the counter input.
***Note:** Terminal 8 is open circuit for 7260.
****Note:** Terminal 15 is open circuit for 7250/60 devices.

Table 1. PIN DESCRIPTIONS

PIN NAME	PIN #		DESCRIPTION
	ICM7240/50/60	ICM7242	
V^+	16	1	Positive power supply pin.
GND	9	4	Ground
RC	13	7	RC timing node. If this pin is grounded, the TB I/O pin is an external clock input. An external resistor and capacitor connected to this pin sets the frequency of the internal oscillator to 1/RC.
Trigger	11	6	The Trigger input sets the internal control flip-flop to the Run state. If the counter is reset and TB I/O is low, a high on Trigger will clock the counter to the all 0s count and counting will begin. If the counter is reset and TB I/O is high, a high level on Trigger will only set the control flip-flop. The counter will clock to the all 0s count on the next falling edge of TB I/O, provided the control flip-flop is set.
Reset	10	5	A high input on Reset while Trigger is low will reset the counter, force all counter outputs high, and stop the counter by resetting the control flip-flop. The Reset input has no effect if Trigger is high.
TB I/O	14	8	The TB I/O pin is an external clock input if the RC pin is grounded. If RC is not grounded the TB I/O pin is the timebase oscillator output. The Maxim TB I/O output is fully buffered and can drive up to 1000pF of capacitance.
Carry Out	15 (ICM 7250/60 only)	—	Carry goes high during the last 10 counts—50 through 59 in the ICM 7260, 90 through 99 in the ICM7250. To cascade two ICM 7250/60s, drive the TB I/O pin of one ICM7250/60 with the Carry Out of the other. (Use the ÷ 128 output to cascade ICM7240 and ICM7242.)
Buffered Reset	15	—	Buffered output of the Reset input of the control flip-flop. (Maxim ICM7240 only)
Counter Outputs	1-8		The ICM7240/50/60 outputs are open drain n-channel outputs which sink current when on and are open circuits when off. These outputs are TTL and CMOS compatible if a pullup resistor is connected to V^+.
Counter Outputs	—	2,3	The ICM7242 outputs are logic outputs which both sink and source currents. The ICM7242 outputs are both TTL and CMOS compatible and do not require pullups. The ÷ 2 output is a square wave at ½ the frequency of the onboard oscillator or external timebase. The ÷ 128/256 output is a square wave with a period 256 times the oscillator or external timebase period. This pin goes high 128 clock cycles after the counter is triggered.
MOD	12	—	Similar to the Control input of an ICM7555, this pin is connected to the resistor string that sets the oscillator thresholds. The internal resistor divider drives the Modulation (MOD) pin to 80% of V^+. Varying the MOD voltage will adjust the oscillator frequency.

Block Diagram



*ICM7240, 7250, 7260 have open drain outputs

Fixed And Programmable Timer/Counters

Circuit Description

The timing cycle is controlled by the internal control flip-flop. This set-reset flip-flop is set to the Run state by a high level on the Trigger input. A high level on the Reset input puts the control flip-flop into the Reset state, provided Trigger is low. Trigger overrides Reset: if both Trigger and Reset are high the control flip-flop is set to the Run state.

When the control flip-flop is set to the run state the counter is set to all 0s (all outputs low), the timebase input is also enabled, and the counter will increment with each negative-going edge at TB I/O.

A high level on the Reset input while Trigger is low resets the control flip-flop. The flip-flop resets the counter forcing all the counter outputs high, inhibiting the counter from being incremented, and unless in the external timebase mode, turns on the internal pullup connected to the RC pin.

The RC oscillator period is set by an external resistor and capacitor. The external resistor charges the capacitor to 80% of V^+. This voltage is detected at the RC terminal, TB I/O goes low, the counter increments one count, and the internal discharge transistor rapidly discharges the capacitor to 45% of V^+. When the capacitor voltage goes below 45% of V^+ the internal discharge transistor turns off, TB I/O goes high, and the external capacitor again starts to charge through the external resistor. The period of each oscillator cycle is 1.0 RC.

In many applications, one or more of the counter outputs can be used to reset the counter after a programmed count is completed. With no outputs connected back to the Reset pin, the circuit operates in the astable (free running) mode.

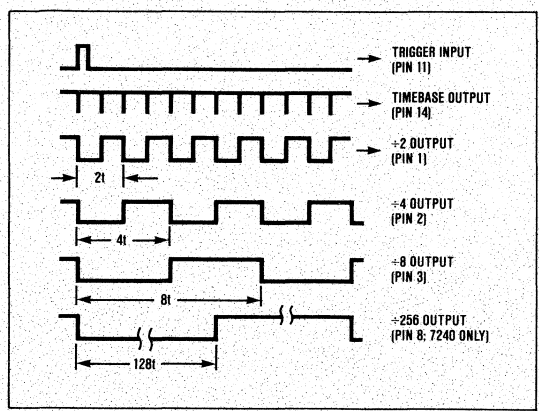
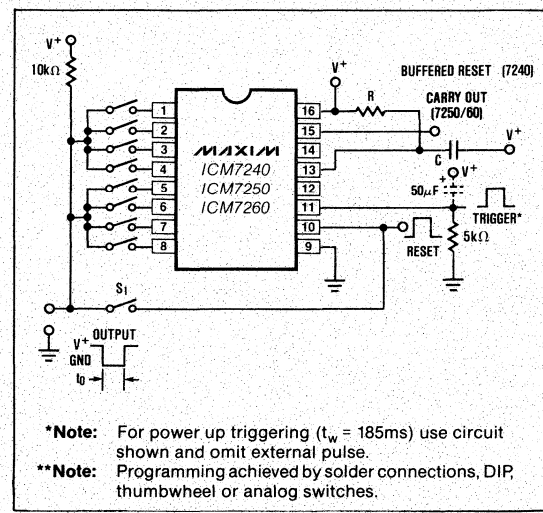


Figure 1. Timing Diagram for ICM7240/50/60.

Applications

Programmable Time Delay

Figure 2 shows a basic programmable time delay. When the circuit is triggered all outputs go low. When the programmed count is reached, the Reset input is pulled high by the 10kΩ resistor, resetting the counter. The programming can be achieved by using either mechanical switches such as thumbwheel or DIP switches, or analog switches such as the CD4016 and CD4066.



**Note: For power up triggering (t_w = 185ms) use circuit shown and omit external pulse.

**Note: Programming achieved by solder connections, DIP, thumbwheel or analog switches.

Figure 2. Generalized Circuit for Timing Applications (Switch S_1 open for astable operation, closed for monostable operation)

Output Count Programming (ICM7240/50/60)

The counter outputs on the ICM7240/50/60 are open-drain-channel FETs, enabling a "wired-OR" connection to be achieved by shorting together the desired outputs with a common pull-up resistor. In this way, the timing cycle can be programmed from:

1RC to 255RC (ICM7240)
1RC to 99RC (ICM7250)
1RC to 59RC (ICM7260)

Programming the ICM7240/50/60 can achieved by hard wiring, DIP switches, or standard thumbwheel switches.

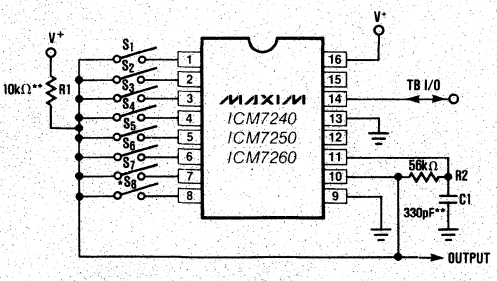
ICM7242 Counter Outputs

The ICM7242 is a non-programmable timer/counter. The outputs on the ICM7242 are inverters which both source and sink current, unlike the open drain N-channel outputs of the ICM7240/50/60 which only sink current. The ICM7242 output inverters eliminate the need for external pull-up resistors.

Outputs on pins 2 and 3 are $\div 2$ and $\div 2^8$ respectively. To use the 8 bit counter without the timebase, connect pin 7 (RC) to ground and drive pin 8 (TB I/O) with an external timebase. For monostable applications connect the $\div 2^8$ output to the reset pin.

Programmable Divider

With the addition of an RC network betweeen the Reset and Trigger inputs, the circuit of Figure 3 becomes a programmable divider. The output period is N times the oscillator (or external input) period, where N is the number programmed into the thumbwheel switches. The 56kΩ and 30pF RC network drives the Trigger high approximately 7μs after Reset goes high, retriggering the counter and starting the cycle again. For high speed operation the capacitor should be reduced to 39pF and the 10kΩ pullup resistor reduced to 2.2kΩ.



* **Note:** S_2 not used on ICM7260.
****Note:** For high-speed operation replace resistor R1 with 2.2 kΩ and capacitor C1 with 39pF.

Figure 3. Programming the Counter Section of the ICM7240/50/60

Competitive Comparison

Maxim's ICM7240/42/50/60 devices are upwardly compatible with Intersil's devices. The counters used in Maxim's parts are synchronous versus the ripple-type used in Intersil's parts. In the programmable divider mode, the maximum frequency of operation is limited by the propagation delay across the counter and the reset delay of the flip-flop. These delays must be less than one half the timebase period, for reliable operation.

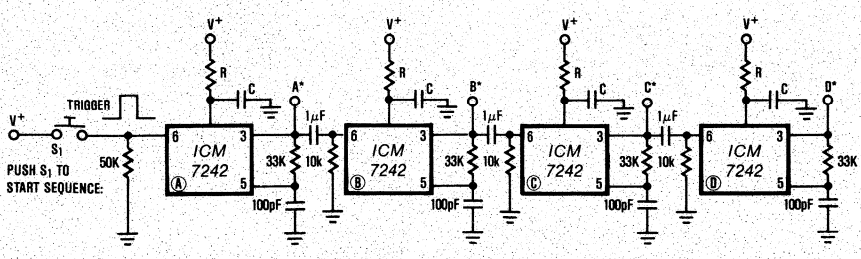
Maxim's ICM7240 has a Buffered Reset Output on pin 15 versus a No Connection on Intersil's part. This output is a buffered output from the reset line for the counters contained within the ICM7240, so that when the device is being used in the programmable divider mode, the output can be used as the divider count output.

When Maxim's devices are operated with the time-base inhibited (RC pin grounded) and the counter is reset, the supply current for the Maxim part is guaranteed to be no more than 10μA versus a possible 8mA at +5Volts and 20mA at +16Volts for the Intersil part.

The TB I/O output has significantly improved drive capability and can drive up to 1,000pF of load capacitance versus 50pf for the Intersil part. Maxim's devices are also less sensitive than Intersil's to the rate of change of the input waveform at TB I/O when in the external clock mode. This reduces the possibility of false triggering on slow falling clock waveforms.

Sequence Timer

Figure 4 shows how to cascade multiple counters to perform more complex control functions.



***Note:** Select RC values to desired "ON time" for each ICM7242.

Figure 4. Sequence Timer Using ICM7242

Fixed And Programmable Timer/Counters

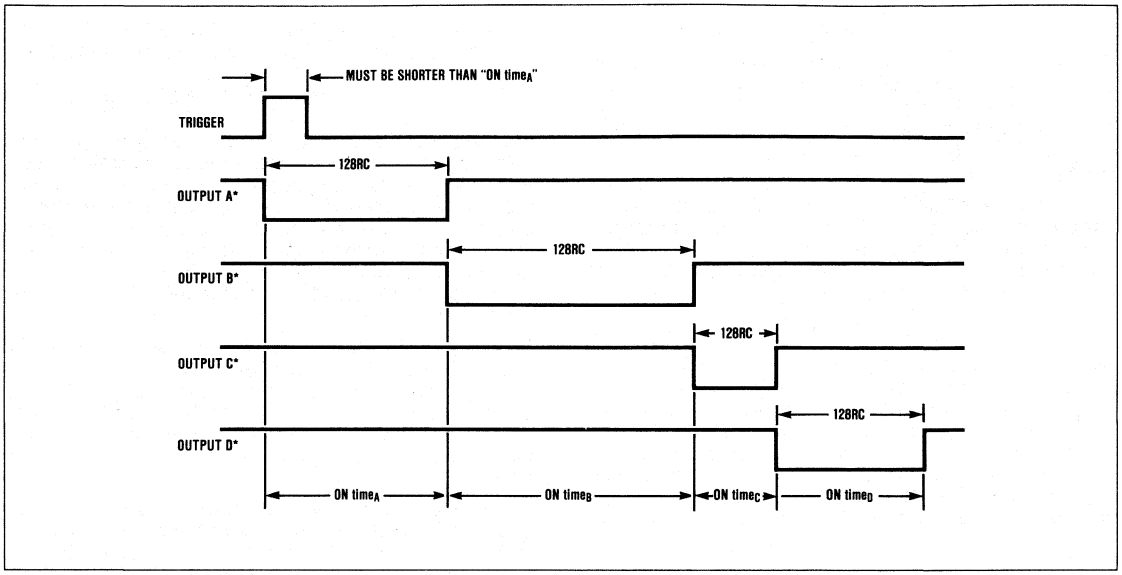
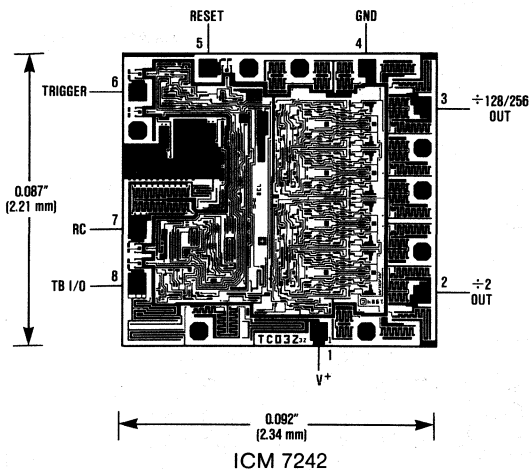
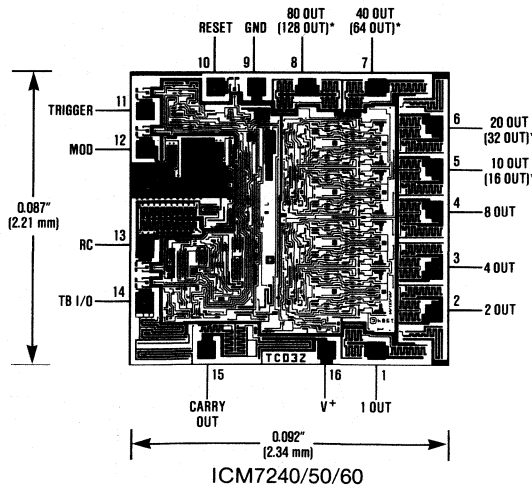


Figure 5. Timing Diagram for Sequence Timer of Figure 4.

Chip Topography



ICM 7242



ICM7240/50/60

***Note:** Pin descriptions in parentheses refer to ICM7240.

General Description

The IH5341 and the IH5352 are dual and quad, single pole single throw (SPST) switches designed specifically for switching RF and video signals. Maxim's IH5341 and IH5352 incorporate an enhanced series-shunt-series structure, providing 70dB of OFF isolation and cross coupling rejection (an additional 10dB compared with other manufacturers' products).

Both devices can be operated with supplies ranging from ±5V to ±15V. The switches typically have a t_{ON} = 160ns and a t_{OFF} = 70ns, assuring break-before-make switching. The channel thruput resistance of 50Ω provides excellent matching to video impedances. In the D.C. state, with switches being either on or off, power supply quiescent currents are typically 100nA. This limits the quiescent current drain to 3μ watts—ideal for portable equipment.

Applications

These devices are used in applications requiring the routing, blocking or switching of video or RF signals such as:

Winchester Disk Drives
Commercial TV Cameras
Video Special Effects
Low Power RF Switching
Radar Switching
Mil and Space Communications

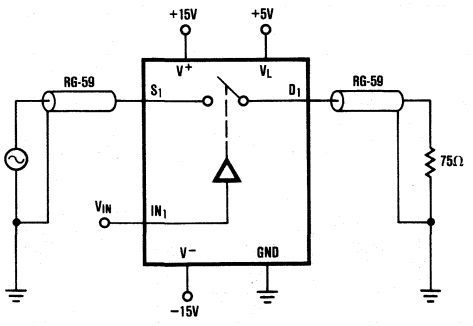
Features

- **"OFF" Isolation ≥ 70dB @ 10MHz**
- **Cross Coupling Isolation ≥ 70dB @ 10MHz**
- **$r_{ds(on)}$ < 75Ω, < 3dB Loss from DC to 100 MHz**
- **±5V to ±15V Operating Supply Range**
- **Supply Currents < 1μA**
- **Fast, Break-Before-Make Switching (70ns/160ns typ.)**
- **Monolithic, Low Power CMOS Design**

Ordering Information

PART	TEMP. RANGE	PACKAGE
IH5341CPD	0°C to +70°C	14 Lead Plastic DIP
IH5341IJD	-20°C to +85°C	14 Lead CERDIP
IH5341ITW	-20°C to +85°C	10 Lead TO-100
IH5341MJD	-55°C to +125°C	14 Lead CERDIP
IH534IMTW	-55°C to +125°C	10 Lead TO-100
IH5341C/D	0°C to 70°C	Dice
IH5352CPE	0°C to +70°C	16 Lead Plastic DIP
IH5352IJE	-20°C to +85°C	16 Lead
IH5352MJE	-55°C to +125°C	16 Lead CERDIP
IH5352C/D	0°C to 70°C	Dice

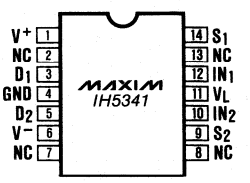
Typical Operating Circuit



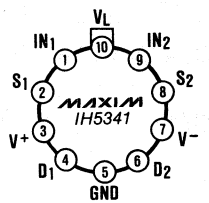
75Ω Video Switch
(Only one channel shown)

Pin Configuration

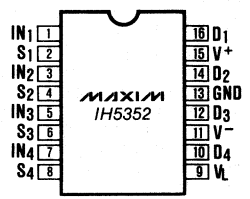
Top View



14 Lead DIP



10 Lead TO-100



16 Lead DIP

Dual/Quad RF/Video Switches

ABSOLUTE MAXIMUM RATINGS

Supply Voltages V^+ and V^- ..... ±17V
Current in any Terminal 50mA
Analog Input Voltage ..... V^+ to V^-
Operating Temperature Range
(M Version) -55°C to +125°C
(I Version) -20°C to +85°C
(C Version) 0°C to +70°C

Power Dissipation 250mW
(Derate 7.5mW/°C above 25°C)
Storage Temperature Range ..... -65°C to +160°C
Logic Control Voltage ..... V^+ to V^-
Voltage on V_L Pin ..... V^+ to V^-
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = +15V, V_L = +5V, V^- = -15V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	TYP	M GRADE DEVICE			I/C GRADE DEVICE			UNITS
				-55°C	+25°C	+125°C	-20/ 0°C	+25°C	+85/ +70°C	
Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	 V^+ V_L V^-	 (Note 3)	 4.5 > 16 4.5 > V^+ -4 > -16		 5 to 15 5 to V^+ -5 to -15			 5 to 15 5 to V^+ -5 to -15		V
Switch "ON" Resistance (Note 4)	$r_{ds(ON)}$	V_D = -5V to +5V I_S = 10 mA, V_{IN} = 2.4V V_D = -15V to +15V		75 125	75 125	100 175	75 150	75 150	100 175	Ω
Switch "ON" Resistance	$r_{ds(ON)}$	V^+ = V_L = 5V, V_{IN} = 3V V^- = -5V, V_D = ±5V		250	250	350	300	300	350	
On Resistance Match		I_S = 10mA, V_D = ±5V	5							
Switch "OFF" Leakage (Notes 2 and 4)	$I_{D(OFF)}$ or $I_{S(OFF)}$	$V_{S/D}$ = +5V to -5V V_{IN} = 0.8V $V_{S/D}$ = +14V to -14V		0.1 0.2	0.1 0.2	20 50	0.5 1.0	0.5 1.0	20 100	nA
Switch "ON" Leakage	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = +5V or -5V V_{IN} = 2.4V V_D = +14V to -14V		0.3 0.5	0.3 0.5	50 100	1.0 1.0	1.0 5.0	40 100	
Input Logic Current	I_{IN}	V_{IN} > 2.4V or < 0	0.001	1	1	10	1	1	10	μA
Positive Supply Quiescent Current	I^+	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	
Negative Supply Quiescent Current	I^-	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	
Logic Supply Quiescent Current	I_L	V_{IN} = 0V or +5V (Note 5)	0.01	1	1	10	1	1	10	

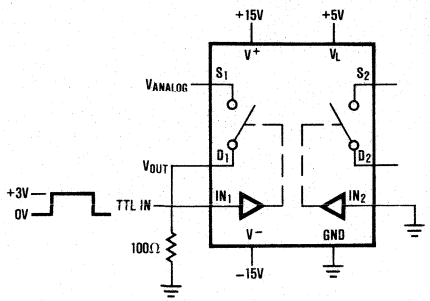
AC ELECTRICAL CHARACTERISTICS

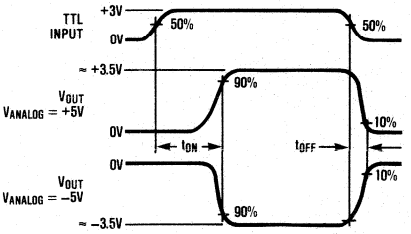
V^+ = +15V, V_L = +5V, V^- = 0V, T_A = 25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switch "ON" Time	t_{ON}	See Figure 1		160	300	ns
Switch "OFF" Time	t_{OFF}	See Figure 1		70	150	
"OFF" Isolation Rejection Ratio	OIRR	See Figure 2 (Note 6)	70	80		dB
Cross Coupling Rejection Ratio	CCRR	See Figure 3 (Note 6)	70	80		
Frequency where $r_{ds(ON)}$ = 0.7 x DC		(Note 6)	100			MHz

Note 1: Typical values are not tested in production. They are given as a design aid only.
Note 2: Positive and negative voltages applied to opposite sides of switch, in both directions successively.
Note 3: These are the operating voltages at which the other parameters are tested, and are not directly tested.
Note 4: The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
Note 5: Maximum values shown are for the dual (IH5341). They are doubled for the quad (IH5352).
Note 6: All AC parameters are sample tested only. Test circuits should be built on copper clad ground plane board, with correctly terminated coax leads, etc.
Note 7: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C Method 3015.2 Test Circuit)

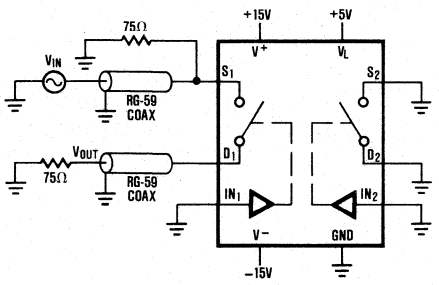
Test Circuits





Note: Only one channel shown. Others act identically.

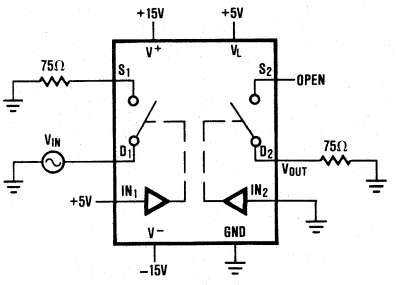
Figure 1. Switching Time Test Circuit and Waveforms



V_{IN} = ±5V (10V_{p-p}) @ f = 10MHz OIRR = 20 $\log\frac{V_{IN}}{V_{OUT}}$

Note: Only one channel shown. Others act identically.

Figure 2. OFF Isolation Test Circuit

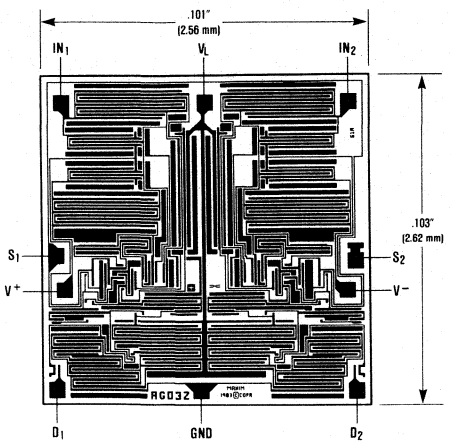


V_{IN} 225mVrms @ f = 10MHz

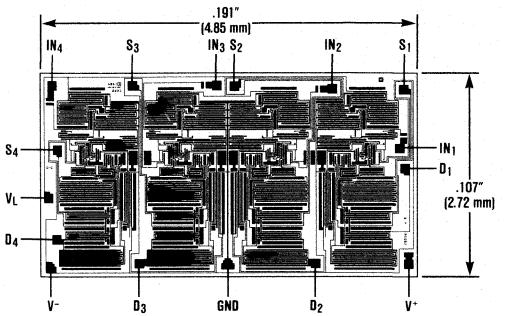
CCRR = 20 $\log\frac{V_{IN}}{V_{OUT}}$

Figure 3. Cross-Coupling Rejection Test Circuit

Chip Topography



IH5341 (Dual SPST)



IH5352 (Quad SPST)

Low Power, 3½ Digit A/D Converter With Display Hold

General Description

The Maxim MAX136 is a monolithic analog to digital converter with very high input impedance. It differs from the Maxim ICL7136 in that the MAX136 provides a Hold pin, which makes it possible to hold or "freeze" a reading. The MAX136 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external drive circuitry. With minor external component changes, it is pin compatible with the ICL7116 but with significantly reduced power consumption, making the MAX136 a superior device for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. True differential inputs allow direct measurements of bridge transducer outputs or load cells. The zero-integrator phase eliminates overrange hangover and hysteresis effects. The MAX136 offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1μV/°C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

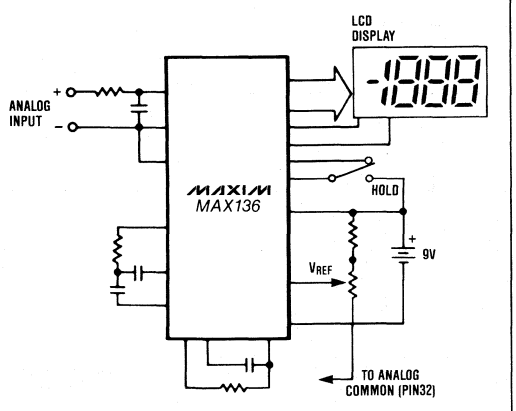
Features

- **Power dissipation less than 1mW—9V battery life 8000 hours typical**
- **Hold pin allows indefinite display hold**
- **Guaranteed first reading recovery from overrange**
- **On board Display Drive Capability—no external circuitry required**
- **High Impedance CMOS Differential inputs**
- **Low Noise (< 15μV p-p) without hysteresis or overrange hangover**
- **Clock and Reference On-Chip**
- **Zero Input Gives Zero Reading**
- **True Polarity Indication for Precision Null Applications**
- **Key Parameters Guaranteed over Temperature**

Ordering Information

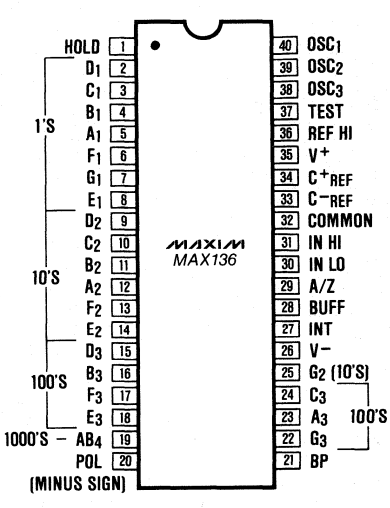
PART	TEMP. RANGE	PACKAGE
MAX136CPL	0°C to +70°C	40 Lead Plastic DIP
MAX136CJL	0°C to +70°C	40 Lead CERDIP
MAX136CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MAX136C/D	0°C to +70°C	Dice

Typical Operating Circuit



(Detailed Circuit Diagram—See 3rd page)

Pin Configuration



See last page for Plastic Chip Carrier Pin Configuration

Low Power, 3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input, Hold Input ..... TEST to V^+

Power Dissipation (Note 2)
Cerdip Package 800mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) ..... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±1mA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 9V; T_A = 25°C; f_{CLOCK} = 48kHz; test circuit - Figure 1 unless noted.)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 -000.0 -000.0	 ±000.0 ±000.0	 +000.0 +000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	 999 998	 999/1000 999/1000	 1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ ≅ 200.0mV T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C (Note 6)	-1	 ±0.2 ±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 7)	V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		50		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		µV
Input Leakage Current	V_{IN} = 0, T_A = 25°C (Note 3) 0° ≤ T_A ≤ 70°C		1 20	10 200	pA
Zero Reading Drift	V_{IN} = 0, 0° ≤ T_A ≤ 70°C (Note 6)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ 70°C (Ext. Ref. 0ppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current	V_{IN} = 0 T_A = 25°C 0° ≤ T_A ≤ 70°C		80	150 200	µA
Analog Common Voltage (with respect to Pos. supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply	250kΩ between Common & Pos. Supply		75		ppm/°C
Input Resistance, Pin 1			1000		Ω
V_{IL}, Pin 1				TEST +1.5	V
V_{IH}, Pin 1		V^+ -1.5			V
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V^+ to V^- = 9V (Note 8)	4	5	6	V
Test Pin Voltage	With Respect to V^+	4	5	6	V
Overload Recovery Time (Note 5)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 3: Test condition is V_{IN} applied between pins IN-HI and IN-LO, i.e., 1MΩ resistor in Figures 1 and 2.
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883C, Method 3015 .2)
Note 5: Number of measurement cycles for display to give accurate reading.
Note 6: 1MΩ resistor is removed in Figures 1 and 2.
Note 7: Refer to "Differential Input" discussion (See Maxim's ICL7136 data sheet).
Note 8: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Low Power, 3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim MAX136 3½ digit A/D converter is similar to the Maxim ICL7136 except for the addition of a Hold pin. For a detailed product description, and applications information (other than the operation of the Hold pin described below), refer to Maxim's ICL7136 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test. The MAX136 continuously performs conversions, independent of the Hold input. When the Hold input is at V^+ the display latch pulse is inhibited, and the display latches are not updated; when the Hold input is low or at the Test voltage, the display is updated at the end of each conversion. The MAX136 maintains low power dissipation even during display hold by eliminating the pull-down resistor between Hold and Test present on the ICL7116. The Hold input is CMOS compatible, and can also be driven by a switch connected between Test and V^+ (Figure 1).

Unlike the ICL7136, the MAX136 does not have a Reference low input. Apply the reference voltage between Reference high (REF HI) and Common.

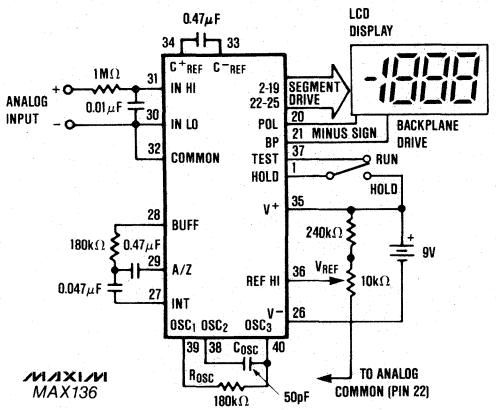


Figure 1. Maxim MAX136 Typical Operating Circuit, 200mV Full Scale.

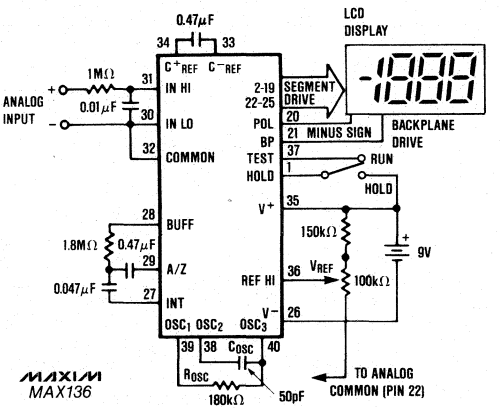
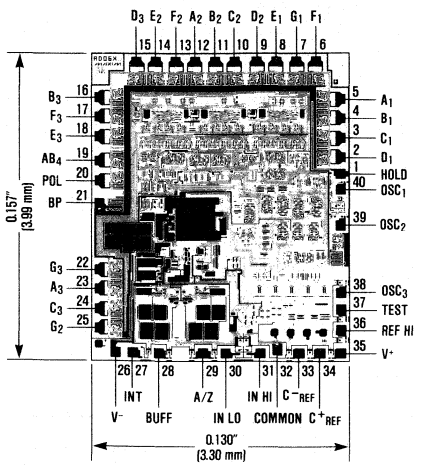
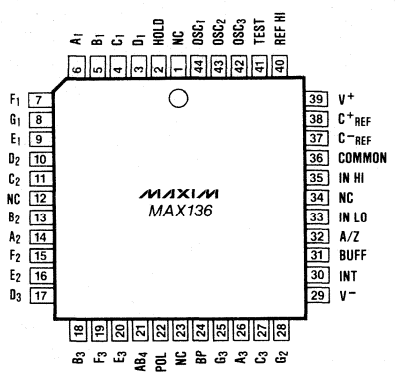


Figure 2. Maxim MAX136 Typical Operating Circuit, 2.0V Full Scale.

Chip Topography



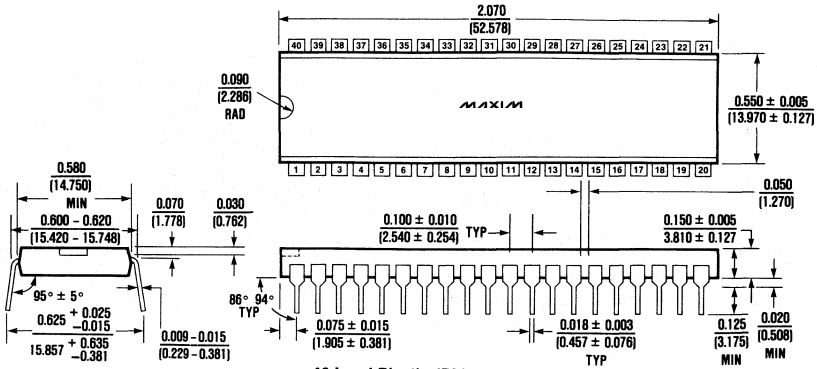
Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

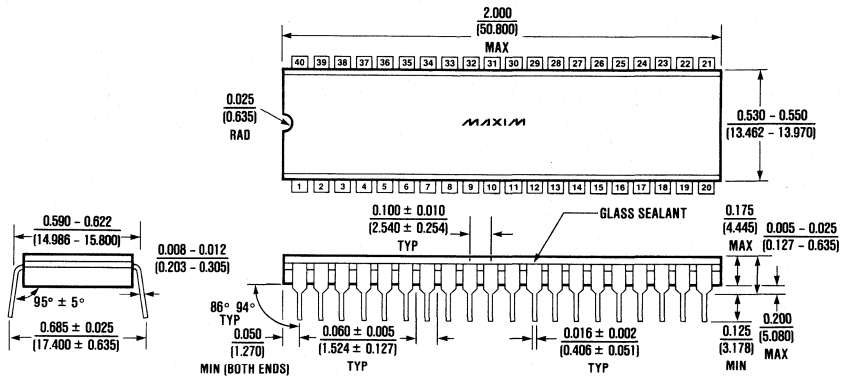
Low Power, 3½ Digit A/D Converter With Display Hold

Package Information



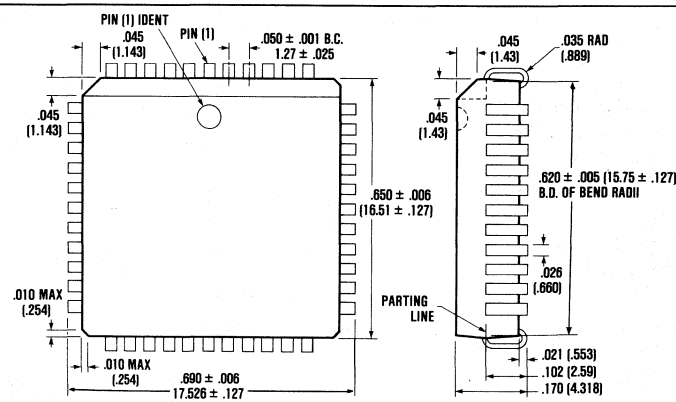
40 Lead Plastic (PL)

θ_{JA} = 100°C/W, θ_{JC} = 45°C/W



40 Lead Cerdip (JL)

θ_{JA} = 45°C/W



44 Lead Plastic Chip Carrier (Quad Pack) (QH)

θ_{JA} = 60°C/W

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

+5V Powered Dual RS-232 Transmitter/Receiver

General Description

The MAX232 is a dual RS-232 receiver/transmitter that meets all EIA RS-232C specifications while using only a +5V power supply. Significantly simplifying system design by removing the need for power supply voltages other than +5V, the MAX232 has two onboard charge pump voltage converters which generate +10V and -10V power supplies from a single 5V power supply.

The MAX232 contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS input levels into ±9V RS-232 outputs.

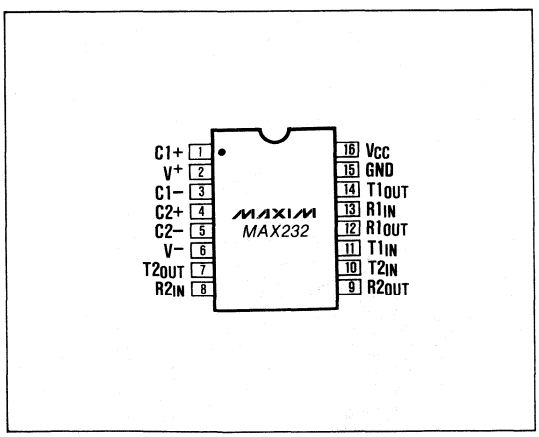
The other two level translators are RS-232 receivers, which convert RS-232 inputs to 5V TTL/CMOS output levels. These receivers have a nominal threshold of 1.3V, a typical hysteresis of 0.5V, and can operate with up to ±30V inputs.

Typical Applications

The MAX232 is suitable for all RS-232C communication links. It is particularly useful where the ±12V power supplies required for other RS-232 drivers are not available. The power supply section of the MAX232 can be used as a voltage quadrupler for input voltage up to 5.5V.

Computers
Peripherals
Instruments
Modems
Battery Powered Systems

Pin Configuration



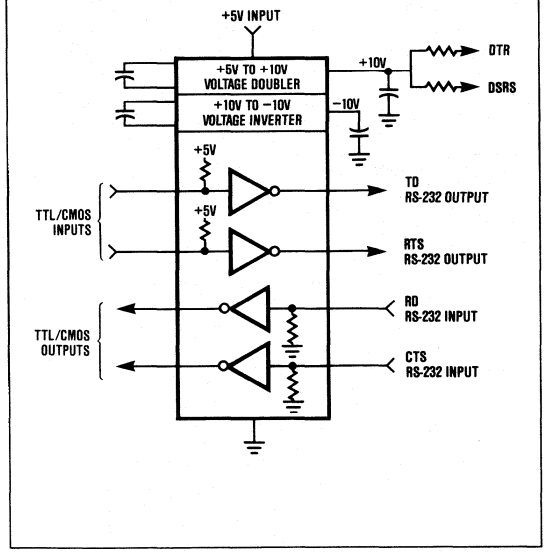
Features

- Operates from Single 5V Power Supply
- Meets all RS-232C Specifications
- 2 Drivers and 2 Receivers
- Onboard Voltage Quadrupler
- ±30V Input Levels
- ±9V Output Swing with +5V Supply
- Low Power CMOS: 5mA

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX232CPE	0°C to +70°C	16 Pin Plastic DIP
MAX232CWE	0°C to +70°C	16 Pin Small Outline
MAX232C/D	0°C to +70°C	Dice
MAX232EPE	-40°C to +85°C	16 Pin Plastic DIP
MAX232EWE	-40°C to +85°C	16 Pin Small Outline
MAX232EJE	-40°C to +85°C	16 Pin CERDIP
MAX232MJE	-55°C to +125°C	16 Pin CERDIP

Typical Operating Circuit



+5V Powered Dual RS-232 Transmitter/Receiver

ABSOLUTE MAXIMUM RATINGS

V_{CC} 6V
V^+ 12V
V^- 12V
Input Voltages
$T1_{IN}$, $T2_{IN}$ ..... -0.3 to (V_{CC} + 0.3V)
$R1_{IN}$, $R2_{IN}$ ..... ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ ..... (V^++0.3V) to (V^--0.3V)
$R1_{OUT}$, $R2_{OUT}$ ..... -0.3V to (V_{CC} + 0.3V)

Short Circuit Duration
V^+ ..... 30 seconds
V^- ..... 30 seconds
$T1_{OUT}$, $T2_{OUT}$ ..... continuous
Power Dissipation
CERDIP 500mW
derate 9.5mW/°C above 70°C
Plastic DIP 375mW
derate 7mW/°C above 70°C
Small Outline (SO) 375mW
derate 7mW/°C above 70°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

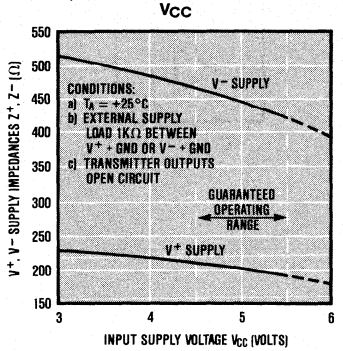
ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V±10%, T_A = operating temperature range, test circuit unless otherwise noted)

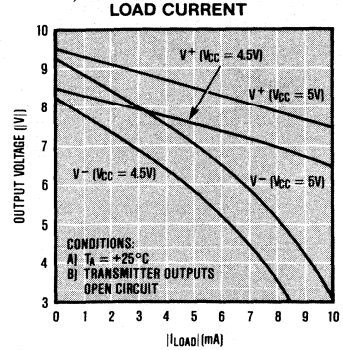
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage Swing	$T1_{OUT}$, $T2_{OUT}$ loaded with 3kΩ to ground.	±5V	±9	±10	V
Power Supply Current			5	10	mA
Input Logic Threshold Low	T_{IN}, $T2_{IN}$			0.8	V
Input Logic Threshold High	$T1_{IN}$, $T2_{IN}$	2.0			V
Logic Pullup Current	$T1_{IN}$, $T2_{IN}$ = 0V		15	200	µA
RS-232 Input Voltage Operating Range		-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V	0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V		1.7	2.4	V
RS-232 Input Hysteresis		0.2	0.5	1.0	V
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA	3.5			V
Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		µs
Instantaneous Slew Rate	C_L = 10pF, R_L = 3-7kΩ, T_A = 25°C (Note 1)			30	V/µs
Transition Region Slew Rate	R_L=3kΩ, C_L=2500pF Measured from 3V to -3V or -3V to +3V		3		V/µs
Output Resistance	V^+ = V^+ = 0V, V_{OUT} = ±2V	300			Ω
RS-232 Output Short Circuit Current			±10		mA

Note 1: Sample tested.

V+, V- LOAD IMPEDANCES VS. VCC



V+, V- OUTPUT VOLTAGES VS. LOAD CURRENT



Detailed Description

The MAX232 has three sections: a dual transmitter, a dual receiver, and a +5V to ±10V dual charge pump voltage converter.

+5 to ±10V Dual Charge Pump Voltage Converter

The MAX232 power supply section contains two charge pumps. The first uses external capacitor C1 to double the +5V input to +10V, with an output impedance of approximately 200 ohms.

The second charge pump uses external capacitor C2 to invert the +10V to -10V, with an overall output impedance of 450Ω (including the effects of the +5 to +10 voltage doubler impedance).

The test circuit uses 22μF capacitors for C1-C4, but the value is not critical. Normally these capacitors are low cost aluminum electrolytic capacitors, or tantalum if size is critical.

Increasing the value of C1 and C2 to 47μF will lower the output impedance of the +5V to +10V doubler by about 5 ohms and the +10V to -10V inverter by about 10 ohms. Increasing the value of C3 and C4 lowers the ripple on the ±10V power supplies, thereby lowering the 16kHz ripple on the RS-232 outputs. The value of C1-C4 can be lowered to 1μF in systems where size is critical, at the expense of an additional 20 ohms impedance in the +10V output, 40 ohms additional impedance at the -10V output, and 250mV of 16kHz ripple on V^-.

Transmitter Section

Each of the two transmitters is a CMOS inverter powered by the ±10V internally generated supplies. The input is TTL and CMOS compatible, with a logic threshold of about 26% of V_{CC} (1.3V for 5V V_{CC}). The input of an unused transmitter section can be left unconnected; an internal 400 kilohm pullup resistor connected between the transmitter input and V_{CC} will pull the input high, forcing the unused transmitter output low.

The open circuit output voltage swing is from (V^+ - 0.6V) to V^-. The output swing is guaranteed to meet the RS-232C specification of ±5V minimum output swing under the worst case conditions of both transmitters driving the 3 kilohm minimum load impedance, the V_{CC} input at 4.5V, and maximum allowable ambient temperature. Typical voltage swing with 5 kilohm loads and V_{CC} = 5V is ±9V.

As required by the EIA RS-232C specification, the slew rate at the output is limited to less than 30V/μs; and the powered-down output impedance will be a minimum of 300 ohms with ±2V applied to the outputs with V_{CC}=0V.

The outputs are short circuit protected and can be short circuited to ground indefinitely.

Receiver Section

The two receivers fully conform to RS-232C specifications: their input impedance is between 3 kilohms and 7 kilohms, they can withstand up to ±30V inputs (either with or without 5V power applied), and their input switching thresholds are within the ±3V limits of the RS-232C specification. To ensure compatibility with either RS-232 inputs or TTL/CMOS inputs, the MAX232 receivers have a V_{IL} of 0.8V and V_{IH} of 2.4V. The receivers have 0.5V of hysteresis to improve noise rejection.

The TTL/CMOS compatible output of the receiver will be low whenever the RS-232 input is greater than 2.4V. The receiver output will be high when the input is floating or driven between +0.8V and -30V.

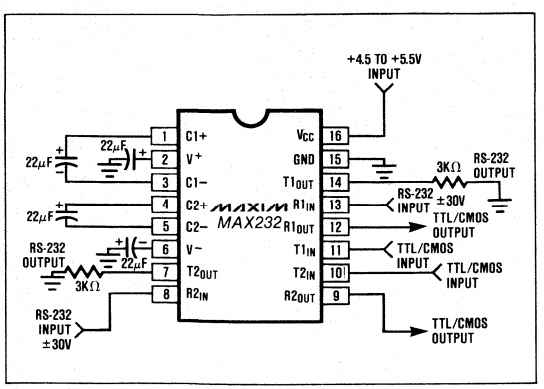


Figure 1. Test Circuit

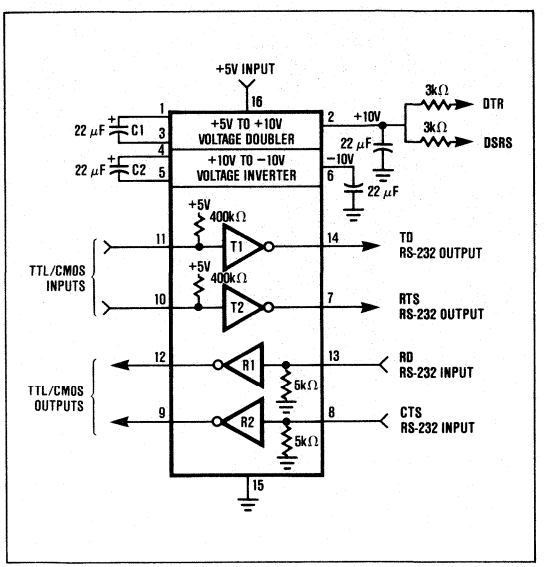
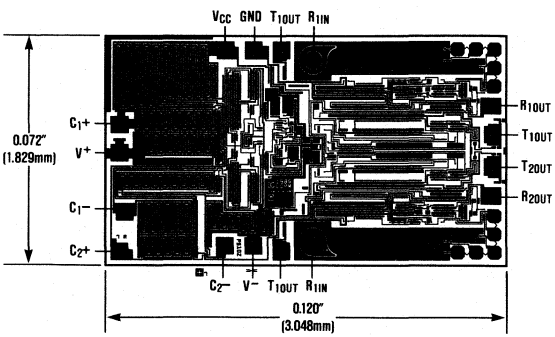


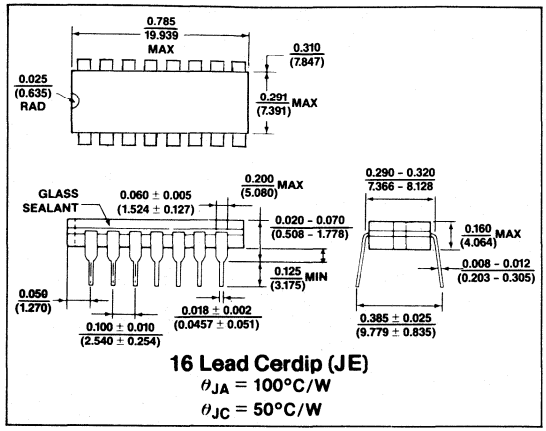
Figure 2. Typical Application +5V Powered RS-232 Dual Transmitter/Receiver

+5V Powered Dual RS-232 Transmitter/Receiver

Chip Topography



Package Information



16 Lead Cerdip (JE)

θ_{JA} = 100°C/W

θ_{JC} = 50°C/W

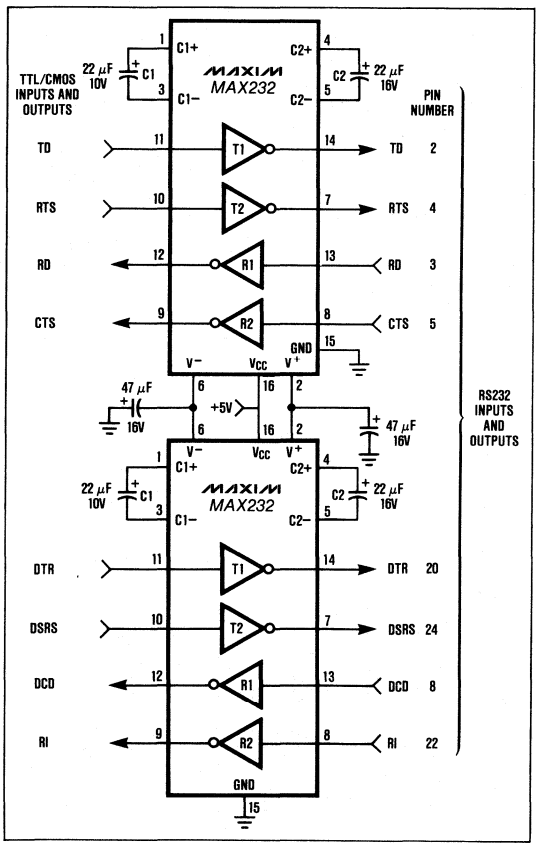
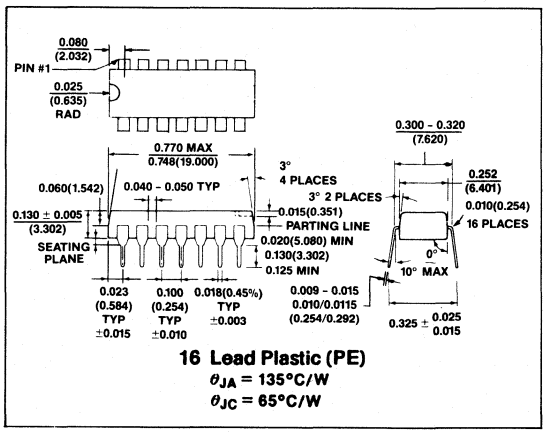


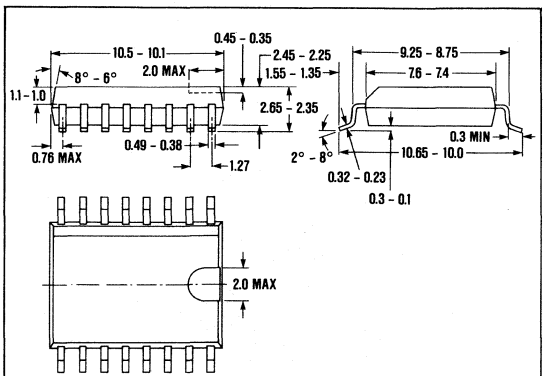
Figure 3. Combining 2 MAX232 For 4 RS-232 Inputs and RS-232 Outputs



16 Lead Plastic (PE)

θ_{JA} = 135°C/W

θ_{JC} = 65°C/W



16 Lead Small Outline, Wide (WE)

MAXIM

±15 Volt Chopper Stabilized Operational Amplifier

General Description

The MAX420, 421, 422, and 423 are a series of ±15V CMOS chopper-stabilized amplifiers, designed for high accuracy amplification, signal conditioning and instrumentation applications. These devices offer input offset and drift specification superior to previous "precision" bipolar amplifiers and monolithic choppers. The maximum offset is 5.0μV while the guaranteed drift limit is 0.05μV/°C.

The combination of ±15 volt operation, low power, and standard op-amp pin configuration allows these devices to virtually "plug-in" replace conventional lower-performance amplifiers. The only additional components required are two external capacitors. A wide input voltage range specification, that includes the negative supply, allows for the amplification of signals including ground in single-supply applications.

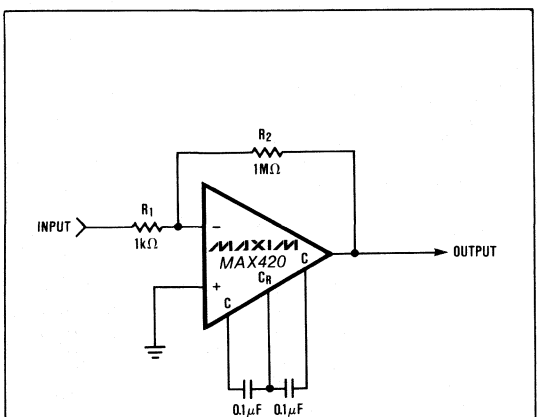
The MAX420 (8 pin) and MAX421 (14 pin) have a maximum supply current of 2mA. The MAX422 (8 pin) and MAX 423 (14 pin) are low power amplifiers with a maximum current of 0.5mA.

Applications

Precision Amplifiers
Signal Conditioning for:
- Thermocouples
- Strain Gauges, Load Cells
- Platinum Temperature Sensors
- Thermistors, Bridges

High Accuracy Data Acquisition
D.C. Stabilization of Amplifiers and Systems

Typical Operating Circuit



Inverting Amplifier

Features

- 5μV Max Offset Voltage
- ±15V Supply Operation
- Input Voltage Range: +12V to -15V
- Low Input Noise: 0.3μV_{p-p} (DC - 1Hz)
- High Gain, CMRR, PSRR: 120dB
- Low Power CMOS Design: 0.5mA Max Supply Current (MAX422/423)
- Low Input Bias Current: 30pA Max

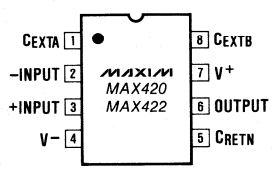
Ordering Information

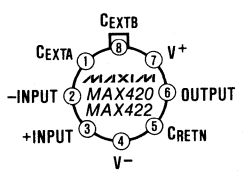
PART	TEMP. RANGE	PACKAGE
MAX420CPA	0°C to +70°C	8 Lead Plastic DIP
MAX420EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX420MTV	-55°C to +125°C	TO-99 Can
MAX421CPD	0°C to +70°C	14 Lead Plastic DIP
MAX421C/D	0°C to +70°C	Dice
MAX421EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX421MJD	-55°C to +125°C	14 CERDIP
MAX421M/D	-55°C to +125°C	Dice

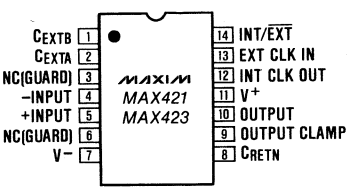
(Ordering information continued on last page)

Pin Configuration

Top View







NC = No internal connection.

±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage ..... (V^+ + 0.3) to (V^- – 0.3) V
Storage Temperature Range ..... -65°C to 160°C
Operating Temperature Range ..... See Note 1
Lead Temperature (Soldering, 10 sec) ..... 300°C
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite

Current Into Any Pin 10mA
Continuous Total Power Dissipation (T_A = +25°C)
CERDIP Package 500mW
Plastic Package 375mW
TO-99 ..... 250mW

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS MAX420, MAX421

(V^+ = +15V, V^- = –15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	C E,M		±1 ±1	±10 ±5	µV µV
		Over Temperature Range (Note 1, 2)	C E,M		±2 ±2	±20 ±10	µV µV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Over Temperature Range (Note 1, 2)	E,M		0.02	0.05	µV/°C
Input Bias Current	I_B	T_A = +25°C	C E,M		10 10	100 30	pA pA
		Over Temperature Range (Note 1)	C E M		30 35 0.5	 5	pA pA nA
Input Offset Current	I_{OS}	T_A = +25°C	C E,M		15 15	200 60	pA pA
		Over Temperature Range (Note 1)	C E M		30 50 0.5	 10	pA pA nA
Input Resistance	R_{IN}				10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 10kΩ, V_{OUT} = ±10V, T_A = 25°C Over Temperature Range (Note 1)		120 120	150 150		dB dB
Output Voltage Swing	V_{OUT}	CLAMP not connected (note 3)	R_L = 10kΩ R_L = 100kΩ	±12	±14.5 ±14.95		V V
Common-Mode Voltage Range	CMVR			+12, –15	+12.5, –15.1		V
Common-Mode Rejection Ratio	CMRR	CMVR = +12V to –15V Over Temperature Range (Note 1)		120	140		dB
Power Supply Rejection Ratio	PSRR	±3V to ±16.5V Over Temperature Range (Note 1)		120	140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	$e_{N_{p-p}}$	R_S = 100Ω, DC to 1Hz DC to 10 Hz			0.3 1.1		μV_{p-p} μV_{p-p}
Input Noise Current	I_N	f = 10Hz			0.01		pA/$\sqrt{Hz}$
Unity-Gain Bandwidth	GBW				500		kHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ			0.5		V/µs
Rise Time	t_r				0.7		µs
Overshoot					20		%

ELECTRICAL CHARACTERISTICS MAX420, MAX421 (continued)

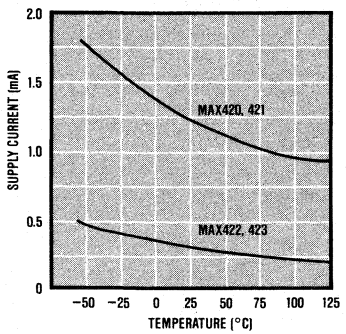
(V^+ = +15V, V^- = -15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Supply Range	V^+, V^-		±2.5		±16.5	V
Supply Current	I_S	No Load, T_A = 25°C Over Temperature Range (Note 1)		1.3	2.0 3.5	mA mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (MAX421)		400		Hz
Clamp ON Current (Note 3)		R_L = 100kΩ	25	100		μA
Clamp OFF Current (Note 3)		-10V ≤ V_{OUT} ≤ +10V		1		pA
Offset Voltage vs Time				100		nV/√month

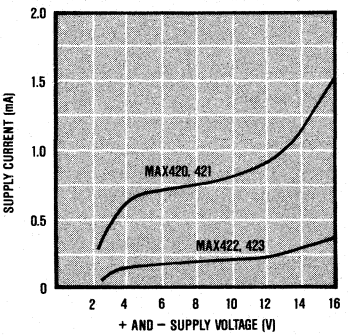
Note 1: Operating temperature range for "C" parts is 0°C to 70°C, for "E" parts is -40°C to 85°C, and for "M" parts is -55°C to 125°C.
Note 2: Guaranteed by design. Sample tested.
Note 3: The OUTPUT CLAMP, pin 9 on MAX421, when connected to the inverting input (pin 4), reduces the overload recovery time inherent with chopper-stabilized amplifiers (see text).
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C, Method 3015.2 Test Circuit)

Typical Operating Characteristics

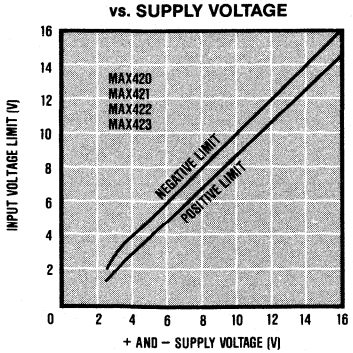
SUPPLY CURRENT vs. TEMPERATURE



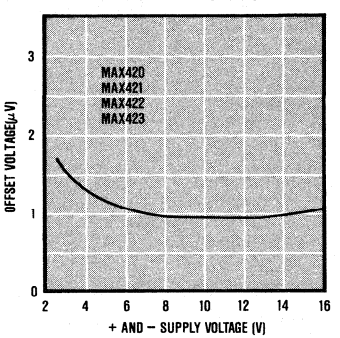
SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



±15 Volt Chopper Stabilized Operational Amplifier

ABSOLUTE MAXIMUM RATINGS: same as for MAX420, 421

ELECTRICAL CHARACTERISTICS MAX422, MAX423

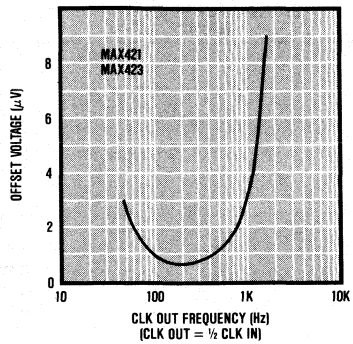
(V^+ = +15V, V^- = -15V, T_A = +25°C. Test circuit unless noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	C E,M		±1 ±1	±10 ±5	µV µV
		Over Temperature Range (Note 1, 2)	C E,M		±2 ±2	±20 ±10	µV µV
Average Temperature Coefficient of Input Offset Voltage	$\frac{\Delta V_{OS}}{\Delta T}$	Over Temperature Range (Note 1, 2)	E,M		0.02	0.05	µV/°C
Input Bias Current (Doubles every 10°C above about 60°C)	I_B	T_A = +25°C	C E,M		10 10	100 30	pA pA
		Over Temperature Range (Note 1)	C E M		30 35 0.5	 5	pA pA nA
Input Offset Current (Doubles every 10°C above about 60°C)	I_{OS}	T_A = +25°C	C E,M		15 15	200 60	pA pA
		Over Temperature Range (Note 1)	C E M		30 50 0.5	 10	pA pA nA
Input Resistance	R_{IN}				10^{12}		Ω
Large Signal Voltage Gain	A_{VOL}	R_L = 100kΩ, V_{OUT} = ±10V, T_A = 25°C Over Temperature Range (Note 1)		120 120	150 150		dB dB
Output Voltage Swing	V_{OUT}	CLAMP not connected (Note 3) R_L = 100kΩ		±14	±14.6		V
Common-Mode Voltage Range	CMVR			+12, -15	+12.5, -15.1		V
Common-Mode Rejection Ratio	CMRR	CMVR = +12V to -15V Over Temperature Range (Note 1)		120	140		dB
Power Supply Rejection Ratio	PSRR	±3V to ±16.5V Over Temperature Range (Note 1)		120	140		dB
Input Noise Voltage (P-P value not exceeded 95% of time)	$e_{N_{p-p}}$	R_S = 100Ω, DC to 1Hz DC to 10 Hz			0.4 1.2		μV_{p-p} μV_{p-p}
Input Noise Current	I_N	f = 10Hz			0.01		$pA/\sqrt{Hz}$
Unity-Gain Bandwidth	GBW				125		kHz
Slew Rate	SR	C_L = 50pF, R_L = 10kΩ			0.125		V/µs
Rise Time	t_r				2.8		µs
Overshoot					20		%
Operating Supply Range	V^+, V^-			±2.5		±16.5	V
Supply Current	I_S	No Load, T_A = 25°C Over Temperature Range (Note 1)			0.3	0.5 1	mA mA
Internal Chopping Frequency	f_{ch}	Pins 12-14 Open (MAX423)			250		Hz
Clamp ON Current (Note 3)		R_L = 100kΩ		5	25		µA
Clamp OFF Current (Note 3)		-10V ≤ V_{OUT} ≤ +10V			1		pA
Offset Voltage vs Time					100		$nV/\sqrt{month}$

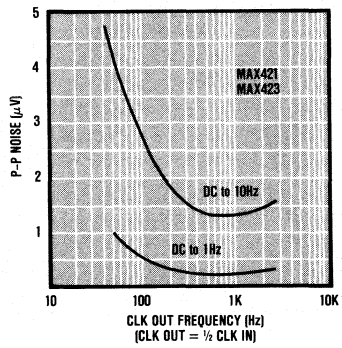
Note 1: Operating temperature range for "C" parts is 0°C to 70°C, for "E" parts is -40°C to 85°C, and for "M" parts is -55°C to 125°C.
Note 2: Guaranteed by design. Sample tested.
Note 3: The OUTPUT CLAMP, pin 9 on MAX423, when connected to the inverting input (pin 4), reduces the overload recovery time inherent with chopper-stabilized amplifiers (see text).
Note 4: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V (Mil Std 883C, Method 3015.2 Test Circuit)

Typical Operating Characteristics

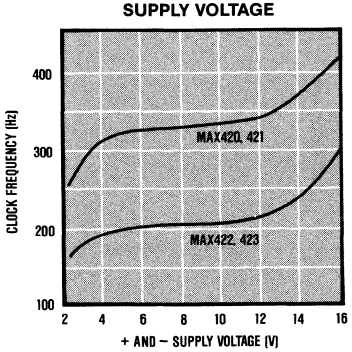
INPUT OFSET VOLTAGE vs. CLOCK FREQUENCY



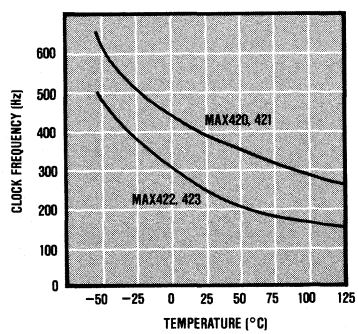
P-P NOISE VOLTAGE vs. CLOCK FREQUENCY



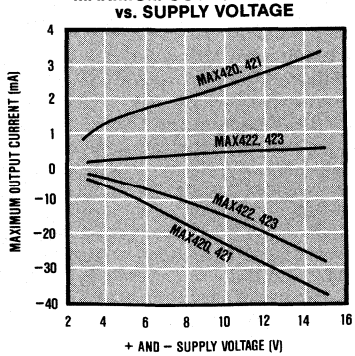
CLOCK FREQUENCY vs. SUPPLY VOLTAGE



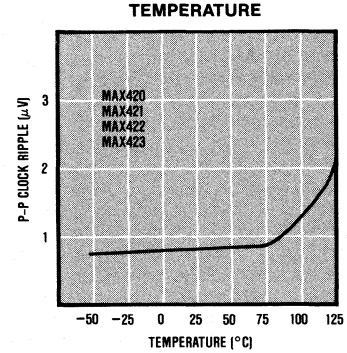
CLOCK FREQUENCY vs. TEMPERATURE



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



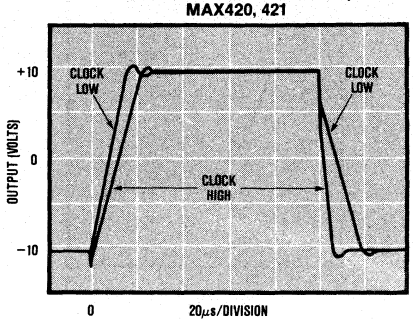
CLOCK RIPPLE REFERRED TO THE INPUT vs. TEMPERATURE



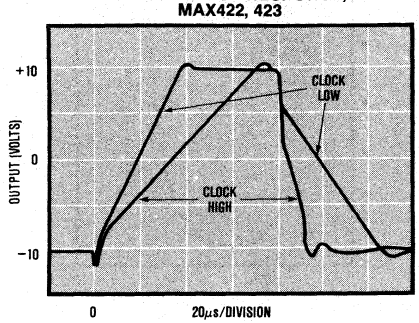
±15 Volt Chopper Stabilized Operational Amplifier

Typical Operating Characteristics

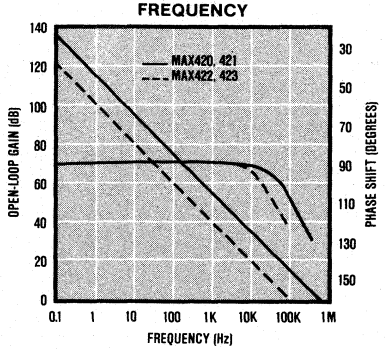
FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX420, 421



FOLLOWER LARGE SIGNAL PULSE RESPONSE, MAX422, 423



OPEN LOOP GAIN AND PHASE SHIFT vs. FREQUENCY



Detailed Description

Amplifier Operation

A block diagram of a MAX420 series amplifier is shown in figure 2. Internally there are two amplifiers, a main amp and a nulling amp. The main amplifier is in the primary signal path and is continuously connected to the external inputs. The null amp alternately corrects its own offset, and then that of the main amp, as its input switches between the two main amp inputs. Offset correction is accomplished by means of compensating FETs in the input stage's bias circuitry (not shown). The offset values that drive these trim FETs are stored for the duration of the correction cycle on two capacitors, C_{EXTA} and C_{EXTB}. Each cycle is controlled by the clock as shown in the timing diagram of Figure 2. An added benefit of the offset correction scheme is that it also increases CMRR, PSRR, and A_{VOL} at low frequencies ($f_{IN} \ll f_{CLK}$).

Capacitor Selection

Two external capacitors, C_{EXTA} and C_{EXTB}, connected as shown in Figure 1, enable the amplifier to store and correct its own offset errors. The MAX420 series is specified with 0.1μF capacitors, however, other values up to 1.0μF may be optimal if different clock rates are used (MAX421, 423 only). If an external clock is used, the capacitor values should be scaled to roughly maintain the ratio between the nominal self-clock period (2.5ms @ 400 Hz) and 0.1μF. For example, if a 200Hz clock were used, then 0.2μF would be best. This relationship is not critical and certainly no change in capacitor value is necessary for part-to-part variations in the internal clock rate.

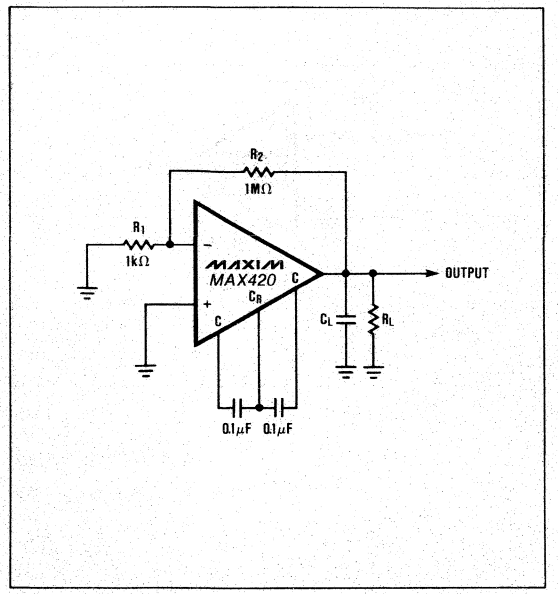


Figure 1. Test Circuit.

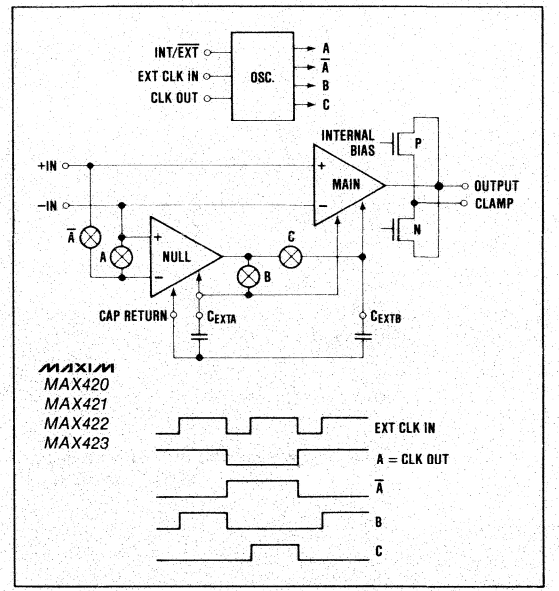


Figure 2. Maxim MAX420 Series Amplifier Block Diagram

The banded or outer foil end of the correction capacitors should be connected to C_{RETN} as this is a low impedance point. C_{EXTA} and C_{EXTB} are high impedance nodes and so the connections to these pins should be as short as possible to minimize noise pick-up.

Capacitor Types

Precision DC performance can be realized with a wide variety of capacitor types, however those with high leakage will cause excessive clock ripple in the signal path and should not be used. Other low cost capacitors, such as ceramics, may have adequate leakage specifications but often also exhibit high dielectric absorption. This will not harm the amplifier's DC performance but can increase the initial settling time on turn-on to 1 or 2 seconds (to 1μV). If fast settling after power-up is required then higher quality capacitors, such as mylar or polypropylene, should be used.

Clock

An on-chip clock is included on all 420 series amplifiers to control the operation of the offset correction circuitry. This oscillator is completely self contained and needs no external components or connections. The internal clock rate is nominaly 400Hz on the MAX420/421 and is 250Hz on the MAX422/423.

External Clock

The MAX421 and 423 have an INT/$\overline{EXT}$ pin for clock selection (pin 14). The pin has an internal pull-up and, for self-clocked operation, can be left open or connected to V^+. When INT/$\overline{EXT}$ is tied to V^- the internal clock is disabled and an external clock can then be applied to EXT CLK IN. Because of an internal divider, the offset nulling circuitry runs at one half the external clock rate.

Duty Cycle and Thresholds

The duty cycle of the external clock is not critical at low frequencies. For EXT CLK IN frequencies of 500Hz or greater, a 50% to 80% positive duty cycle is recommended to allow transients on the null capacitors to settle. This is necessary because the capacitors are only charged when EXT CLK IN is high. The input threshold for EXT CLK IN is typically V^+ - 2.5V so that an external clock signal can swing from either V^+ to GROUND or V^+ to V^-. The internal chopping frequency is available at the CLK OUT pin with either internal or external clock operation .The nominal output levels for CLK OUT are V^+ for a "High" and V^+ - 5V for a clock "Low".

In some instances, it may be advantageous to synchronize two amplifier clocks, or slave one to another. A simple way to accomplish this is to tie the amplifiers' EXT CLK IN pins together (MAX421 or 423 only) and pull one's INT/$\overline{EXT}$ pin low while allowing the other's to float high. The amplifier with INT/$\overline{EXT}$ high will then provide the clock for both devices (see Figure 9).

±15 Volt Chopper Stabilized Operational Amplifier

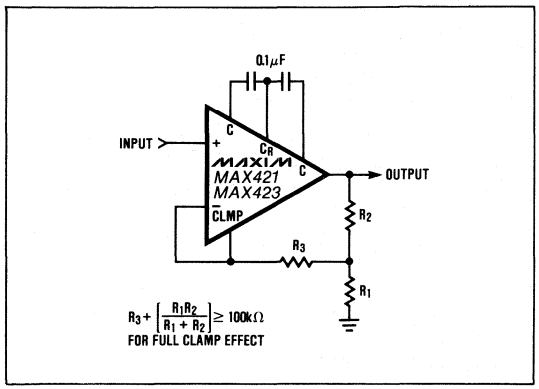


Figure 3. Non-Inverting Amplifier with Optional Clamp

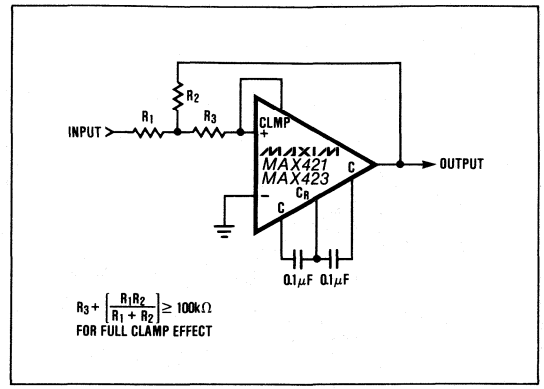


Figure 4. Inverting Amplifier with Optional Clamp

Plugging into a Conventional Op-Amp Socket

As a result of their ±15V supply capability, the 8-pin MAX420 and 422 can plug directly into a conventional op-amp socket for immediate upgrading of DC specifications. Since the external nulling capacitors occupy what are usually "Offset null" pins (1, 5, and 8), the standard op-amp pin-out is still maintained for input, output, and supply connections. Essentially, C_{EXTA} and C_{EXTB} replace the offset trim pot normally required with conventional op-amps.

Output Clamp/Overload

The OUTPUT CLAMP, when connected to the inverting input, reduces the amplifier's overload recovery time (See Figures 3 and 4). It does this by providing a feedback path that is activated just before the output saturates. The resultant reduction in gain prevents differential input overload and consequent charge build-up on the correction capacitors. If the capacitors are allowed to overcharge, the amplifier will need time to recover (typically 500ms) after the overload is removed. Since the OUTPUT CLAMP activates slightly prior to output saturation there is also a small reduction in output swing when it is used. This reduction is typically 500mV with a 10kΩ output load.

Single Supply Operation

The 420 series amplifiers are well suited for operation in single power supply applications that have system ground connected to V^-. With supply voltages of 10 volts or above the input range is typically from Ground to $V^+ - 1.5V$. At lower supply voltages the input-range lower limit will be higher (approx. Gnd + 0.5V at 5V supply). The amplifiers' outputs will swing to within approximately 50mV of Ground or V^+ with a 100kΩ load and within 500mV with 10kΩ (MAX420, 421 only).

Applications

Low Voltage Signals

Realizing microvolt offset and nanovolt drift performance goes beyond the selection of a precision amplifier (though it's not a bad start). When trying to amplify very low level signals and number of outside error sources can confuse the measurement. These errors are often indistinguishable from real signal or amplifier error, which of course is why they are a problem.

Thermo-Electric Effect

This property describes how thermocouples measure temperature. In short it states that two dissimilar metals in contact can be expected to generate a voltage. This is fine for thermocouples but is not so useful when pin-to-socket, socket-to-circuit board, and circuit board-to-edge connector junctions all generate signals which can add to input error. The voltage generated in such situations can range from 0.1 to 10's of μV/°C, many times the offset drift of an MAX420. In general such problems are dealt with by minimizing sockets and connectors in low level circuitry and by using components designed for low thermal EMF when connectors, relays, etc. are unavoidable.

Gradients

The presence of heat in low level circuitry is often not so much a problem as are thermal gradients. Gradients can, for example, cause normally balanced amplifier input connections to be at different temperatures. These connections then generate different thermoelectric voltages that can no longer be completely cancelled by the balanced inputs. The moral then is to minimize thermal gradients by keeping power dissipation and air currents in and around low level circuitry and connections at a minimum.

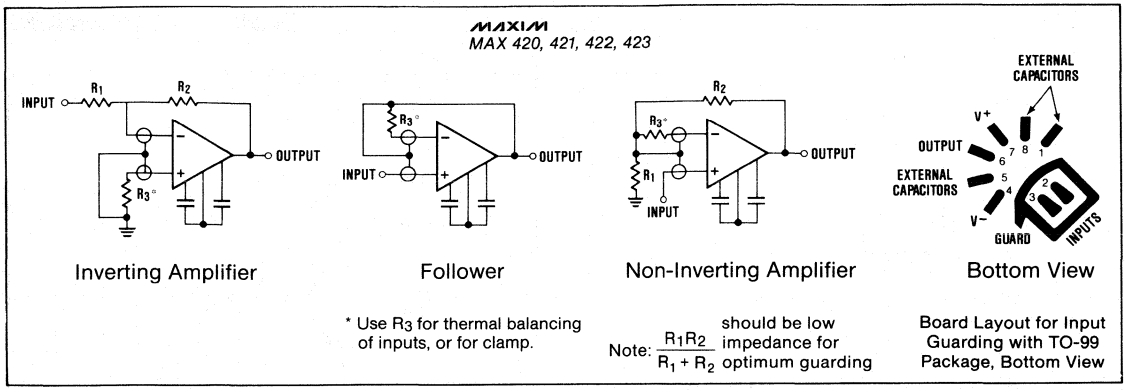


Figure 5. Input Guard Connections.

Thermal Symmetry

Another useful low level technique is to design thermal "symmetry" into the layout. This may mean adding dummy resistors and connections so that the thermal mass, as well as the number of thermoelectric error sources, in an input pair will cancel. It may also involve running input traces near each other and keeping their size the same as well. Thermal "filtering" with small enclosures or even insulation for sensitive areas can also be helpful.

Low Curent Signals, Input Guards

Low leakage, high impedance CMOS inputs allow the MAX420 amplifier family to amplify the signals of very high impedance sources. Though the amplifiers' input bias current is measured in picoamps, getting the surrounding connections to live up to that specification requires some attention. In applications where picoamp or nanoamp errors can be significant, board leakage either from surface contamination or through the board material itself may be a problem.

Controlling Leakage

Using low leakage board materials and proper cleaning methods after assembly can provide marked reductions in leakage induced errors. Beyond this, conformal coatings can be used to control later surface contamination. In some cases, Teflon insulators and/or circuit board guard rings may be necessary to protect very high impedance nodes. Guard connections for various amplifier configurations are shown in Figure 5. In each case the guard is connected to a low impedance point that is approximately at the same potential as the inputs. Leakage currents from other points on the board are then absorbed by the guard. For best results, guard rings should be used on both sides of the circuit board. The 14 pin MAX421 and 423 have specifically been designed to ease input guard layout in that the pins adjacent to the inputs are unused in those packages.

Output Characteristics /Open Loop Gain

The MAX420 and 421 can typically drive a 10kΩ load from +14.8V to -14.5V when operating with ±15V power supplies. With a 100kΩ or greater load, however, the output can typically swing to within 50mV of each rail. The output swing with the lower power MAX422 and 423 will be somewhat less for a given load.

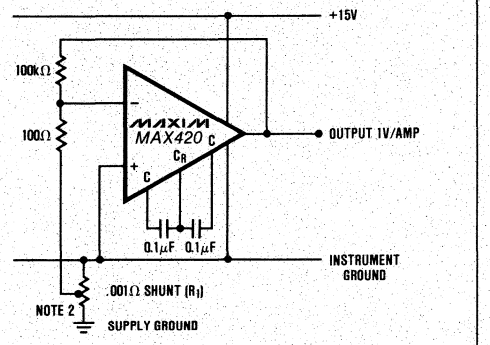
The open loop gain of a MAX420 series amplifier is somewhat load dependent for resistances which are less than 10kΩ. The effect is largely due to the impedance of the amplifier's output stage. The gain is about 17dB lower with a 1kΩ load than it is with 10kΩ. Since even with 1kΩ the gain is still typically 120dB, the reduction is insignificant for low frequency applications. In wideband circuits, however, the best results are achieved with loads of 10kΩ or more where the amplifier's open loop response is a smooth 6dB/octave slope from 0.1Hz to 0.5MHz. Additionally, there is negligible phase shift at the frequency where the null amp is rolled off.

Intermodulation

In some chopper-stabilized amplifier designs, interaction between the input signal and the chopper frequency sometimes produces intermodulation products in the form of sum and difference signals. If the input frequency and the chop rate are near enough to each other, a difference signal may even appear as a DC error at the output. The MAX420 series minimizes these problems with active compensation circuitry that virtually eliminates intermodulation effects and controls the amplifier's open loop gain-phase characteristics as well. With well behaved open loop parameters, the chopper circuitry's impact on the amplifier's dynamic performance can be ignored in most applications.

±15 Volt Chopper Stabilized Operational Amplifier

Typical Applications



Note 1: $R_1 \simeq$ 3 cm. #20 solid copper wire.
Note 2: Shunt contact point determined at calibration.

Figure 6. Ultra-low Current Shunt Amp.

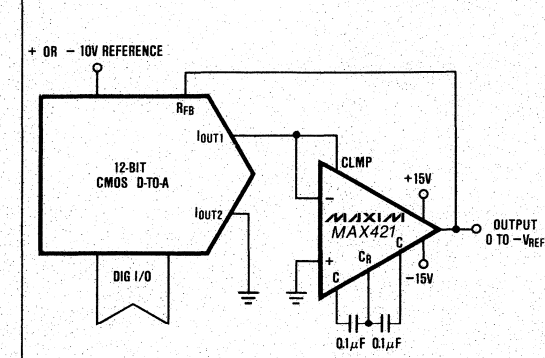
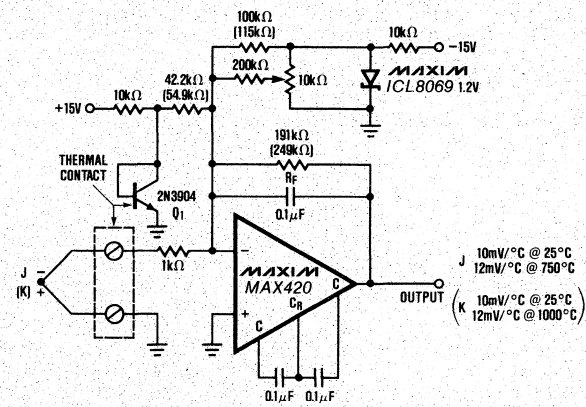


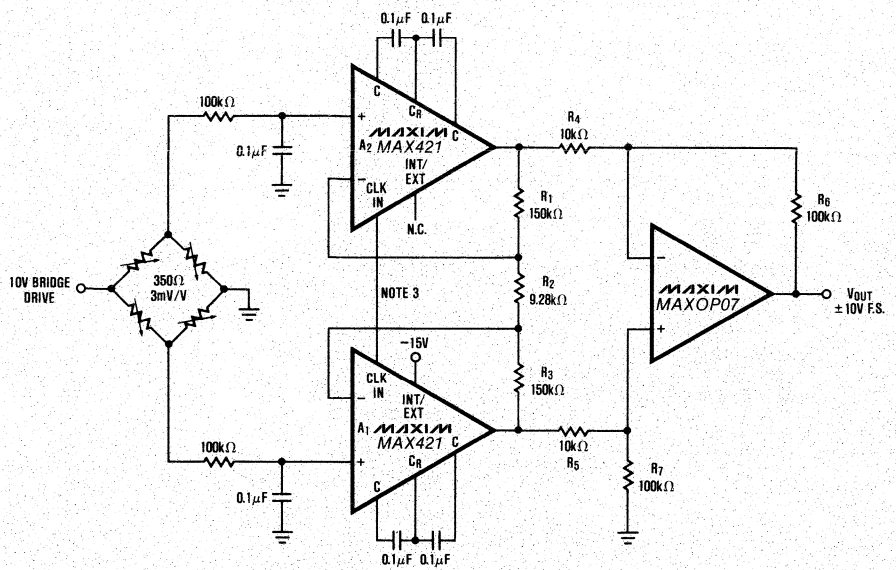
Figure 7. CMOS DAC Output Amplifier. Low offset maintains DAC linearity.



Note 1: Q_1 and connection terminals must be at the same temperature.
Note 2: Values in parentheses are for type K thermocouple.
Note 3: Conections to inverting input of op-amp should be kept as short as possible to reduce noise pickup.
Note 4: All circuit power is ±15V.

Figure 8. Amplifier with Cold-Junction Compensation for Grounded Thermocouples.

Typical Applications



Note 1: Matching rules: $R_1 = R_3$ and $\frac{R_6}{R_7} = \frac{R_4}{R_5}$. Matching determines CMRR, for example 0.1% = 60dB, 0.01% = 80dB.
Note 2: Metal film or wire-wound resistors are recommended.
Note 3: A_1's internal clock is slaved to A_2 via CLK IN pins.
Note 4: All amplifiers powered from ±15V supplies
Note 5: R_2 is a selected value.

Figure 9. 10μV V_{OS}, 0.1μV/°C Strain Gauge Instrumentation Amplifier

Chip Topography

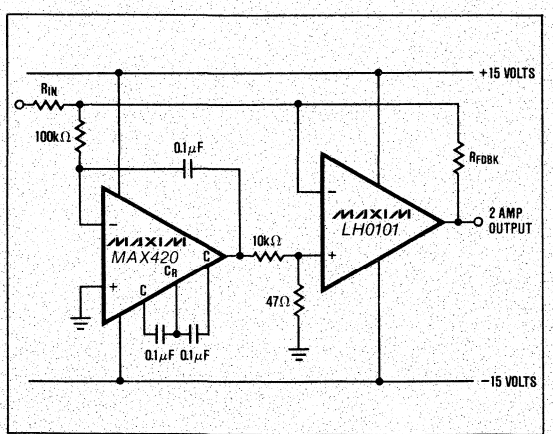
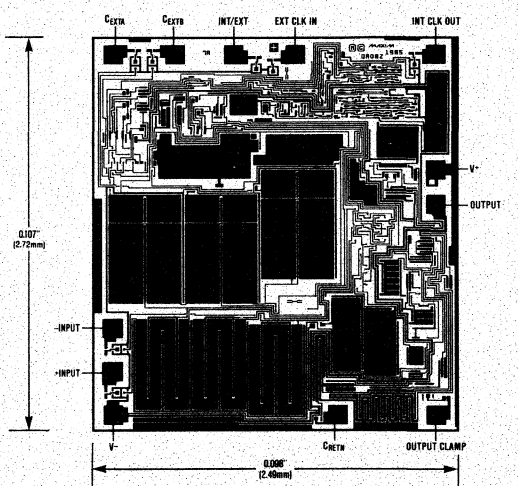


Figure 10. D.C. Stabilized Power Op-Amp. Main amp has 5MHz unity-gain point.

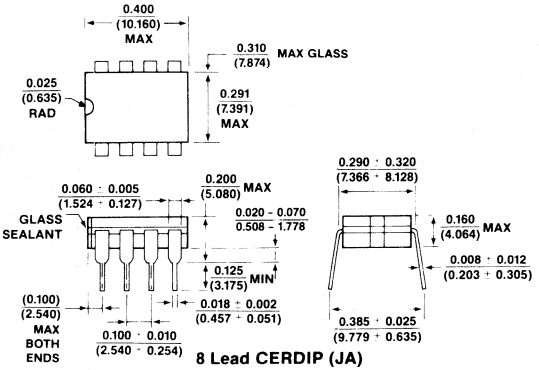


±15 Volt Chopper Stabilized Operational Amplifier

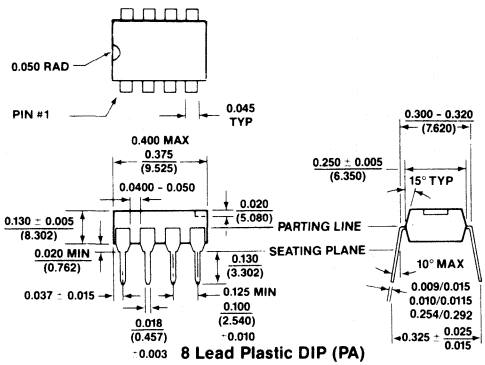
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE
MAX422CPA	0°C to +70°C	8 Lead Plastic DIP
MAX422EPA	-40°C to +85°C	8 Lead Plastic DIP
MAX422MTV	-55°C to +125°C	TO-99 Can
MAX423CPD	0°C to +70°C	14 Lead Plastic DIP
MAX423C/D	0°C to +70°C	Dice
MAX423EPD	-40°C to +85°C	14 Lead Plastic DIP
MAX423MJD	-55°C to +125°C	14 Lead CERDIP
MAX423M/D	-55°C to +125°C	Dice

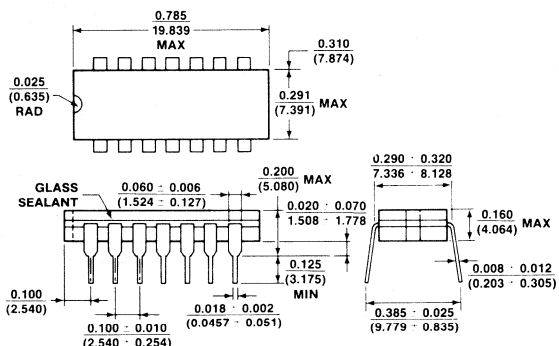
Package Information



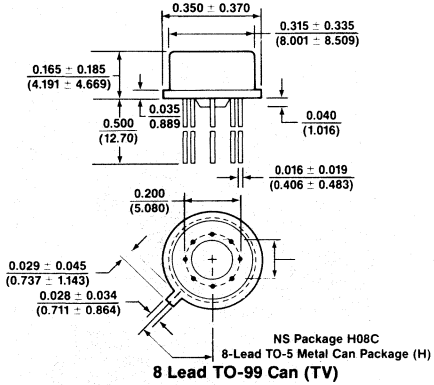
8 Lead CERDIP (JA)
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



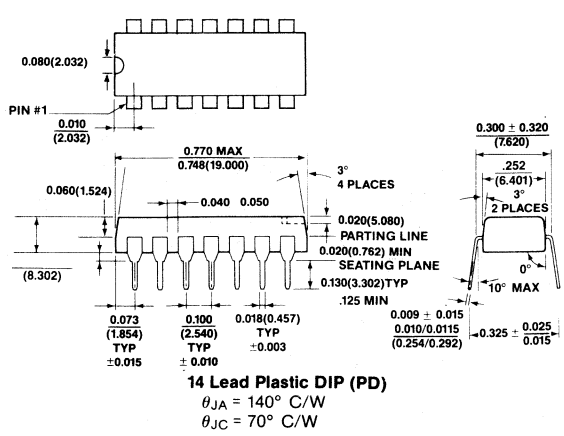
8 Lead Plastic DIP (PA)
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



14 Lead CERDIP (JD)
θ_{JA} = 105° C/W
θ_{JC} = 50° C/W



8 Lead TO-99 Can (TV)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W



14 Lead Plastic DIP (PD)
θ_{JA} = 140° C/W
θ_{JC} = 70° C/W

INTRODUCTORY

SPECIFICATIONS BASED ON EVALUATION OF LIMITED NUMBER OF DEVICES

MAXIM

AC To DC Regulator (110/220 VAC To 5.0V DC)

General Description

The MAX610 family of AC to DC Power Converters minimizes the cost, simplifies the design, and reduces the component count, size, and weight of 1/2 watt power supplies. With an 8 VRMS input voltage the MAX610 needs only a single filter capacitor to make a complete 5V, 100mA power supply. With the addition of a current limiting resistor and a current limiting capacitor, the MAX610 connects directly to the 110VAC or 220VAC power line to make a minimum component count 110/220VAC to 5VDC power supply.

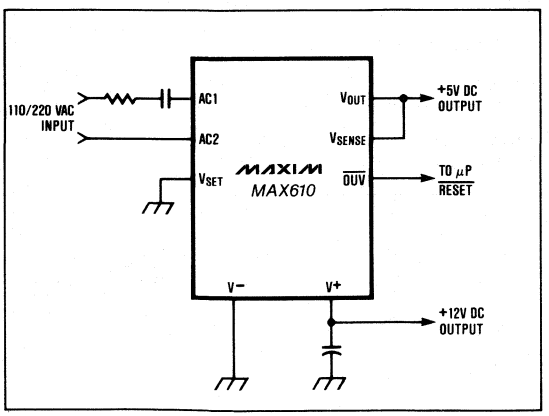
The three members of the MAX610 family differ in three respects: full or half wave rectification, 12V or 18V zener voltage, and the assignment of pin 4 to the function of setting the output voltage or setting the time delay. The MAX610 has a full wave rectifier, a 12V zener, and the output voltage is either the internally preset +5V or user adjustable from 1.3 to 9V. The MAX611 has a half wave rectifier, a 12V zener, a fixed 5V output, and pin 4 controls the time delay of the reset output. The MAX612 has a full wave rectifier, an 18V zener, and the output voltage is either the internally preset +5V or user adjustable in the range of +1.3V to +15V.

Applications

The MAX610 family is ideal for applications where size, weight, component count, and cost of 1/2 watt power supplies must be reduced. The reliable powerup reset and over/undervoltage detection makes the MAX610 family well suited for microprocessor based controllers.

Minimum Component Count Power Supplies
Uninterruptable 5V Power Supplies
Precision Battery Chargers
Line Powered Appliances
Industrial Controls
Off Line Instruments
Triac Output Power Controllers

Typical Operating Circuit



Features

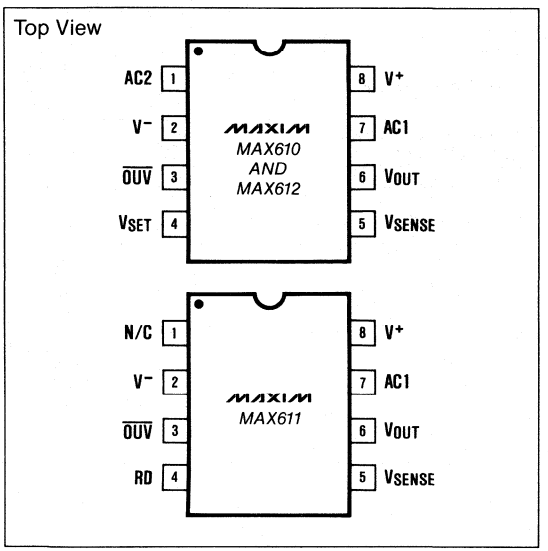
- Direct 110/220VAC to 5V DC Conversion
- Minimum External Component Count
- Output Voltage Preset to 5V ±4%
- 70μA Typical Quiescent Current
- Over/Undervoltage Detection
- Power-up Reset Circuit with Programmable Delay
- Programmable Current Limiting
- Programmable Output Voltage: 1.3V to 15V.

Ordering Information

PART	TEMP. RANGE	PACKAGE
MAX610CP	0°C to +70°C	8 Lead Plastic DIP
MAX611CP	0°C to +70°C	8 Lead Plastic DIP
MAX612CP	0°C to +70°C	8 Lead Plastic DIP

Pin Configurations

Top View



6

AC To DC Regulator (110/220 VAC To 5.0V DC)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range ..... 0°C to +70°C
Maximum Junction Temperature ..... +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Power Dissipation @ 25°C 750mW
derate 8mW/C above 25°C.
Input Current
MAX611
AC1, V⁻; 250μs non-repetitive pulse 5A
AC1, V⁻; continuous ..... 180mA RMS
V⁺ 150mA
MAX610, MAX612
AC1, AC2; 250μs non-repetitive pulse 5A
AC1, AC2; continuous ..... 120mA RMS
V⁺ 150mA
All other terminals 10mA

Input Voltage
MAX610, MAX 611 (Note 1)
AC1, AC2 ..... 11.5V
V⁺ 10.8V
MAX612
AC1, AC2 ..... 17V
V⁺ 16.2V
$\overline{OUV}$ ..... (V⁻ - 0.3) to +16V
All other terminals ..... (V⁻ - 0.3V) to (V⁺ + 0.3V)
Output Current
V⁺, V_{OUT} 150mA
$\overline{OUV}$ 10mA

Note 1: The maximum input voltage may be exceeded if the maximum input current and power dissipation specifications are observed.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is no implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V^+ = 10V, R_{SENSE} = 0Ω, V_{SET} connected to V^- unless noted)

INPUT RECTIFIER AND ZENER

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_F	I_F = 1mA I_F = 50mA		0.62 1.1	 2.0	V V
Zener Voltage	V_Z	I_Z = 50mA, Measure at V^+ MAX610, MAX611, MAX612		 12.4 18.6		 V V
Zener Dynamic Resistance	R_Z	I_Z = 50mA MAX610, MAX611, MAX612		 6 9		 Ω Ω

SERIES VOLTAGE REGULATOR

Preset Output Voltage	V_{OUT}	0.5mA ≤ I_{OUT} ≤ 50mA T_A = 25°C 0°C ≤ T_A ≤ +70°C	4.80 4.75	5.00 5.00	5.20 5.25	V V
Temperature Coefficient of Output Voltage	$\frac{\Delta V_{OUT}}{\Delta T}$	0°C ≤ T_A ≤ +70°C		±100		ppm/°C
Internal Voltage Reference	V_{SET}	MAX610, MAX612, Figure 8		1.3		V
Line Regulation (DC Input)	$\frac{\Delta V_{OUT}}{\Delta V^+}$	8V ≤ V^+ ≤ V_Z, Figure 7		0.25		%/V
Line Regulation (AC Input)	$\frac{\Delta V_{OUT}}{\Delta V_{AC}}$	I_{OUT} = 10mA $70V_{RMS}$ < V_{IN} < $140V_{RMS}$ or $140V_{RMS}$ < V_{IN} < $280V_{RMS}$ Figure 3, 4		 0.001 0.001		 %/V %/V
Output Impedance	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	I_{OUT} changing from 1mA to 51mA		0.6	2.0	Ω
Input-Output Voltage Differential	$V^+ - V_{OUT}$	I_{OUT} = 25mA		1.1	2.0	V
V_{SET} Input Current	I_{SET}			0.01	100	nA
Supply Current	I^+			70	150	μA

ELECTRICAL CHARACTERISTICS (Continued)

(T_A = 25°C, V^+ = 10V, R_{SENSE} = 0Ω, V_{SET} connected to V^- unless noted)

OVER VOLTAGE DETECTOR

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detection Voltage	V_{OUVH}	Measured at V_{SENSE}		5.4	5.65	V
Undervoltage Detection Voltage	V_{OUVL}	Measured at V_{SENSE}	4.35	4.65		V
$\overline{OUV}$ Output Leakage	I_{OUV}	V_{SENSE} = 5V, $\overline{OUV}$ = 5V		0.001	10	μA
$\overline{OUV}$ Output Voltage	V_{OUV}	$V_{SENSE} \geq$ 5.65V or $V_{SENSE} \leq$ 4.35V, I_{OUV} = 1mA			0.4	V
Reset Time Delay	t_{DELAY}	Figure 10A, C3 = 0.01μF		30		ms
Reset Pin Threshold	V_{TH}	MAX611 only $V^+ = V_Z$		8.0		V

Pin Descriptions

PIN	PIN #	DESCRIPTION
AC1	7	AC input to the internal diode rectifier.
AC2	1 (MAX610/12)	Second AC input to the full wave bridge rectifier.
N/C	1 (MAX611)	This pin is not connected on the MAX611.
V^-	2	Negative output terminal. This terminal is also an AC input for the half wave rectifier of MAX611.
V_{OUT}	6	Positive regulated DC output.
V_{SENSE}	5	Current limit input. The output short circuit current limit is 0.6V/R_{SENSE}, where R_{SENSE} is a current sensing resistor connected between V_{OUT} and V_{SENSE}.
$\overline{OUV}$	3	This open drain pin goes low during undervoltage and overvoltage conditions. The undervoltage and overvoltage thresholds are fixed at 4.65V (undervoltage) and 5.4V (overvoltage) and do not change, even if the output voltage is changed via the V_{SET} terminal.

PIN	PIN #	DESCRIPTION
V^+	8	Positive unregulated or raw DC output of the rectifier. The raw DC filter capacitor connects to this terminal.
RD	4 (MAX611)	An external capacitor connected to the Reset Delay pin determines the Reset Delay period. The reset time delay is directly proportional to the capacitance connected to this pin; each 0.01μF of capacitance results in 30 milliseconds of delay. This delay period must elapse before the Reset/$\overline{OUV}$ pin goes high after an overvoltage or undervoltage condition — see Figure 10.
V_{SET}	4 (MAX610/12)	If the V_{SET} terminal is grounded, the MAX610 and MAX612 output voltage will be the preset 5V ±4%. Alternatively, the V_{SET} input can be used to set the output voltage to any voltage from 1.3V to 15V (MAX612) or 1.3V to 10V (MAX610 and MAX611), using a simple resistive voltage divider — see Figure 8.

Block Diagrams

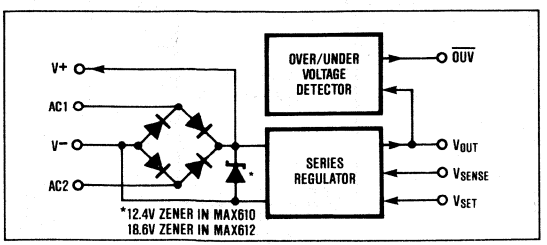


Figure 1. Block Diagram MAX610 and MAX612.

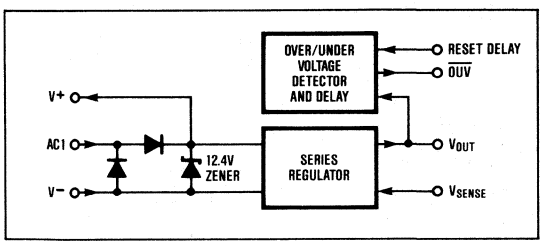


Figure 2. Block Diagram MAX611.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Typical Applications

Simple Line-Powered 5V Supply

Figure 3 shows a 50mA, 5V power supply using the full wave MAX610. Typical component values for both 110VAC and 220VAC 50/60Hz operation are shown. The output of this power supply is **NOT ISOLATED** from the power line: **the MAX610 and any equipment powered by the MAX610 must be enclosed to avoid shock hazards.** To avoid a second potential shock hazard, include the optional 1MΩ resistor shown in dotted lines. This resistor will discharge the voltage left on C1 when the 110/220VAC is disconnected.

110/220VAC to 5V, Half Wave Rectification

Figure 4 shows a 50mA 5V power supply using the half wave MAX611. The circuit differs from Figure 3 in that the 5V output is referenced to one side of the 110VAC power line. This circuit is generally preferred for systems that control triacs, where it is desired to have V^- connected to the power line. Note that for a given amount of output current, the value of C1 must be twice the value used in the full wave circuit of Figure 3. As with all MAX610 family circuits that do not use a transformer to isolate the circuit, this circuit is **NOT ISOLATED** from the power line.

Minimum Component Count 5V, 10mA Power Supply

For output currents of less than 10mA capacitor C1 of Figure 3 can be omitted, resulting in the circuit shown in Figure 5. The available output current is determined by the value of R1. For example, with R1 = 8.2kΩ, the available output current is 10mA, while the power dissipation in R1 is 1.3W. Double both the resistance value and the wattage rating of R1 for use with 220VAC input.

Transformer Isolated 5V Power Supply

If isolation from the power line is required, use the MAX612 in the circuit of Figure 6. The MAX612 must have an input voltage of at least 8V peak to maintain a regulated 5V output, but the peak transformer output voltage must not exceed 17V unless the current is limited as shown in Figures 3 and 4. The AC input line voltage can range from 80VRMS to 160VRMS with the 8VRMS nominal transformer voltage shown.

The MAX612 power dissipation is approximately $(V_{IN(peak)} - V_{OUT}) \times I_{LOAD}$. With the 8VRMS transformer shown, the power dissipated in the MAX612 limits the maximum output current to 100mA at 25°C ambient and 30mA at 70°C. If the 8V transformer is replaced by a 6.3V transformer, the maximum output current increases to 150mA at 25°C, but the minimum input line voltage to maintain output voltage regulation is increased to 100VRMS. When using a 6.3VRMS transformer, the filter capacitor connected to V^+ must be increased to 2200μF to ensure that the minimum voltage at V^+ is greater than 6V throughout each line cycle.

Resistor R1 limits the peak input current, but is not needed if the transformer impedance limits the peak current to a suitable value. As a rule of thumb, R1 can be omitted if the short circuit output current of the transformer is less than 2 Amps.

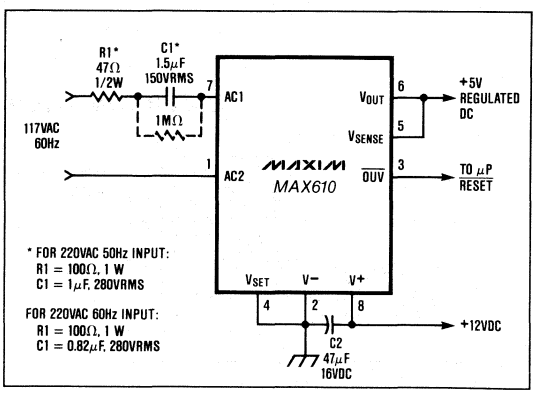


Figure 3. Simple Line-Powered 5V Supply (also used for Typical Operating Circuit).

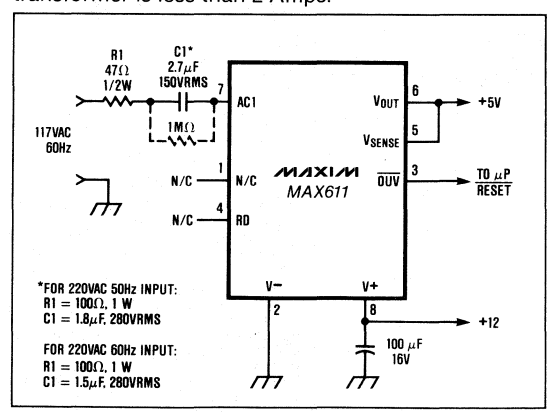


Figure 4. 110/220 VAC to 5V, Half Wave Rectification.

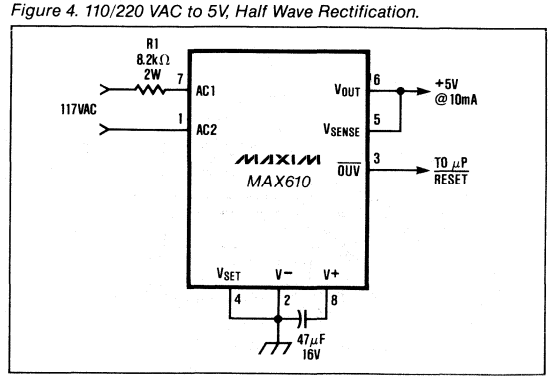


Figure 5. Minimum Component Count 5V, 10mA Supply.

AC To DC Regulator (110/220 VAC To 5.0V DC)

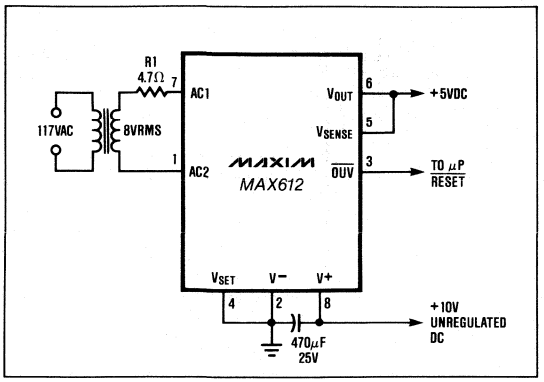


Figure 6. Transformer Isolated 5V Power Supply.

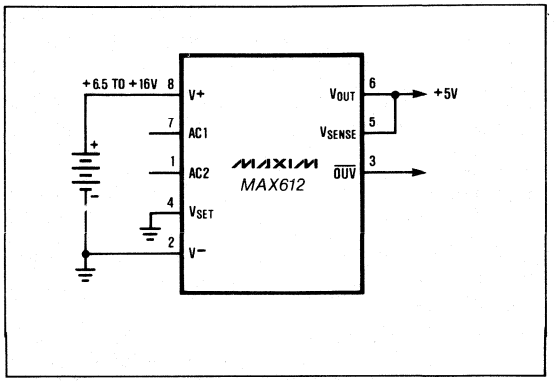


Figure 7. DC Input 5V Output Power Supply.

DC Input 5V Power Supply

The MAX610 family can also be powered by a DC input at the V^+ pin, as shown in Figure 7. The MAX610/11/12 typically use only 70μA of quiescent current, and can supply up to 150mA at 5V. The power dissipation in this mode of operation is simply calculated as

$$Pd = (V_{IN} - V_{OUT}) \times I_{OUT}.$$

The MAX610 family has a very low minimum $V_{IN} - V_{OUT}$ or dropout voltage; they need only 6.5V input to deliver 150mA at 5V.

The MAX612 can be used with input voltages up to 16V. The MAX610 and MAX611 are suitable for use with input voltages up to 10V.

Adjustable Output Voltage

The MAX611 output voltage is fixed at 5V ± 4%. The MAX610 and MAX612 output voltages can be set to 5V ± 4% by simply connecting the V_{SET} terminal to V^-; other output voltages can be selected by connecting an external resistive voltage divider between the output and V_{SET} as shown in Figure 8. Calculate the resistor values for other voltages using the formula

$$V_{OUT} = 1.3V \times \left(1 + \frac{R2}{R3}\right).$$

The maximum input voltage to the MAX612 is limited to 16V, enabling the MAX612 to supply any voltage from 1.3V to 15V. The maximum input voltage to the MAX610 is 10V, and the MAX610 can supply any output voltage from 1.3V to 9V.

The output voltage of the standard MAX610 is set to 5V ± 4% with an undervoltage trip point of 4.65V and an overvoltage trip point of 5.4V. Other output voltages are available through fusible link programming. The

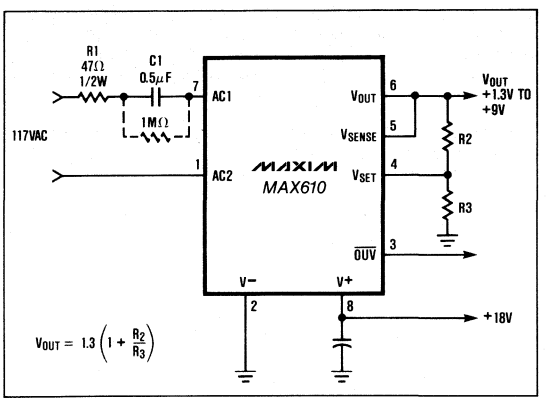


Figure 8. Adjustable Output Voltage.

overvoltage and undervoltage trip points are fixed at 107% and 93% of the pretrimmed output voltage. Consult factory regarding availability and minimum order requirements for preset voltages other than 5V.

Output Circuit Current Limiting

Figure 9 shows how a resistor, R_{SENSE}, can be added to any of the above circuits to provide short circuit current limit protection. A voltage difference between V_{SENSE} and V_{OUT} greater than a base-emitter voltage (approximately 0.6V) activates the MAX610/11/12 output current limit protection circuitry.

$$I_{CURRENT\ LIMIT} = \frac{0.6V}{R_{SENSE}}$$

When current limiting occurs, the voltage at V_{SENSE} will fall below 4.65V, causing the $\overline{OUV}$ output to go low.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Powerup Reset Delay

The MAX611 differs from the MAX610/12 in that MAX611 pin 4 controls a reset delay period, whereas the MAX610/12 pin 4 is used to adjust the output voltage. Both the MAX610/12 $\overline{OUV}$ pin and the MAX611 $\overline{OUV}$ pin go low immediately the output voltage goes below the undervoltage or above the overvoltage threshold. The MAX610/12 $\overline{OUV}$ pin will go high immediately the output returns to 5V. The MAX611 $\overline{OUV}$ pin will go high only after the output has been at 5V for a delay period determined by the value of a capacitor connected between V^- and pin 4 of the MAX611. This makes the $\overline{OUV}$ output well suited for driving the reset input of microprocessors.

Upon power-up the MAX611 $\overline{OUV}$ output will stay low until the output has been at 5V for the length of the delay period. This provides a reliable power-up reset to the microprocessor. Whenever the MAX611 output falls below 4.65V (as during a brownout), the $\overline{OUV}$ pin will go low, resetting the microprocessor. The output voltage must remain above 4.65V for the entire delay period before the $\overline{OUV}$ pin will go high: each time the voltage falls below 4.65V the reset delay period is restarted.

The delay period is approximately 30 milliseconds for each 0.01μF of capacitance. Leave pin 4 floating if this additional delay is not desired.

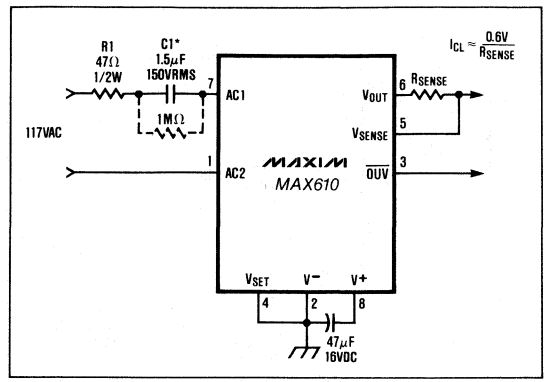


Figure 9. Short Circuit Current Limiting.

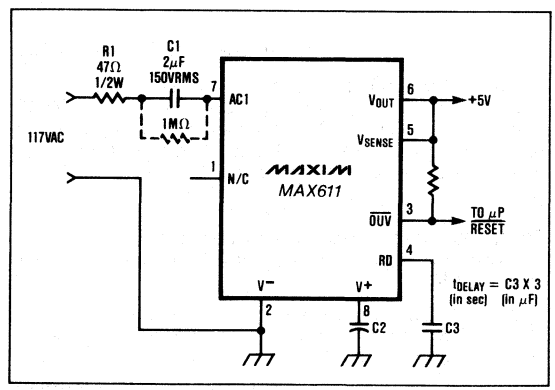


Figure 10A. Power-Up Reset Delay.

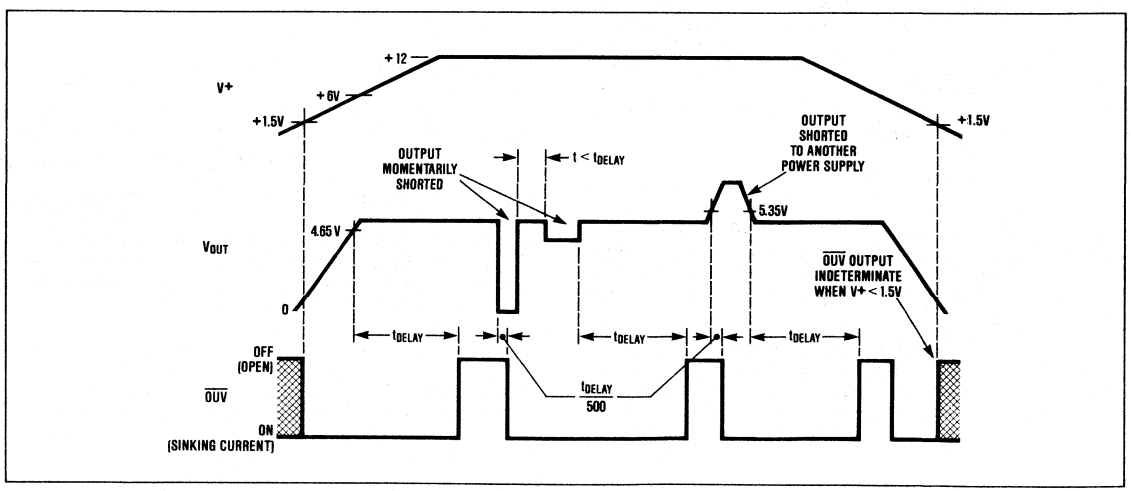


Figure 10B. Power-Up Reset Delay.

AC To DC Regulator (110/220 VAC To 5.0VDC)

+12V Output for Driving Triacs, Relays and MOSFETs

In some circuits a voltage higher than 5V is needed to drive relays, triacs, or power MOSFET gates. The DC output voltage at V^+ is +12V (+18V for MAX612) and can be used to trigger triacs as shown in Figure 11. The V^+ voltage is equal to the MAX610/11 zener voltage until the load current (total current drawn from the +12V and the +5V) approaches the maximum available output current (40mA for each μF of C1 capacitance with 110VAC 60Hz input, 70mA/μF with 220VAC 50Hz input). The ripple on the +12V is relatively low. With the components shown in Figure 11 the ripple voltage is about 5mV peak-peak at 10mA load current and 20mV at 40mA load current.

Increasing Output Current

The maximum allowable value for C1, and therefore the output current available from the MAX610 family, is limited by the power dissipated in the internal zener under no load conditions. By dissipating some of this power in an external zener, the output current capability can be increased.

The MAX611 can deliver up to 150mA at 5V when an external 7.5V zener is connected as shown in Figure 12. Note that capacitor C1 has been increased to 10μF, and that the 7.5V zener must be capable of dissipating approximately 2 watts under no load conditions.

Figure 13, the equivalent circuit using the MAX610, can supply 120mA at 5V. Since the MAX610 has a full wave rectifier, the value of C1 need only be half the value needed in the half wave circuit of Figure 12. The zeners each dissipate approximately 1 watt under no load conditions, with the zener power dissipation decreasing with increased output load current.

The method of increasing the available output current of the MAX610 shown in Figure 14 uses only one zener. The power dissipation of the MAX610 is slightly higher in this circuit than in that of Figure 13, since the zener current passes through the bridge rectifier of the MAX610. The values shown are suitable for up to 100mA output current.

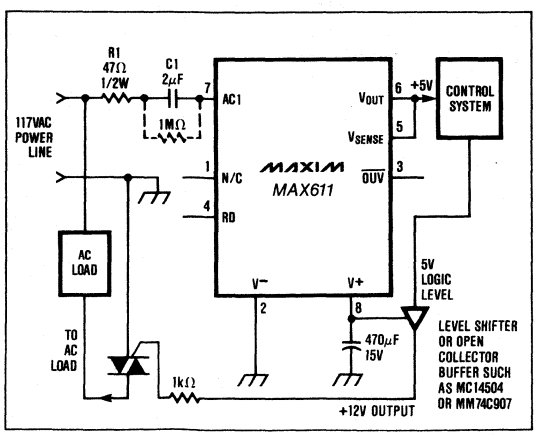


Figure 11. Driving Triacs With +12V Supply.

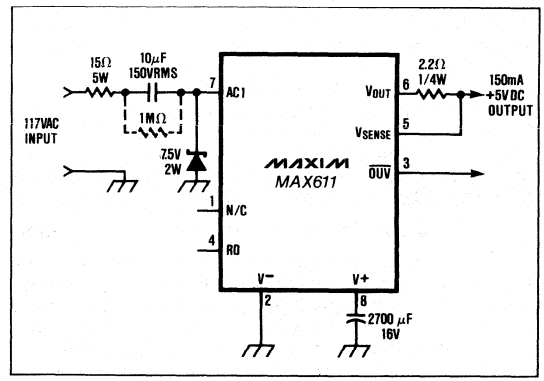


Figure 12. Increasing Maximum Allowable MAX611 Output Current.

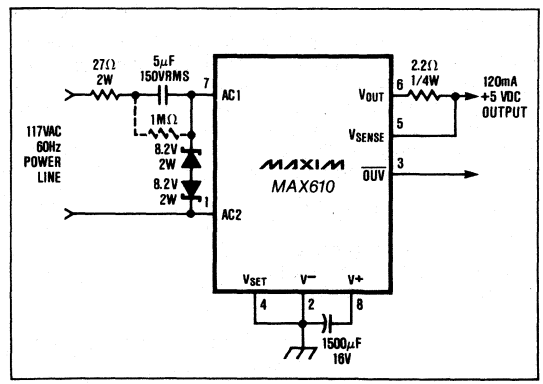


Figure 13. Increasing MAX610 Output Current.

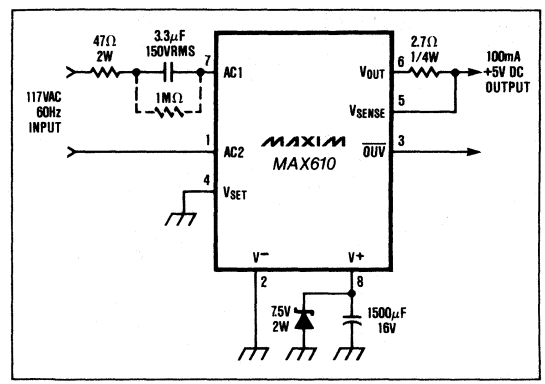


Figure 14. Increasing MAX610 Output Current, Alternative Method.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Uninterruptable 5V Power Supply

Figure 15 shows a simple way to combine a MAX610 with a battery to form an uninterruptable 5V power supply. When the 110VAC line voltage is present resistor R2 trickle charges the 7.2V NiCad battery. When the 110VAC is removed the NiCad battery will supply current through diode D1, and the MAX610 output will remain a constant 5V. The MAX610 will continue to deliver 5V out until V^+ is approximately 5.8V and the battery voltage is approximately 6.5V. Alkaline 9V or NiCad 8.4V batteries are also suitable; R2 should not be used with the non-rechargeable 9V alkaline battery. If isolation from the power line is required, drive AC1 and AC2 with a transformer as shown in Figure 6.

Polarity Insensitive Battery Powered Supply

Figure 16 shows a +5V power supply which will work even if the battery is installed backwards: the full wave bridge rectifier of the MAX612 will correct the battery polarity. The MAX612 is well suited for battery powered circuits since its quiescent current is only 70μA. The MAX610 can also be used if the battery voltage is less than 10V.

Battery Charger

The +6.7V open circuit or float voltage of Figure 17 is set by R2 and R3; the maximum charging current of 60mA is set by the value of C1. Since, unlike transformer driven battery chargers, C1 conducts current throughout most of each line cycle, the ratio of the RMS charging current to the average charging current is only about 1.2:1, and capacitor C2 is optional.

$I_{AVG(MAX)} = V_{IN} \times 5.56\ F_{IN} \times C$ (maximum charging current)

F_{IN} = Input Frequency
$I_{RMS} = 1.2\ I_{AVG}$; without C2
$I_{RMS} = I_{AVG}$; with C2.

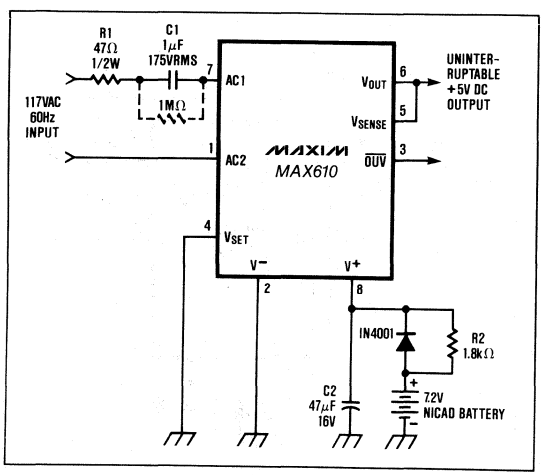


Figure 15. Uninterruptable 5V Power Supply.

The half wave MAX611 can also be used in this circuit, but the value of C1 must be doubled and the ratio of RMS current to average current increases to about 1.7:1.

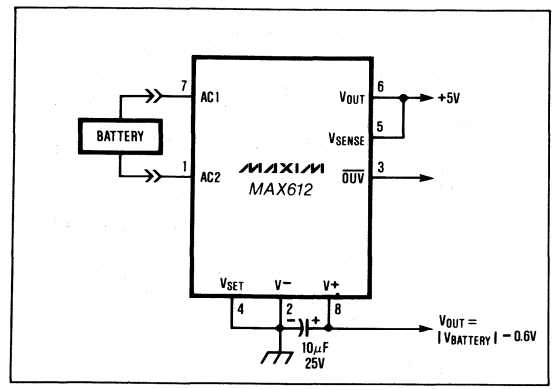


Figure 16. Polarity Insensitive Battery-Powered Supply.

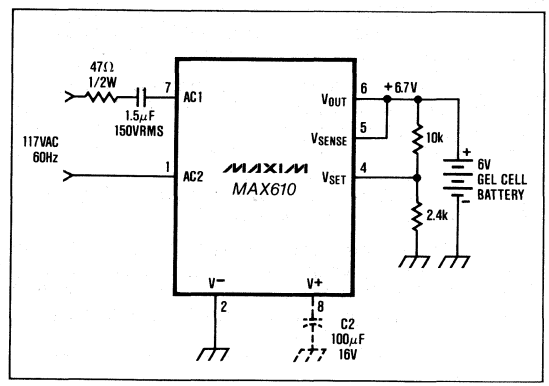


Figure 17. Simple Battery Charger.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Component Selection

The component values shown in the Typical Applications above are suitable for most applications. This section gives the reasons for the particular component values chosen, explains the effect of using other values, and discusses the component specifications.

Current Limiting Capacitor, C1

This capacitor is the most critical component for a 110/220VAC input power supply based on the MAX610 family. It must continuously withstand the full line voltage so it should be rated for AC operation. A conservative designer will use a capacitor rated for at least 150VRMS working voltage for 110VAC circuits, and at least 280VRMS for 220VAC or 240VAC circuits. This capacitor must be a NON-POLARIZED capacitor such as polyester (Mylar™) or polypropylene metallized film. Metallized film capacitors are preferred over metal foil capacitors since metal foil capacitors are more likely to fail as a short circuit than are metallized film capacitors.

The value of C1 determines both the power dissipation of the MAX610/11/12 and the maximum available output current. The value of C1 should be the smallest value that will deliver the desired output current at minimum line voltage, since the power dissipated by the MAX610/11/12 increases with increasing values of C1. Table 1 gives the formula for calculating C1 as a function of the desired output current. Table 2 shows some typical component suppliers and part numbers.

Current Limiting Resistor, R1

R1 limits the maximum peak current that occurs when power is first applied to the MAX610 just as the power line voltage is at its maximum. The instantaneous peak current must be limited to 5 Amps. For 110VAC input voltage R1 must be 33Ω or greater; for 220VAC input voltage R1 must be 68Ω or greater. The recommended values are 47Ω for 110VAC and 100Ω for 220VAC. The power dissipation in R1 is constant, independent of the load current.

With 110VAC 60Hz input

$$\underset{\text{(in mW)}}{Pd(R1)} = 1.6 \times \underset{\text{(in } \mu F)}{C1} \times \underset{\text{(in } \Omega)}{R1}$$

With 220VAC 50Hz input

$$\underset{\text{(in mW)}}{Pd(R1)} = 2.7 \times \underset{\text{(in } \mu F)}{C1} \times \underset{\text{(in } \Omega)}{R1}$$

Raw DC Filter Capacitor, C2

This capacitor is normally an aluminum or tantalum electrolytic capacitor. C2 is ordinarily 47μF when the MAX610/12 are driven from the 110/220VAC power line. The half wave MAX611 requires larger values for C2 since the output current is supplied by C2 for one-half of each line cycle.

Reset Delay Capacitor

This capacitor, labeled C3 in Figure 10, is non-critical and is usually a low cost ceramic capacitor.

Table 1. DESIGN FORMULAE

FORMULA	EXAMPLE in FIGURE	COMMENTS
V_{OUT} = 5V ± 4%. V_{SET} Grounded	3	
$V_{OUT} = 1.3V\ (1 + \frac{R2}{R3})$	8	MAX610 and MAX612
$I_{OUT(MAX)} = C1 \times 4\ \sqrt{2} \times V_{RMS} \times F_{IN}$	3	Full wave — MAX610, MAX612
$I_{OUT(MAX)} = C1 \times 2\ \sqrt{2} \times V_{RMS} \times F_{IN}$	4	Half wave — MAX611
$I_{CURRENT\ LIMIT} = \frac{0.6V}{R_{SENSE}}$	9	
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 4\ \sqrt{2} \times F_{IN}}$	3	Full wave — MAX610, MAX612
$C1 = \frac{I_{OUT(MAX)}}{(V_{RMS} - V_{OUT}) \times 2\ \sqrt{2} \times F_{IN}}$	4	Half wave — MAX611
Time delay (in secs) = C3 (in μF) × 3	10	MAX611 only

Table 2. COMPONENT MANUFACTURERS

MFG	PART #	DESCRIPTION
Sprague	730P105X9250	1μF, 175V_{RMS} metallized polypropylene capacitor
	730P205X9250	2μF, 175V_{RMS} metallized polypropylene capacitor
	730P105X9400	1μF, 275V_{RMS} metallized polypropylene capacitor
	730P205X9400	2μF, 275V_{RMS} metallized polypropylene capacitor
TRW	TRW-40 1.0 20% 330VAC	1μF, 330VAC metallized polyester capacitor
	TRW-40 2.0 20% 330VAC	2μF, 330VAC metallized polyester capacitor
Aavid	5801B	Slip on heatsink for 8 pin Plastic DIP

Sprague Electric Co.
481 Marshall St.
North Adams, MA
(413) 664-4481

TRW Capacitor Division
301 W. O St.
Ogallala, NE 69153
(308) 284-3611

Aavid Engineering, Inc.
30 Cook Court, Box 400
Laconia, NH 03247
(603) 524-4443

The above table is included to assist you in obtaining components for use with the MAX610 family. This list is by no means inclusive and does not constitute an endorsement by Maxim Integrated Products.

AC To DC Regulator (110/220 VAC To 5.0V DC)

Cautions and Application Hints

1) Unless driven by a transformer, the 5V output of the MAX610/11/12 is **NOT ISOLATED** from the power line, and all circuitry connected to the MAX610/11/12 should be treated as if it were directly connected to the power line. The MAX610/11/12, its circuitry, and all components driven by the 5V output present a shock hazard and should be in a protective enclosure to prevent accidental contact.

2) Use an isolation transformer or ground fault interrupter (GFI) when breadboarding, testing, or troubleshooting a MAX610 family based line-power supply or any circuitry powered by the MAX610 family. If the MAX610/11/12 is connected directly to the power line, do **NOT** connect the ground of an oscilloscope to the circuit — this will severely damage the oscilloscope and destroy the MAX610/11/12.

3) When the 110/220VAC input is disconnected from a MAX610 family based power supply, the input capacitor, C1, may be left charged to the peak input line voltage, creating a shock hazard on the input terminals. The optional 1MΩ resistor shown in Figure 3 is recommended for use in any of the circuits when the input to the power supply may be disconnected or where the input capacitor must be discharged to prevent shock hazards to maintenance or service personnel.

4) C1 must be able to withstand the peak AC input voltage. The power source should be properly fused.

5) Observe the power dissipation limit. Excessive power dissipation will cause the junction temperature to rise above the absolute maximum rating and will degrade the reliability.

6.) Use the minimum value of C1 that will deliver the desired output current. Minimizing the value of C1 minimizes the dissipation of the MAX610/11/12, thus increasing the reliability of the power supply.

7) The over/undervoltage detection circuit is setup for 5V operation. Even if the V_{SET} terminal is used to set another output voltage, the over/undervoltage detection is left set at 4.65V and 5.4V.

8) If the value of C2, the raw DC filter capacitor, is above 750μF, limit the maximum output current by inserting a resistor between V_{OUT} and V_{SENSE}. This prevents damage to the MAX610/11/12 which might occur if the energy stored in a large valued C2 were discharged into a short circuit. If C2 is below 750μF this protection is not necessary.

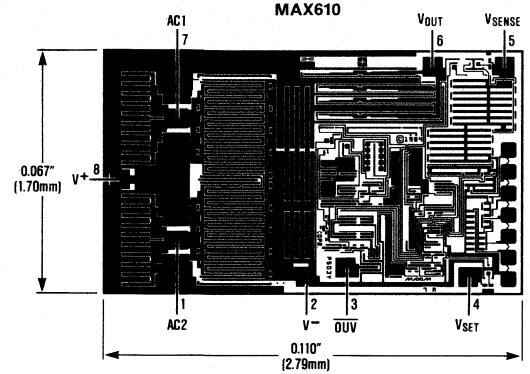
9) While the MAX610 family is stable without an output filter capacitor, it is good engineering practice to have power supply bypass capacitors on the output to compensate for the increased output impedance of the MAX610/11/12 at high frequency. A 47μF in parallel with a 0.1μF will keep the effective output impedance low from DC to greater than 1MHz.

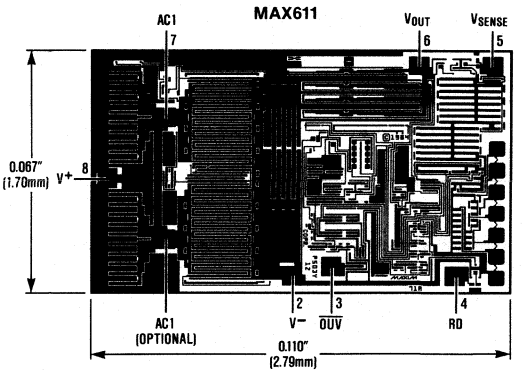
10) When powering the MAX610 or MAX612 through the V^+ terminal and using only the DC linear regulator, connect both AC1 and AC2 terminals to V^-.

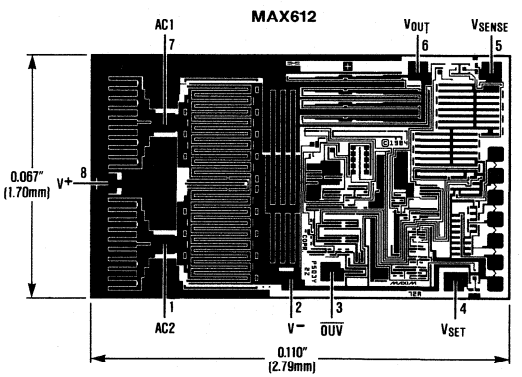
When using only the DC linear regulator portion of the MAX611 the AC1 terminal should be connected to V^-.

AC To DC Regulator (110/220 VAC To 5.0V ADC)

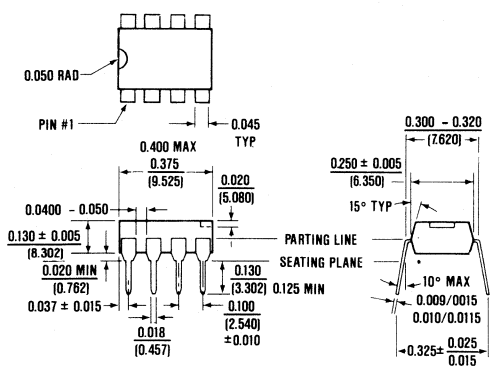
Chip Topography







Package Information



8 Lead Plastic DIP (P)

θ_{JA} = 125° C/W

θ_{JC} = 55° C/W

6

General Description

Maxim's MAX8211 and 8212 are CMOS micropower voltage detectors. Each contains a comparator, a 1.15V bandgap reference, and an open drain N-channel output driver. Two external resistors are used in conjunction with the internal reference to set the trip voltage to the desired level. A Hysteresis output is also included, allowing the user to apply positive feedback for noise-free output switching.

The MAX8211 provides a 7mA current-limited output sink whenever the voltage applied to the Threshold pin is less than the 1.15V internal reference. In the MAX8212, a voltage greater than 1.15V at the Threshold pin turns the output stage on (no current limit).

The MAX8211/8212 are plug-in replacements for the bipolar ICL8211/8212 in applications where the maximum supply voltage is less than 16.5V. They offer several performance advantages, including reduced supply current, a more tightly controlled bandgap reference, and more available current from the Hysteresis output.

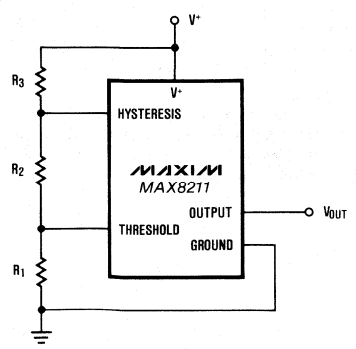
Applications

The 5μA quiescent current of the MAX8211 and MAX8212 make them suitable for a wide variety of voltage detection applications, especially in battery powered equipment.

Under Voltage Detection
Over Voltage Detection
Battery Backup Switching
Power Supply Fault Monitoring
Low Battery Detection

Maxim's ICL7665 Over/Under Voltage Detector is recommended for new designs requiring both low and high voltage detection.

Typical Operating Circuit



Logic Supply Under-Voltage Detector
(Detailed Circuit Diagram—Figure 5)

Features

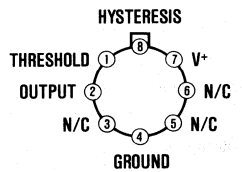
- **Improved 2nd Source for ICL8211/8212**
- **Low Power CMOS Design**
- **5μA Quiescent Current**
- **Onboard Hysteresis Outputs**
- **±40mV Threshold Accuracy (±3.5%)**
- **2.0V to 16.5V Supply Voltage Range**
- **Defined Output Current Limit—MAX8211**
- **High Output Current Capability—MAX8212**

Ordering Information

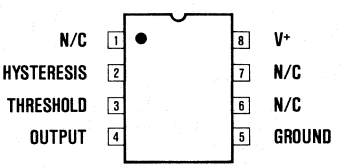
PART	TEMP. RANGE	PACKAGE
MAX8211CPA	0°C to +70°C	8 lead Mini DIP
MAX8211CTY	0°C to +70°C	TO-99 Can
MAX8211CSA	0°C to +70°C	8 lead Small Outline
MAX8212C/D	0°C to +70°C	Dice
MAX8212CPA	0°C to +70°C	8 lead Mini DIP
MAX8212CTY	0°C to +70°C	TO-99 Can
MAX8211C/D	0°C to +70°C	Dice
MAX8212CSA	0°C to +70°C	8 lead Small Outline

Pin Configuration

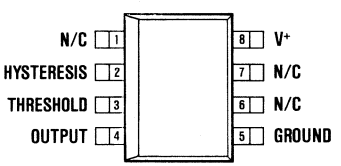
Top View



8 Lead TO-99 Metal Can



8 Lead Plastic DIP



8 Lead Small Outline

Programmable Voltage Detectors

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... -0.5 to +18 volts
Output Voltage ..... -0.5V to +18 volts
Hysteresis Voltage ..... +0.5 to -18 volts w.r.t. V^+
Threshold Input Voltage ..... $\leq V^+ +0.5$ volts
$\geq V$ GROUND -0.5 volts

Current into Any Terminal ..... ±50mA
Power Dissipation (Note 1) 300mW
Operating Temperature Range ..... 0°C to +70°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C
Storage Temperature Range ..... -65°C to +150°C

Note 1: Derate linearly above 50°C by -10mW/° C for MAX8211C/8212C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V^+ = 5V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MAX8211			MAX8212			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I^+	$2.0V \leq V^+ \leq 16.5V$ $GND \leq V_{TH} \leq V^+$		5	15		5	15	µA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 4mA, V_{OUT} = 2V $2V \leq V^+ \leq 16.5V$	1.11	1.15	1.19	1.11	1.15	1.19	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4mA I_{HYST} = 1mA		±0.1			±0.1		mV
Guaranteed Operating Supply Voltage Range	V_{SUPP}	+25°C 0°C to +70°C	2.0 2.2		16.5 16.5	2.0 2.2		16.5 16.5	V V
Typical Operating Supply Voltage Range	V_{SUPP}	+25°C	1.5		16.5	1.5		16.5	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	I_{OUT} = 4mA V_{OUT} = 2V		-200			-200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V^+$	ΔV^+ = 10% at V^+ = 5V		1.0			0.2		mV
Threshold Input Current	I_{TH}	$0 \leq V_{TH} \leq V^+$		0.01	10		0.01	10	nA
Output Leakage Current	I_{OLK}	V_{OUT} = 16.5V, V_{TH} = 1.0V V_{OUT} = 16.5V, V_{TH} = 1.3V V_{OUT} = 5V, V_{TH} = 1.0V V_{OUT} = 5V, V_{TH} = 1.3V			10 1			10 1	µA µA µA µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 2mA V_{TH} = 1.0V V_{TH} = 1.3V		0.17	0.4		0.17	0.4	V V
Max Available Output Current	I_{OH}	0°C to +70°C, V_{OUT} = 5V V_{TH} = 1.0V (Note 2) V_{TH} = 1.3V (Note 3)	4	7.0	30	12	35		mA
Hysteresis Leakage Current	I_{LHYS}	V^+ = 10V, V_{TH} = 1.0V V_{HYST} = -16.5V w.r.t.V^+			0.1			0.1	µA
Hysteresis Sat Voltage	$V_{HYS\ (max)}$	I_{HYST} = 0.5mA, V_{TH} = 1.3V measured with respect to V^+		-0.1	-0.2		-0.1	-0.2	V
Max Available Hysteresis Current	$I_{HYS\ (max)}$	V_{TH} = 1.3V	-2	-10		-2	-10		mA

NOTE 2: The maximum output current of the MAX8211 is limited by design to 30mA under any operating conditions. The output voltage may be sustained at any voltage up to +16.5V as long as the maximum power dissipation of the device is not exceeded.

NOTE 3: The maximum output current of the MAX8212 is not defined, and systems using the MAX 8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.

Detailed Description

As shown in the block diagrams of Figures 1 & 2, the MAX8211 and MAX8212 each contain a 1.15V reference, a comparator, an open drain n-channel output transistors, and an open drain p-channel hysteresis output. The MAX8211 output n-channel turns on when the voltage applied to the THRESHOLD pin is less than the internal reference (1.15V). The sink current is limited to 7mA (typical), allowing direct drive of an LED without a series resistor. The MAX8212 output turns on when the voltage applied to the THRESHOLD pin is greater than the internal reference. The output of the MAX8212 is not current limited, and will typically sink 35mA.

Compatibility with ICL8211/8212

The CMOS MAX8211/8212 are plug-in replacements for the bipolar ICL8211/8212 in most applications. The use of CMOS technology has several advantages. The quiescent supply current is much less than in the bipolar parts. Higher value resistors can also be used in the networks that set up the trip voltage, since the comparator input (THRESHOLD pin) is a low leakage MOS transistor. This further reduces system current drain. The tolerance of the internal reference has also been significantly improved, allowing for more precise voltage detection without the use of potentiometers.

The available current from the HYSTERESIS output has been increased from 21μA to 10mA making the hysteresis feature easier to use. The disparity between the voltage required at the THRESHOLD pin to switch the OUTPUT compared with the HYSTERESIS output has also been reduced in the MAX8211 from 8mV to 0.1mV to eliminate output "chatter" or oscillation.

Most voltage detection circuits operate with supplies that are 15V or less: in these applications, the MAX8211/8212 will replace ICL8211/8212s with the performance advantages described above. However it should be noted that the CMOS parts have an absolute maximum supply voltage rating of 18V, and should never be used in applications where this rating could be exceeded.

Caution should also be exercised when replacing ICL8211/8212s in closed loop applications such as programmable zeners. Although neither the ICL8211/8212 nor the MAX8211/8212 are internally compensated, the CMOS parts have higher gain and may not be stable for the external compensation capacitor values used in lower gain ICL8211/8212 circuits.

Typical Applications

Basic Voltage Detectors

Figure 3 shows the basic circuit for both under-voltage detection (MAX8211) and over-voltage detection (MAX8212). For applications where no hysteresis is needed, R_3 should be omitted. The ratio of R_1 to R_2 is then chosen such that, for the desired trip voltage at V_{IN}, 1.15V is applied to the THRESHOLD pin. Since the comparator inputs are very low leakage MOS transistors, the MAX8211/8212 can use much higher resistor values in the attenuator network than the bipolar ICL8211/8212.

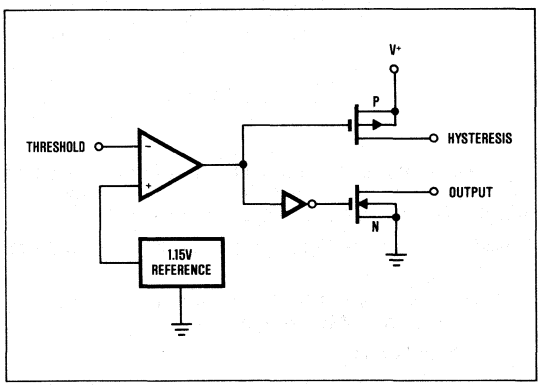


Figure 2. Block Diagram of MAX8212

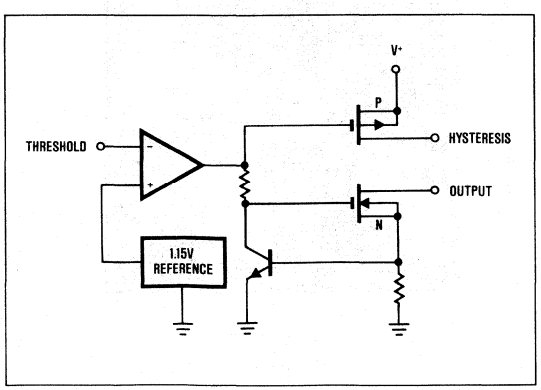


Figure 1. Block Diagram of MAX8211

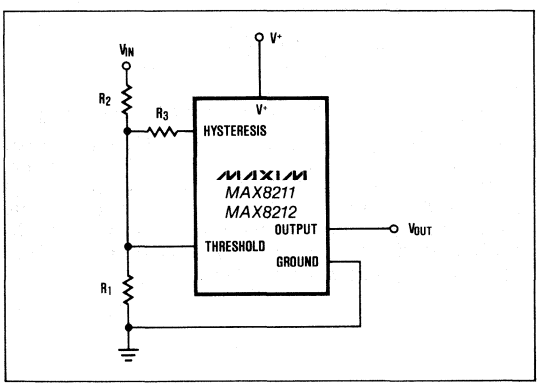


Figure 3. Basic Over-Voltage/Under-Voltage Circuit

Programmable Voltage Detectors

Voltage Detectors with Hysteresis

To ensure noise-free output switching, hysteresis is frequently used in voltage detectors. For both the MAX8211 and MAX8212, the HYSTERESIS output is ON for THRESHOLD voltages greater than 1.15V. R_3 (Figure 3) controls the amount of current (positive feedback) supplied from the HYSTERESIS output to the mid-point of the resistor divider, and hence the magnitude of the hysteresis, or dead-band.

Resistor values for Figure 3 should be calculated as follows:

1) Choose a value for R_1. Typical values are in the 10kΩ to 10MΩ range.
2) Calculate R_2 for the desired upper trip point V_U using the formula:

$$R_2 = R_1 \times \frac{(V_U - V_{TH})}{V_{TH}} = R_1 \times \frac{(V_U - 1.15V)}{1.15V}$$

3) Calculate R_3 for the desired amount of hysteresis, where V_L is the lower trip point:

$$R_3 = R_2 \times \frac{(V^+ - V_{TH})}{(V_U - V_L)} = R_2 \times \frac{(V^+ - 1.15V)}{(V_U - V_L)}$$

or if $V^+ = V_{IN}$

$$R_3 = R_2 \times \frac{(V_L - V_{TH})}{(V_U - V_L)} = R_2 \times \frac{(V_L - 1.15V)}{(V_U - V_L)}$$

Figure 4 shows an alternate circuit, suitable only when the voltage being detected is also the power supply voltage for the MAX8211 or MAX8212.

Resistor values for Figure 4 should be calculated as follows:

1) Choose a value for R_1. Typical values are in the 10kΩ to 10MΩ range.
2) Calculate R_2

$$R_2 = R_1 \times \frac{(V_L - V_{TH})}{V_{TH}} = R_1 \times \frac{(V_L - 1.15V)}{1.15V}$$

3) Calculate R_3

$$R_3 = R_1 \times \frac{(V_U - V_L)}{1.15V}$$

Low Voltage Detector for Logic Supply

The circuit of Figure 5 will detect when a 5.0V (nominal) supply goes below 4.5V, which is the V_{min} normally specified in logic systems. Resistor values have been selected which ensure that false under-voltage alarms will not be generated even with worst-case Threshold Trip Voltages and resistor tolerances. R_3 provides approximately 75mV of hysteresis.

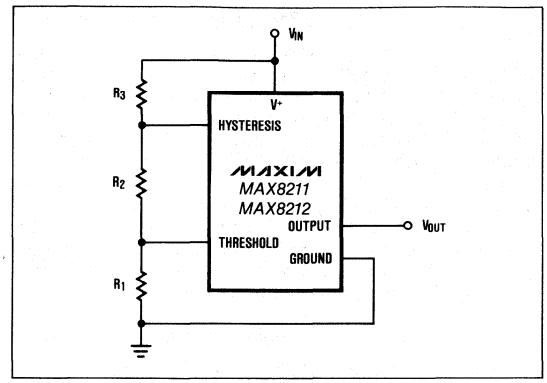


Figure 4. Alternate Circuit for $V_{IN} = V^+$

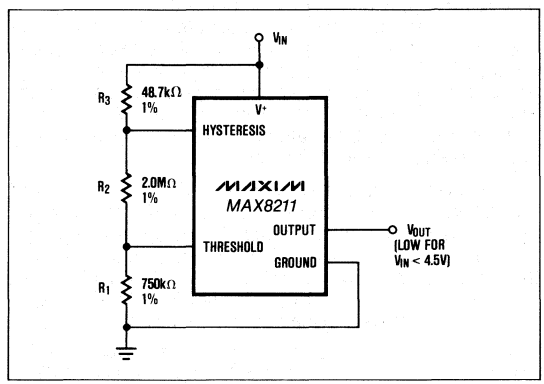
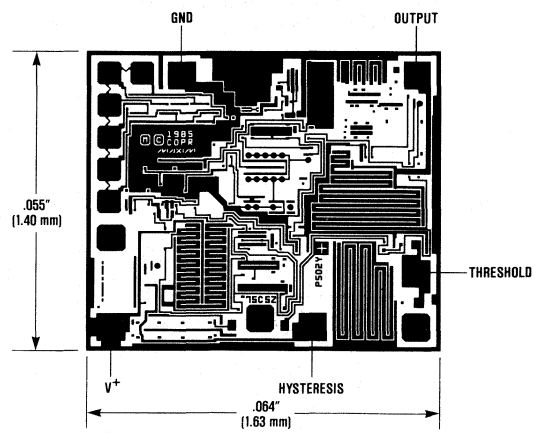


Figure 5. Logic Supply Low Voltage Detector

Chip Topography



4 Digit Up/Down Counter/Decoder/Driver

General Description

The MM74C945 and MM74C947 are synchronous 4 digit up/down counters with latches, 7-segment decoders, and all segment and backplane driver, and oscillator circuitry necessary to directly drive LCD displays.

Maxim's MM74C945 has a select input which allows the counter contents or the latch contents to be displayed, and a blanking input which allows the display to be blanked.

The MM74C947 only displays the latch contents, but provides leading zero blanking. The leading zero blanking input allows the user to force leading zeros to be displayed, and the leading zero output allows cascaded counters to blank leading zeroes properly.

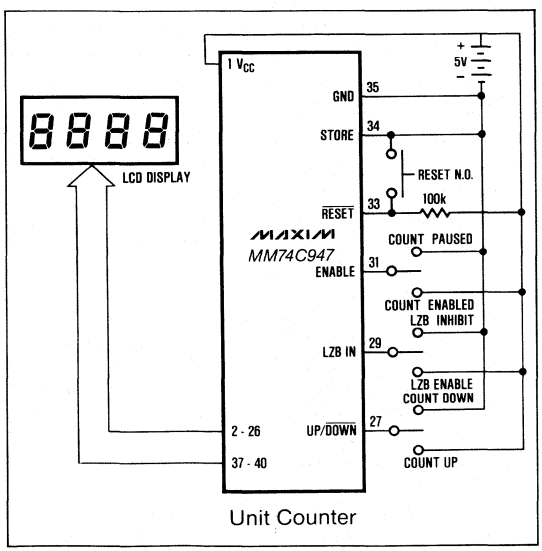
Both devices provide 28 segment outputs and a backplane input/output. When the oscillator pin is open, the device generates its own display waveform timing. When the oscillator pin is grounded, the backplane pin becomes an input.

The MM74C945 and MM74C947 are available in a 44 lead plastic chip carrier package in addition to the standard 40 lead plastic DIP.

Applications

Unit Counter
Frequency Counter
Tachometer
Hour Meter
Totalizer

Typical Operating Circuit



Unit Counter

Features

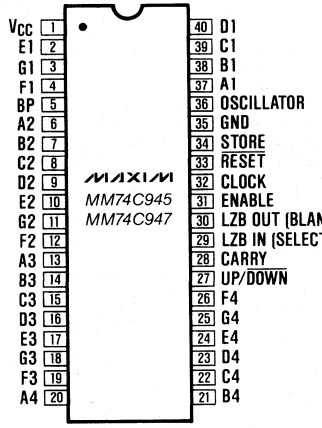
- **4 Decade Synchronous Up/Down Counter**
- **All Circuitry for Segments and Backplane of 4-Digit LCD**
- **Carry/Borrow Output Allows Ripple or Synchronous Cascading**
- **Schmitt Trigger Count Input**
- **Store and Reset Inputs Allow Operation as Frequency or Period Counter**
- **MM74C945 Provides Input to Select Display of Counter or Latch**
- **MM74C947 Provides Leading Zero Blanking Input and Output. Least Significant Digit May be Blanked.**

Ordering Information

PART	TEMP. RANGE	PACKAGE
MM74C945N	-40°C to +85°C	40 Lead Plastic DIP
MM74C945CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MM74C945C/D	0°C to +70°C	Dice
MM74C947N	-40°C to +85°C	40 Lead Plastic DIP
MM74C947CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
MM74C947C/D	0°C to +70°C	Dice

Pin Configuration

Top View



*Note:

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
29	Select	LZB In
30	Blanking	LZB Out

See Last Page for 44 Lead Chip Carrier Pin Configuration.

4 Digit Up/Down Counter/Decoder/Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Input Voltage ..... -0.3V to V^+ +0.3V
Power Dissipation
40 Lead Plastic Dip 0.5W
44 Lead Plastic Chip Carrier 0.5W

Operating V_{CC} Range ..... 3.0V to 6.0V
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Min/max limits apply across temperature range , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	V_{CC} = 5V, V_{IN} (0 → 5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Only)	V_{CC} = 5V, V_{IN} (5 → 0) V	1.5	2.2	2.4	V
Hysteresis (V_{T+} - V_{T-}) (Clock Only)	V_{CC} = 5V	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN\ (1)}$)	V_{CC} = 5V	3.5			V
Logical "0" Input Voltage ($V_{IN\ (0)}$)	V_{CC} = 5V			1.5	V
Logical "1" Output Voltage ($V_{OUT\ (1)}$)(LZO and Carry)	V_{CC} = 5V, I_O = -10 μA	4.5			V
Logical "0" Output Voltage ($V_{OUT\ (0)}$)(LZO and Carry)	V_{CC} = 5V, I_O = +10 μA			0.5	V
Clock Input Current $\|I_{IN}\|$	V_{CC} = 5V, V_{IN} = 5V/0V		0.005	1.0	μA
Input Current @ Pins 27, 29, 31, 33, and 34 (Note 1)	V_{CC} = 5V, V_{IN} = 0V V_{IN} = 5V			±0.1 ±0.1	μA μA
Oscillator Input Current (I_{OSL})	V_{CC} = 5V, V_{IN} = 0V/5V		±1	±10.0	μA
Supply Current (I_{CC})(Note 2)	V_{CC} = 5V, V_{IN} = 0V/5V		10	60	μA
Oscillator Input Voltage $V_{IH\ (OSC)}$ $V_{IL\ (OSC)}$	When Driving Oscillator Pin with External Signal	 0.2 V_{CC}		V_{CC} -0.2	 V V
DC Offset Voltage (Note 3)	V_{CC} = 5V			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN\ (1)}$)	V_{CC} = 4.75V	V_{CC}-1.5V			V
Logical "0" Input Voltage ($V_{IN\ (0)}$)	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT\ (1)}$)(LZO and Carry)	V_{CC} = 4.75V, I_O = -360 μA	2.4			V
Logical "0" Output Voltage ($V_{OUT\ (0)}$)(LZO and Carry)	V_{CC} = 4.75V, I_O = +360 μA			0.4	V
OUTPUT DRIVE (SHORT CIRCUIT CURRENT)					
Output Source Current (I_{SOURCE})(LZO and Carry)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	1.75	2.7		mA
Output Sink Current (I_{SINK})(LZO and Carry)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	1.75	3.2		mA
Output Source Current (I_{SOURCE})(Segment Outputs)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	1.4	2.0		mA
Output Sink Current (I_{SINK})(Segment Output)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	1.4	2.2		mA
Output Source Current (I_{SOURCE})(Backplane Output)	V_{CC} = 5V, V_{OUT} = 0V T_A = 25°C	12.6	15.0		mA
Output Sink Current (I_{SINK})(Backplane Output)	V_{CC} = 5V, V_{OUT} = 5V T_A = 25°C	12.6	20.0		mA

Note 1: Does not apply to backplane and oscillator pins. Does apply to pin 30 on MM74C945.
Note 2: Display blanked. See Test Circuit.
Note 3: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

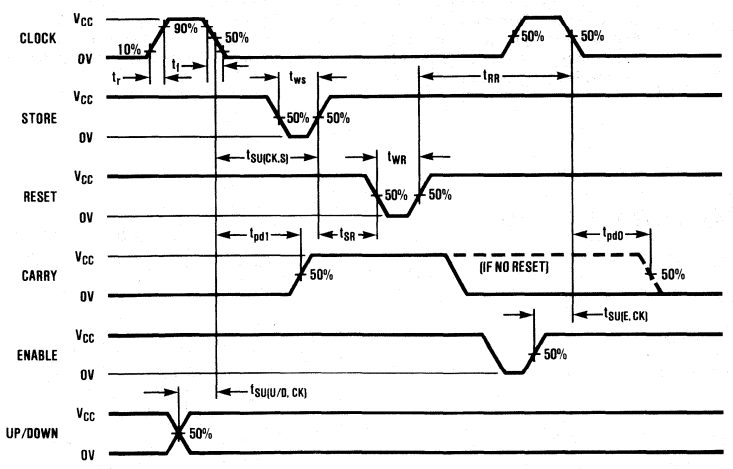
AC ELECTRICAL CHARACTERISTICS

T_j = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Clock to Carry	t_{pd0}, t_{pd1}	V_{CC}= 5.0V (Note 2)		600	800	ns
Maximum Clock Frequency	f_{CLK}	V_{CC}= 5.0V	2	3		MHz
Clock Input Rise/Fall Time	t_r, t_f	V_{CC}= 5.0V			No Limit	
Reset Pulse Width	t_{WR}	V_{CC}= 5.0V	180	120		ns
Store Pulse Width	t_{WS}	V_{CC}= 5.0V	150	80		ns
Clock to Store Set-Up Time	$t_{SU(CK, S)}$	V_{CC}= 5.0V	500	270		ns
Store to Reset Wait Time	t_{SR}	V_{CC}= 5.0V	280	170		ns
Enable to Clock Set-Up Time	$t_{SU(E, CK)}$	V_{CC}= 5.0V	140	80		ns
Reset Removal	t_{RR}	V_{CC}= 5.0V	50	0		ns
Up/Down to Clock Set-Up Time	$t_{SU(U/D, CK)}$	V_{CC}= 5.0V (Note 3)	600	300		ns
Backplane Output Frequency	f_{BP}	Pin 36 Floating, V_{CC}= 5.0V		85		Hz
Input Capacitance	C_{IN}	Logic Inputs (Note 1)		5		pF
Segment Rise/Fall Time	t_{rfs}	C_{Load}= 200 pF		0.5		μS
Backplane Rise/Fall Time	t_{rfb}	C_{Load}= 5000 pF		1.5		μS
Oscillator Frequency	f_{OSC}	Pin 36 Floating, V_{CC}= 5.0V		11		kHz

Note 1: Does not apply to backplane and oscillator pins. Does apply to pin 30 on MM74C945.
Note 2: National's MM74C945/947 is specified at 600ns maximum.
Note 3: National's MM74C945/947 is specified at 300ns minimum.

AC Waveforms



4 Digit Up/Down Counter/Decoder/Driver

TABLE 1. PIN DESCRIPTIONS

(Pin numbers correspond to 40 lead DIP package)

PIN	FUNCTION	DESCRIPTION
1	V_{CC}	Positive power supply
2-4 6-26 37-40	Segment Outputs	These 28 pins directly drive LCD display segments. Segments A1-G1 drive the least significant digit, segments A4-G4 drive the 1000s digit.
5	BACKPLANE	The backplane pin is both an input and an output. As an output it drives the LCD backplane with an internally generated backplane signal. The backplane pin is an input when the slave mode is selected by grounding pin 36, Oscillator.
27	UP/DOWN	This input controls the direction of counting. When high, counter counts up, when low, down.
28	CARRY	The CARRY output goes high when the ENABLE input is high and the counter is at 9999 counting up or at 0000 counting down. When the ENABLE input is low CARRY is low. This output may be used to ripple or synchronously cascade counters.
29	SELECT	When high, counter contents displayed. When low, latch contents displayed. MM74C945 only.
30	BLANKING	When high, entire display is blanked. MM74C945 only.
29	LZB IN	The MM74C947 displays leading zeroes when this pin is grounded. Connecting this pin to V_{CC} enables leading zero blanking. The entire display will be blanked if this pin is high, the counter is at 0000, and the oscillator pin is grounded. If the oscillator pin is floating, the least significant digit A1-G1 will not blank. MM74C947 only.
30	LZB OUT	This output allows the proper blanking of cascaded counters. The LZB OUT goes high when all digits are blanked. MM74C947 only.
31	ENABLE	When this input is low, the counter is inhibited and the CARRY output will be low. When this input is high, the counter is enabled.
32	CLOCK	Every negative-going transition at the CLOCK input clocks the counter. This input has a Schmitt trigger to prevent multiple clocking with slow rate-of-fall inputs.
33	RESET	A low level at this input will reset the counter to 0000. This input is inactive when high.
34	STORE	When the STORE input is low, the latches are transparent and the counter contents are displayed. When this input is high, the data is latched.
35	GROUND	The negative power supply input.
36	OSCILLATOR	When this pin is left floating, the chip oscillator will free-run at approximately 11kHz. Connecting an external capacitor between this pin and either power supply will lower the oscillator frequency as shown in the Typical Characteristics graphs. The oscillator may be overdriven but care must be taken to avoid swinging too close to ground. Grounding this pin puts the chip into the backplane slave mode making pin 5, BACKPLANE, into an input, and on the MM74C947 allowing the least significant digit to leading zero blank.

TABLE 1. TYPICAL LCD DISPLAYS

MANUFACTURER	PART NUMBER	DIGIT HEIGHT	NUMBER OF DIGITS
Epson (213) 534-0360	LD-H7924 LD-H7916 LD-K7994	0.350″ 0.500″ 0.700″	4½ 4 4
LXD (216) 292-3300	44D3F-85 44D3F-45	0.800″ 0.400″	4½ 4½
Hamlin (414) 648-2361	3909 3912	0.400″ 0.800″	4½ 4½
AND (415) 347-9916	FE0202W-DU FE0206W-DU	0.500″ 0.400″	4 4½

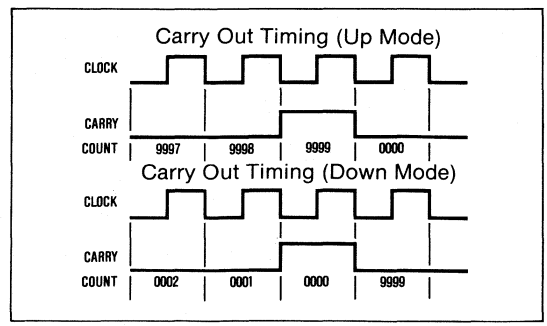


Figure 1. Carry Timing

4 Digit Up/Down Counter/Decoder/Driver

Applications Information

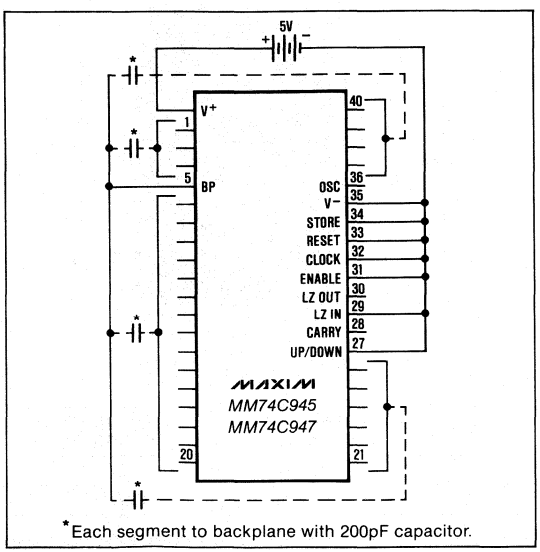
Display Drive Circuitry Description

The MM74C945 and MM74C947 have 28 segment outputs and a backplane input-output which directly drive a 4-digit seven-segment LCD display. The segment and backplane drivers are designed to provide matched rise and fall times which eliminates any DC component of the display signals maximizing display life.

The backplane driver may be disabled by connecting the oscillator pin to ground. In this mode, the backplane pin becomes an input, and the display waveforms will be synchronized with the signal applied to the pin. Several chips may be ganged in this manner, allowing the use of single-backplane displays with four, eight, twelve, etc. digits where one four-digit counter drives the backplane and the rest are slaved to it.

On the MM74C947, which implements leading zero blanking, the oscillator pin also controls the blanking of the least significant digit; when the oscillator pin is open (backplane master) the least significant digit will not blank, and when the oscillator pin is grounded, the entire display will blank when the latch contents of all four digits are zero and the Leading Zero Blanking input is high. In order to cascade counters and have leading zero blanking operate correctly, the least-significant counter should be the backplane master, with the other counters as slaves.

An on-board oscillator and divider chain generate the backplane and segment timing. The oscillator typically runs at 11kHz resulting in a backplane frequency of 85Hz. The oscillator may be slowed by connecting a capacitor between the oscillator pin and either power supply, or the oscillator pin may be overdriven by an external signal. When overdriving the oscillator, ensure that the input waveform does not swing close to ground to avoid putting the device into backplane slave mode. See VIH(osc) and VIL(osc) specifications.



*Each segment to backplane with 200pF capacitor.

Figure 2. Test Circuit

Counter Circuitry Description

The MM74C945/7 are synchronous four-decade up/down counters. A high level on the UP/DOWN input causes the counter to count up, while a low level at this input causes the counter to count down. The counter indexes on the negative-going edge of the CLOCK input. The CARRY output will be high for one clock period when the counter is at 9999 in up mode or 0000 in down mode. On the Maxim devices, the CARRY output will not go high if the ENABLE input is low. This ensures that synchronous cascading does not allow the higher-order digits to count incorrectly as can occur with the original manufacturer's device when the low-order counter ENABLE input is low and the counter is at 9999 up or 0000 down. As shown in the applications figures, the CARRY output allows synchronous or ripple cascading.

The RESET and ENABLE inputs are provided to allow these counters to perform frequency and period measurements. The counter is forced to 0000 when RESET is taken low, and the counter (including the CARRY output) is disabled when the ENABLE input is taken low.

The counter outputs are latched. The latches are transparent and the display will follow the counter when the STORE input is low. The latches store the counter outputs when the STORE input is taken high.

On the MM74C945 the SELECT input allows the counter or latch to be selected for display. When the SELECT input is high, the counter contents are displayed, and when low, the latch contents are displayed. The BLANKING input on the MM74C945 blanks the entire display when taken high. The MM74C945 does not implement leading zero blanking.

On the MM74C947 the latch contents are always displayed, but the decoders include leading zero blanking circuitry and two pins to allow cascaded counters to leading zero blank properly. When the LZB IN pin is low, leading zero blanking is inhibited. When the LZB IN is high, the device will blank leading zeros except for the least-significant digit when the oscillator pin is open (backplane master). When the oscillator pin is grounded (backplane slave) the device will blank all digits when in 0000, and the LZB OUT will go high.

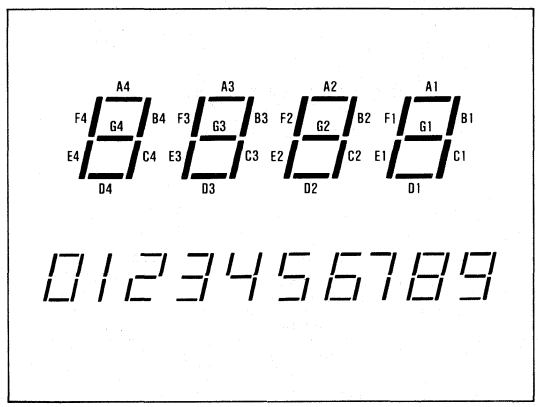
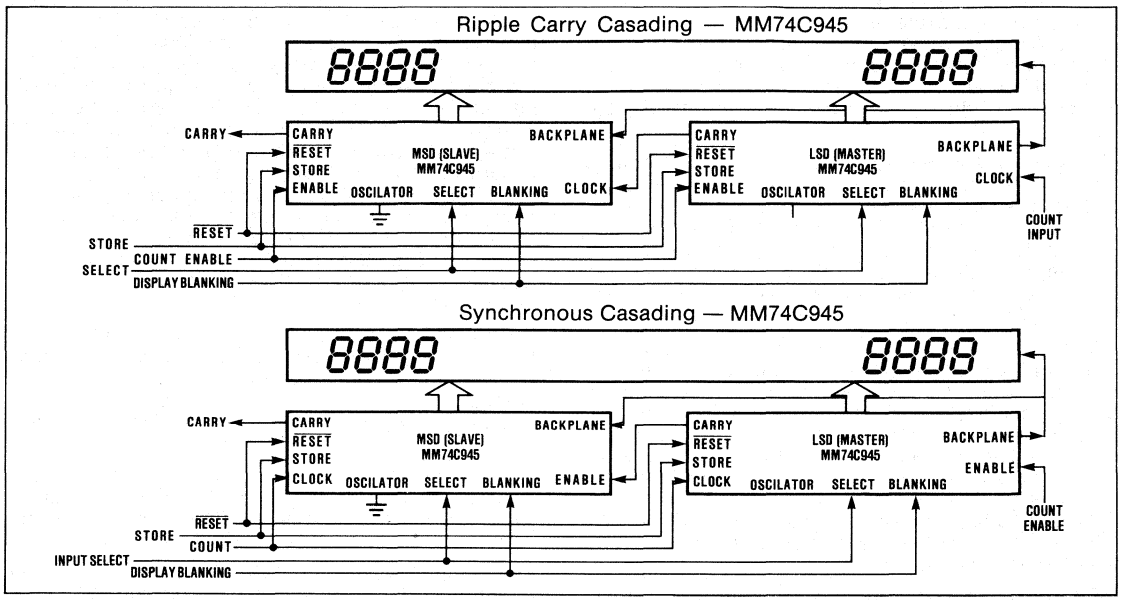


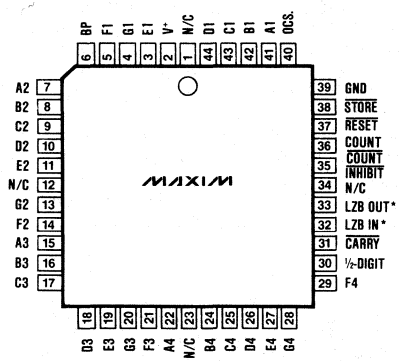
Figure 5. Segment Assignment and Display Font

4 Digit Up/Down Counter/Decoder/Driver

Typical Applications



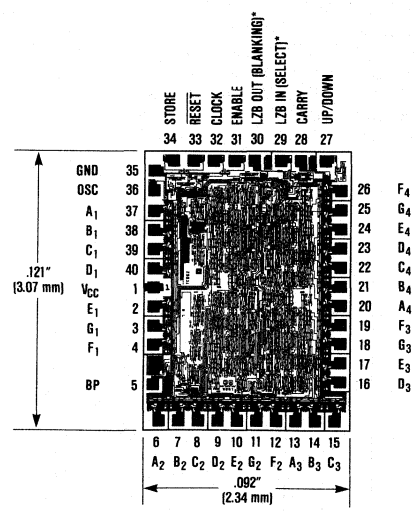
Pin Configuration



*Note:

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
32	Select	LZB IN
33	Blanking	LZB OUT

Chip Topography



*Note:

PIN #	MM74C945 FUNCTION	MM74C947 FUNCTION
29	Select	LZB IN
30	Blanking	LZB OUT

MAXIM

+5V, +10V Precision Voltage References

General Description

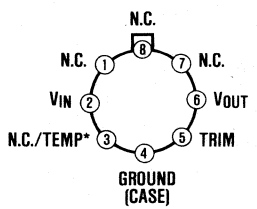
The REF01 and REF02 are precision voltages references that are pretrimmed to within ±.3% of 10V and 5V respectively. Both references feature excellent temperature stability (as low as 8.5 ppm/°C worst case), low current drain and low noise. The REF02 also provides a TEMP pin whose output voltage varies linearly with temperature, making this device suitable for a wide variety of temperature sensing and control applications. Both devices are available from Maxim in the space-saving Small Outline package, as well as the standard 8 pin TO-99 and MINI-DIP packages.

Applications

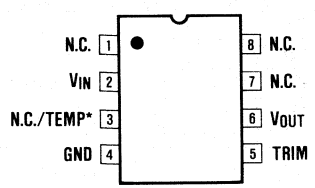
A to D Converters
D to A Converters
Digital Voltmeters
Voltage Regulators
Threshold Detectors

Pin Configuration

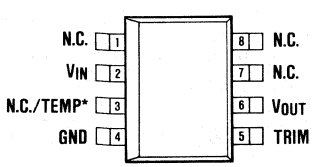
Top View



8 Lead TO-99 Metal Can



8 Lead DIP



8 Lead Small Outline

***NOTE:** Pin 3 is N.C. (No Connection) on REF01, TEMP Output on REF02

Features

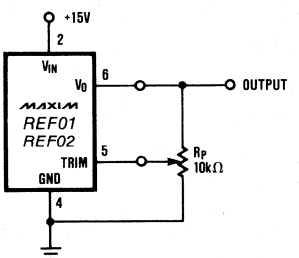
- **Pretrimmed to +5V, +10V ±0.3%**
- **Excellent Temperature Stability: 3ppm/°C**
- **Low Noise: 10μV_{p-p} (REF02)**
- **Low Supply Current: 1.4mA Max**
- **Short Circuit Proof**
- **Linear Temperature Transducer O/P (REF02)**

Ordering Information

PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C		
REF01EJ	10V ± 30mV	TO-99
REF01HJ	10V ± 50mV	TO-99
REF01CJ	10V ± 100mV	TO-99
REF01EZ	10V ± 30mV	Hermetic DIP
REF01HZ	10V ± 50mV	Hermetic DIP
REF01CZ	10V ± 100mV	Hermetic DIP
REF01HP	10V ± 50mV	Plastic DIP
REF01CP	10V ± 100mV	Plastic DIP
REF01HSA	10V ± 50mV	Small Outline
REF01CSA	10V ± 100mV	Small Outline
TEMP RANGE: -55°C TO +125°C		
REF01AJ	10V ± 30mV	TO-99
REF01J	10V ± 50mV	TO-99
REF01AZ	10V ± 30mV	Hermetic DIP
REF01Z	10V ± 50mV	Hermetic DIP

(Ordering information continued on last page.)

Typical Operating Circuit



Reference with Trimmed Output

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF01

Input Voltage
- REF01, A, E, H, All DICE 40V
- REF01C 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Output Short-Circuit Duration
- (to Ground or V_{IN}) ..... Indefinite

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF01A, REF01 ..... -55°C to +125°C
- REF01E, REF01H, REF01C ..... 0°C to +70°C

DICE Junction Temperature (T_j) ..... -65°C to +150°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	9.97	10.00	10.03	9.95	10.00	10.05	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3.0	±3.3	—	±3.0	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	20	30	—	20	30	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 4)		I_L = 0 to 10mA	—	0.005	0.008	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF01A and REF01, 0°C ≤ T_A ≤ +70°C for REF01E and REF01H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01A/E			REF01/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 1, 2)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	3.0	8.5	—	10.0	25.0	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 13V to 33V)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 4)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA

Note 1: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 10V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{10V} \right| \times 100$$

Note 2: ΔV_{OT} specification applies trimmed to +10.000V or untrimmed.
Note 3: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 4: Line and Load Regulation specifications include the effect of self heating.
Note 5: Sample tested.

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	9.90	10.00	10.10	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±3.3	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 5)	—	25	35	μV_{p-p}
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.009	0.015	%/V
Load Regulation (Note 4)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 0.006	0.015 0.015	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	mA
Load Current	I_L		8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	mA

ELECTRICAL CHARACTERISTICS—REF01

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF01C			UNITS
			MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 1 and 2)	—	0.14	0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 3)	—	20	65	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	ppm/%
Line Regulation (Note 4)		V_{IN} = 13V to 30V	—	0.011	0.018	%/V
Load Regulation (Note 4)		I_L = 0 to 5mA	—	0.008	0.018	%/mA

Notes: See previous page.

Output Adjustment

The REF01 trim terminal can be used to adjust the voltage over a 10V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 10V, including 10.240V for binary applications (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. The temperature coefficient change is approximately 0.7 ppm/°C for 100mV of output adjustment.

Burn-in Circuit

The burn-in circuit of Figure 1 is used for both the REF01 and the REF02. All Maxim REF01s and REF02s are 100% burned-in for a minimum of 24hrs at 150°C (except for Small Outline package), which is equivalent to 25 years of operation at 25°C. This substantially improves the long term stability of the part, and allows Maxim to offer a product with a F.I.T. rate of better than 10 (See Product Reliability Report RR-1A).

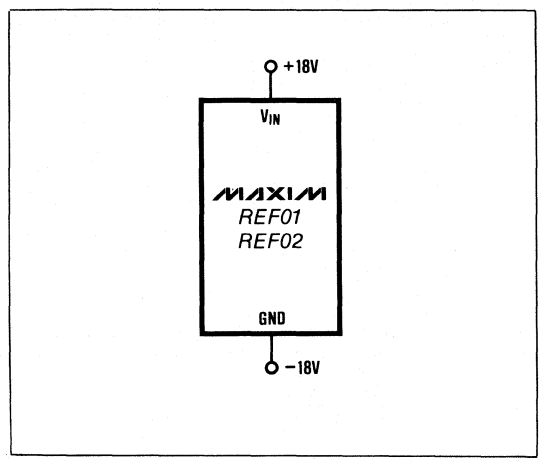


Figure 1. Burn-in circuit

+5V, +10V Precision Voltage References

ABSOLUTE MAXIMUM RATINGS—REF02

Input Voltage
- REF02, A, E, H, All DICE 40V
- REF02C, D 30V

Power Dissipation
- T099 (J) 500mW
  (Derate at 7.1mW/°C above 80°C)
- CERDIP (Z) 500mW
  (Derate at 6.7mW/°C above 75°C)
- Plastic DIP (P) 500mW
  (Derate at 5.6mW/°C above 36°C)
- Small Outline (S) 300mW
  (Derate at 5.0mW/°C above 55°C)

Storage Temperature Range ..... -65°C to +150°C

Operating Temperature Range
- REF02A, REF02 ..... -55°C to +125°C
- REF02E, REF02H ..... 0°C to +70°C
- REF02C, REF02D ..... 0°C to +70°C

Lead Temperature (Soldering, 60 sec.) ..... +300°C

DICE Junction Temperature (T_j) ..... -65°C to +150°C

Output Short-Circuit Duration
(to Ground or V_{IN}) ..... Indefinite

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = +25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0	4.985	5.000	5.015	4.975	5.000	5.025	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±3	±6	—	±3	±6	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	10	15	—	10	15	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 33V	—	0.006	0.010	—	0.006	0.010	%/V
Load Regulation (Note 1)		I_L = 0 to 10mA	—	0.005	0.010	—	0.006	0.010	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.4	—	1.0	1.4	mA
Load Current	I_L		10	21	—	10	21	—	mA
Sink Current	I_S		-0.3	-0.5	—	-0.3	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, -55°C ≤ T_A ≤ +125°C for REF02A and REF02, 0°C ≤ T_A ≤ +70°C for REF02E and REF02H, I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02A/E			REF02/H			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature (Notes 3, 4)	ΔV_{OT}	0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.02 0.06	0.06 0.15	— —	0.07 0.18	0.17 0.45	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	3	8.5	—	10	25	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (V_{IN} = 8V to 33V)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.007 0.009	0.012 0.015	— —	0.007 0.009	0.012 0.015	%/V
Load Regulation (I_L = 0 to 8mA)(Note 1)		0°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C	— —	0.006 0.007	0.010 0.012	— —	0.007 0.009	0.012 0.015	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Note 1: Line and Load Regulation specifications include the effect of self heating.
Note 2: Limit current in or out of pin 3 to 50nA and capacitance on pin 3 to 30pF.
Note 3: ΔV_{OT} is defined as the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range expressed as a percentage of 5V:

$$\Delta V_{OT} = \left| \frac{V_{MAX} - V_{MIN}}{5V} \right| \times 100$$

Note 4: ΔV_{OT} specification applies trimmed to +5.000V or untrimmed.
Note 5: TCV_O is defined as ΔV_{OT} divided by the temperature range.
Note 6: Sample tested.

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, T_A = 25°C, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	V_O	I_L = 0mA	4.950	5.000	5.050	4.900	5.000	5.100	V
Output Adjustment Range	ΔV_{trim}	R_p = 10kΩ	±2.7	±6.0	—	±2.0	±6.0	—	%
Output Voltage Noise	e_{np-p}	0.1Hz to 10Hz (Note 6)	—	12	18	—	12	—	μV_{p-p}
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.009	0.015	—	0.010	0.04	%/V
Load Regulation (Note 1)		I_L = 0 to 8mA I_L = 0 to 4mA	— —	0.006 —	0.015 —	— —	— 0.015	— 0.04	%/mA
Turn-on Settling Time	t_{ON}	To ±0.1% of final value	—	5	—	—	5	—	μs
Quiescent Supply Current	I_{SY}	No Load	—	1.0	1.6	—	1.0	2.0	mA
Load Current	I_L		8	21	—	8	21	—	mA
Sink Current	I_S		-0.2	-0.5	—	-0.2	-0.5	—	mA
Short-Circuit Current	I_{SC}	V_O = 0	—	30	—	—	30	—	mA
Temperature Voltage Output	V_T	(Note 2)	—	630	—	—	630	—	mV

ELECTRICAL CHARACTERISTICS—REF02

(V_{IN} = +15V, 0°C ≤ T_A ≤ +70°C and I_L = 0mA, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	REF02C			REF02D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Change with Temperature	ΔV_{OT}	(Notes 3 and 4)	—	0.14	0.45	—	0.49	1.7	%
Output Voltage Temperature Coefficient	TCV_O	(Note 5)	—	20	65	—	70	250	ppm/°C
Change in V_O Temperature Coefficient with Output Adjustment		R_p = 10kΩ	—	0.7	—	—	0.7	—	ppm/%
Line Regulation (Note 1)		V_{IN} = 8V to 30V	—	0.011	0.018	—	0.012	0.05	%/V
Load Regulation (Note 1)		I_L = 0 to 5mA	—	0.008	0.018	—	0.016	0.05	%/mA
Temperature Voltage Output Temperature Coefficient	TCV_T	(Note 2)	—	2.1	—	—	2.1	—	mV/°C

Notes: See previous page.

Output Adjustment

The REF02 trim terminal can be used to adjust the output voltage over a 5V ±300mV range. This feature allows the system designer to trim system errors by setting the reference to a voltage other than 5V (see "Typical Operating Circuit" on first page).

Adjustment of the output does not significantly affect the temperature performance of the device. Typically, the temperature coefficient change is 0.7ppm/°C for 100mV of output adjustment.

Temperature Voltage Output

The REF02 provides a temperature dependent output voltage on the TEMP pin. This voltage is proportional to the absolute temperature, and has a scale factor of approximately 2.1mV/°C (Figure 2).

Output Voltage = 2.1(T + 273)mV
where T = Temperature in °C

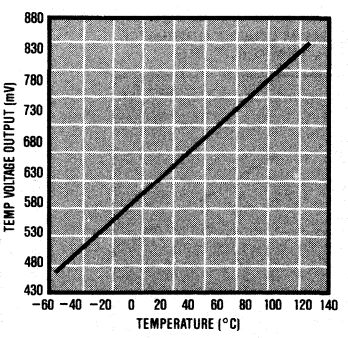
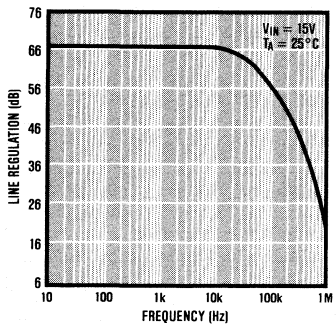


Figure 2. REF02 Temperature Voltage Output vs. Temperature.

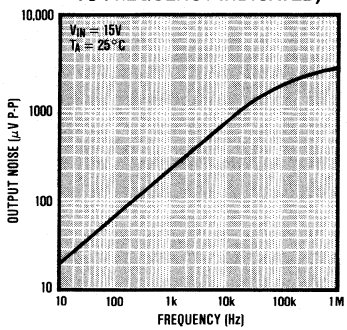
+5V, +10V Precision Voltage References

Typical Operating Characteristics

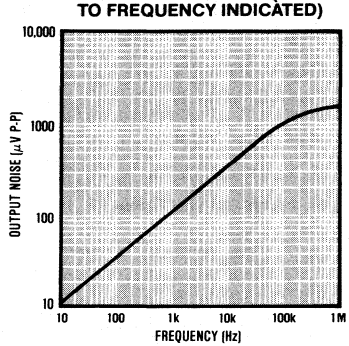
LINE REGULATION vs FREQUENCY



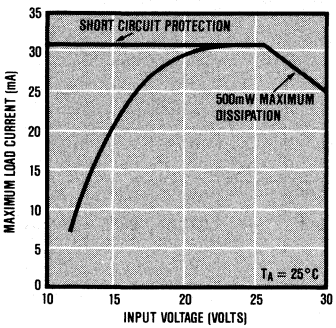
REF01 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



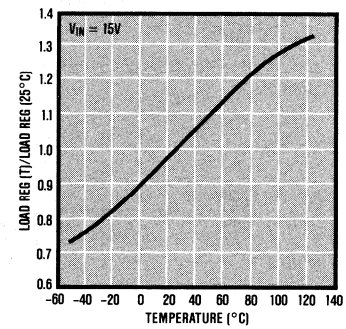
REF02 OUTPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



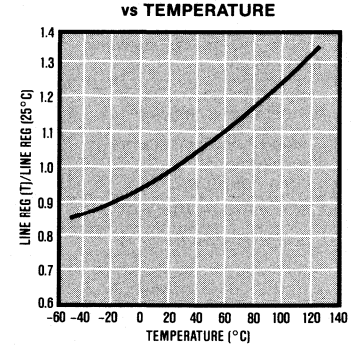
MAXIMUM LOAD CURRENT vs INPUT VOLTAGE



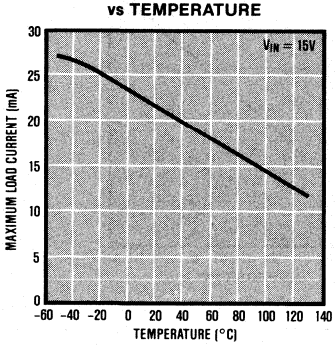
NORMALIZED LOAD REGULATION (ΔI_L = 10 mA) vs TEMPERATURE



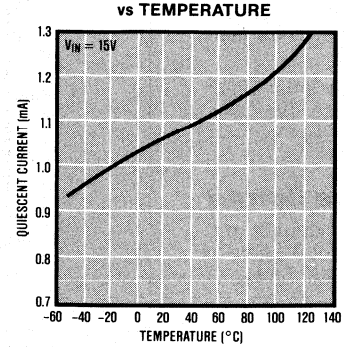
NORMALIZED LINE REGULATION vs TEMPERATURE



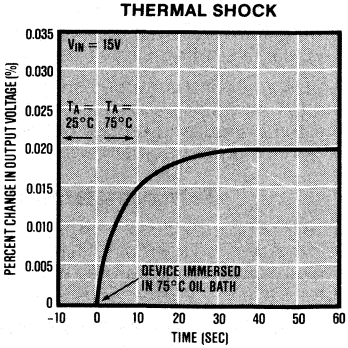
MAXIMUM LOAD CURRENT vs TEMPERATURE



QUIESCENT CURRENT vs TEMPERATURE



OUTPUT CHANGE DUE TO THERMAL SHOCK



Typical Applications

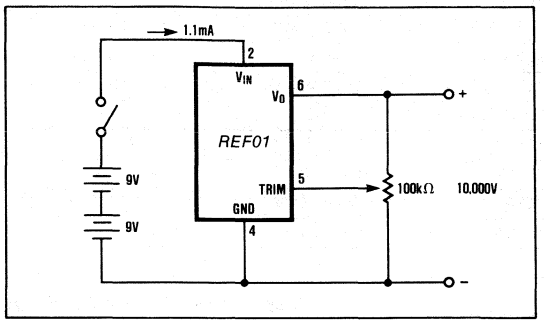


Figure 3. Precision Calibration Standard

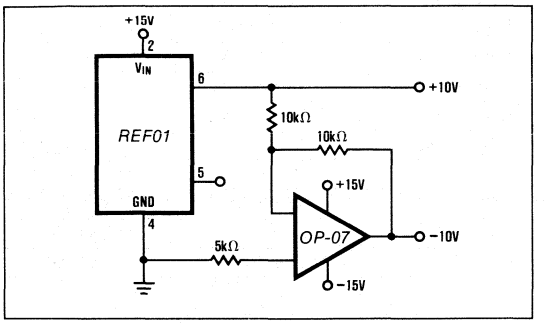


Figure 4. ±10V Reference

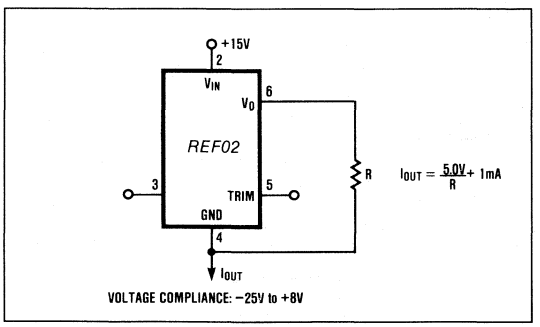


Figure 5. Current Source

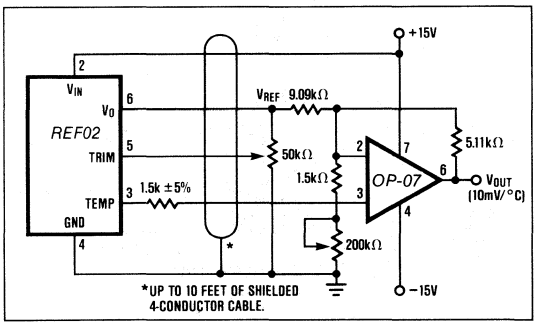
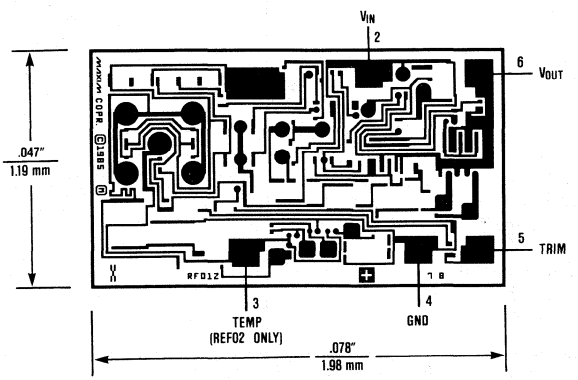


Figure 6. Precision Temperature Transducer with Remote Sensor

Chip Topography



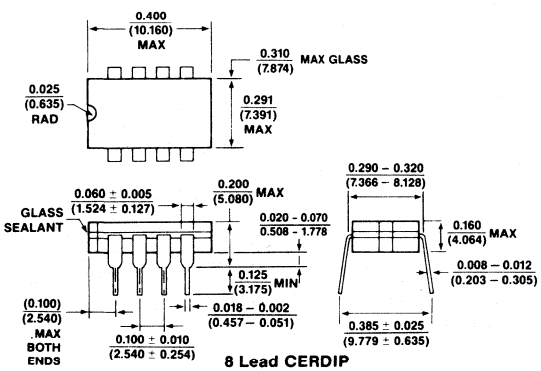
+5V, +10V Precision Voltage References

Ordering Information

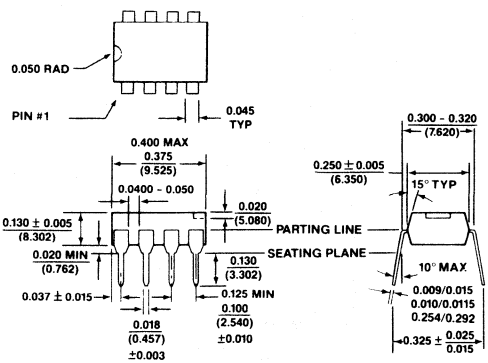
(Continued from first page)

PART	V_{OUT} @ 25°C	PACKAGE	PART	V_{OUT} @ 25°C	PACKAGE
TEMP RANGE: 0°C TO +70°C			**TEMP RANGE: 0°C TO +70°C**		
REF02EJ	5V ± 15mV	TO-99	REF02DP	5V± 100mV	Plastic DIP
REF02HJ	5V ± 25mV	TO-99	REF02HSA	5V ± 25mV	Small Outline
REF02CJ	5V ± 50mV	TO-99	REF02CSA	5V ± 50mV	Small Outline
REF02DJ	5V ± 100mV	TO-99	REF02DSA	5V ± 100mV	Small Outline
REF02EZ	5V ± 15mV	Hermetic DIP	**TEMP RANGE: -55°C TO +125°C**		
REF02HZ	5V ± 25mV	Hermetic DIP	REF02AJ	5V ± 15mV	TO-99
REF02CZ	5V ± 50mV	Hermetic DIP	REF02J	5V ± 25mV	TO-99
REF02DZ	5V ± 100mV	Hermetic DIP	REF0AZ	5V ± 15mV	Hermetic DIP
REF02HP	5V ± 25mV	Plastic DIP	REF0AZ	5V ± 25mV	Hermetic DIP
REF02CP	5V ± 50mV	Plastic DIP			

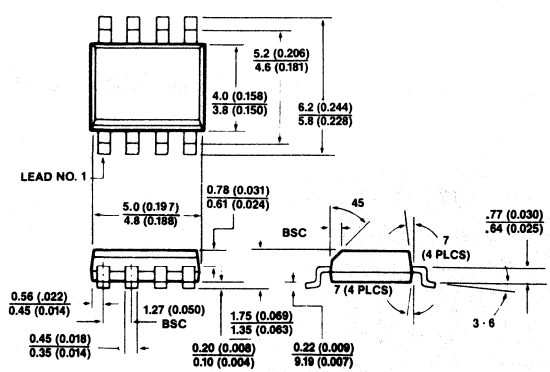
Package Information



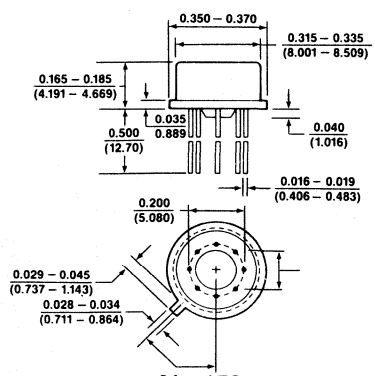
8 Lead CERDIP
θ_{JA} = 125° C/W
θ_{JC} = 55° C/W



8 Lead Plastic DIP
θ_{JA} = 160° C/W
θ_{JC} = 75° C/W



8-Lead Small Outline (SO)
θ_{JA} = 180°C/W
θ_{JC} = 90°C/W



8 Lead TO-99 Can
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

Appendix

A

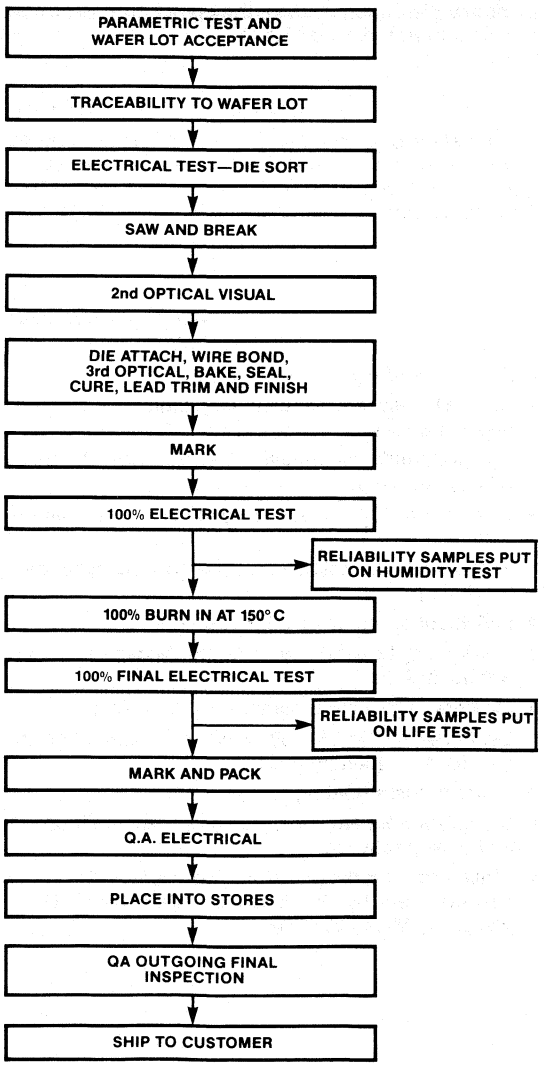
Packaged Unit Process Flow

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below IpA current levels, and less than IpF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.



Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature.* This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85° C/85%) cycles. In addition, *every unit shipped has been burned-in* (with the exception of Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including 100% burn-in, at no additional cost.*

Surface Mount Products

Maxim is committed to providing high-quality, high-reliability 8-44 lead plastic surface mount products. These products are processed through the same manufacturing flow as the Dual-in-Line (DIP) plastic parts and are tested to the same stringent electrical and visual AQL levels. They receive the same product conditioning and lot qualification as the DIPs with the exception of 100% burn-in. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a Long-term Life Test prior to shipment.

A

Die and Wafer Sales Information

All Maxim's standard products are available in die and wafer form. Maxim's precision wafer test equipment is the most sophisticated in the industry. All products are tested in wafer form to limits that are, with very few exceptions, more stringent than the data sheet 25° C worst case parameters. Furthermore, when product is shipped in die or wafer form, die from that lot are assembled into packaged units and subjected to the "Package Unit Process Flow" (Page A-1) to ensure lot quality and reliability.

Maxim produces devices on 3" and 4" wafers. Chip thickness dimensions differ for 3" and 4" wafers and for backlapped and unbacklapped wafers.

Physical Specifications

PARAMETER		3"	4"	Units
Chip Thickness	Backlapped wafers	13 ± 1	15 ± 1	mils
	Unbacklapped wafers	15 ± 1	20.7 ± 1	mils
Die length/width tolerance		±1		mils
Bonding pads dimensions (minimum)		4.0 × 4.0		mils
Bonding pad and interconnect material thickness		10K - 15K		A
Storage temperature		-40 to +150		°C
Operating temperature		-20 to +70		°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010.2, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by HF etching or by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.

Maxim guarantees die and wafer AQL levels as follows:

Visual 1.0%
Functional Electrical Testing 0.65%
Parametric DC testing 2.5%
Untested Parameters 6.5%

Recommended Assembly Procedures

Recommended Handling

Maxim recommends that die and wafers be stored in a clean, dry, ambient—preferably inert—gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment and harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385° C and 435° C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150° C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Packages

- **Easy to handle, store and inventory.**
- **100% visually sorted with mechanical and visual rejects removed.**
- **Die are 100% electrically probed with electrical rejects removed.**
- **Wafers are 100% electrically probed with rejects inked.**
- **Easy visual inspection—dice are in carriers, geometry side up.**
- **Individual compartment for each die.**
- **Carrier may be used as storage container for unused wafers and die.**
- **Carriers usable in customer production area.**
- **Die carriers hold 25, 100 or 400 die, depending on die size and quantity ordered.**
- **Wafer carriers hold up to 10 wafers.**
- **Die and wafers are packaged as shown in Figures 1 and 2, respectively.**
- **When ordering die in wafer form, replace "D" in the part numbers by "W." Example: MAX 7231C/D replaced by MAX 7231C/W.**

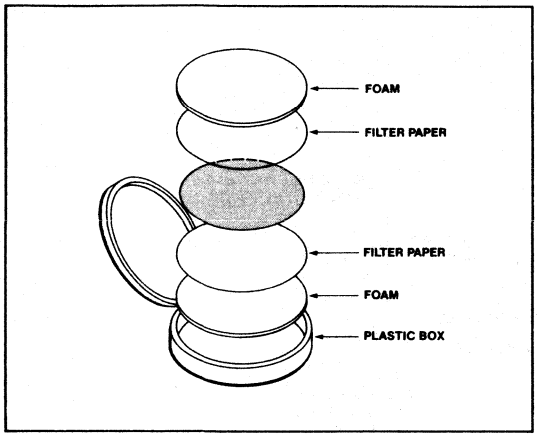


Figure 1. Wafer Carrier Package

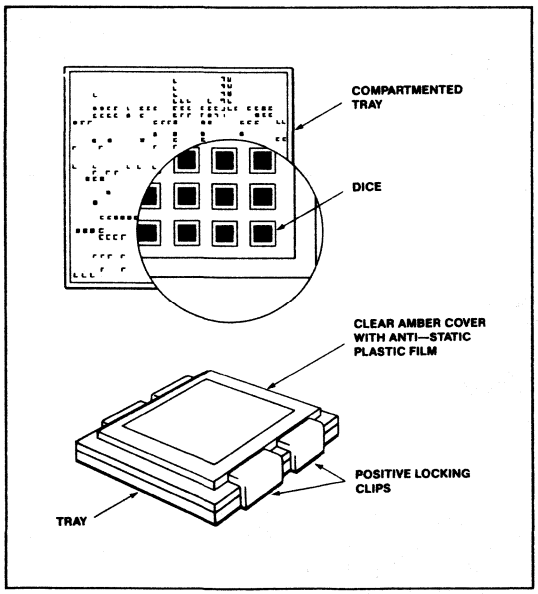


Figure 2. Die Carrier Package

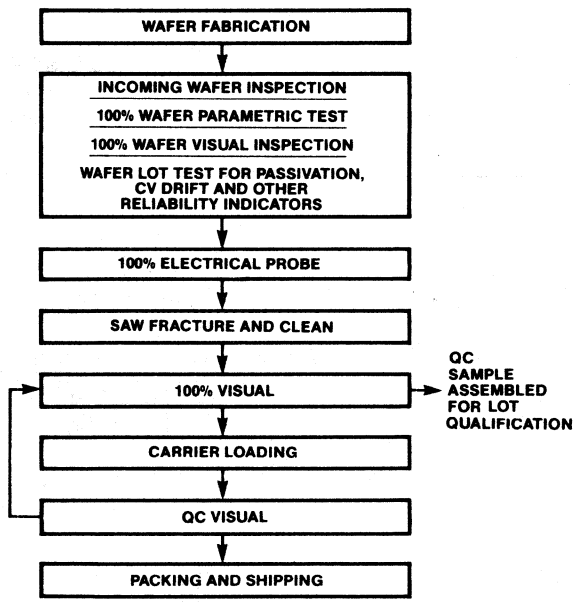
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

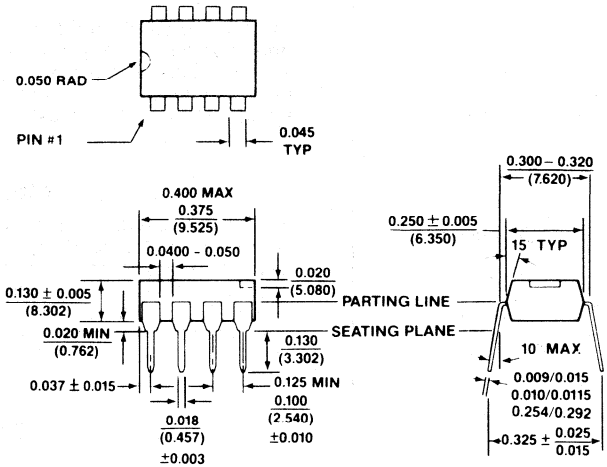
User Responsibility

Written notification of any non-conformance by Maxim of Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



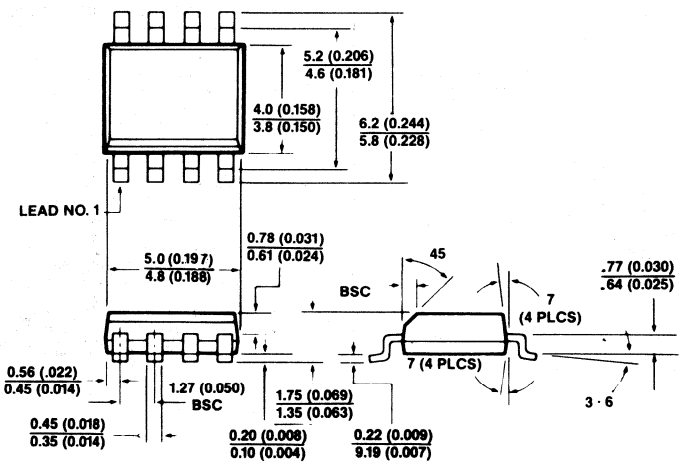
A



8 Lead Plastic Dip (PA)

$\theta_{JA} = 160°$ C/W

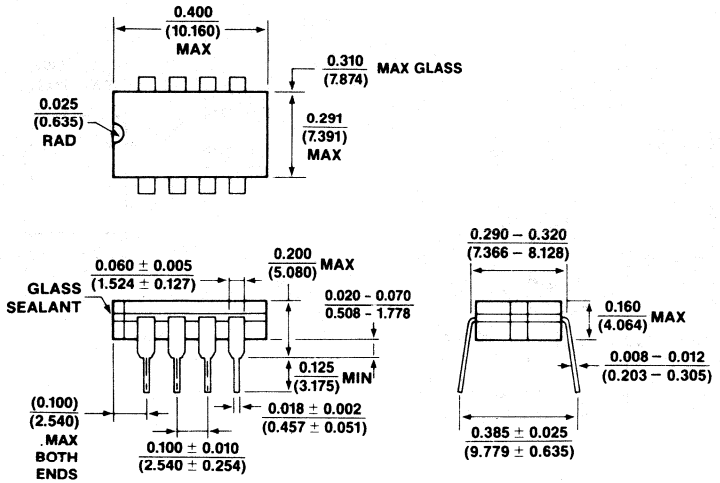
$\theta_{JC} = 75°$ C/W



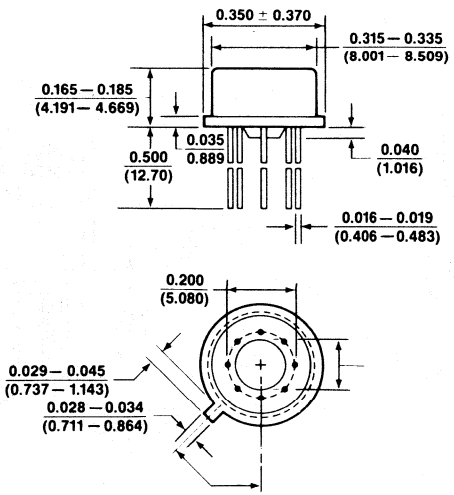
8 Lead Small Outline (SO)

$\theta_{JA} = 170°$ C/W

$\theta_{JC} = 80°$ C/W

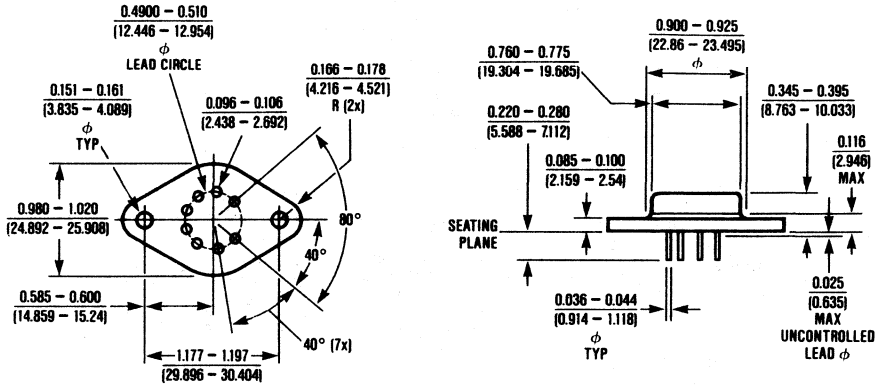


8 Lead CERDIP (JA)
$\theta_{JA} = 125°$ C/W
$\theta_{JC} = 55°$ C/W

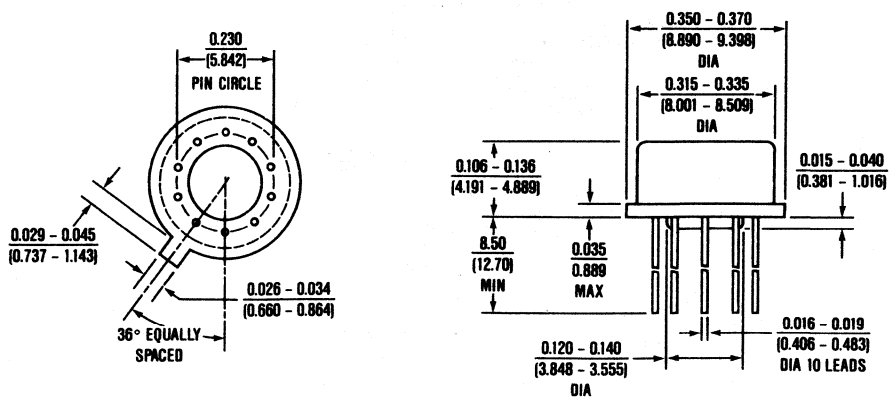


8 Lead TO-99 Can (TV)
$\theta_{JA} = 150°$ C/W
$\theta_{JC} = 45°$ C/W

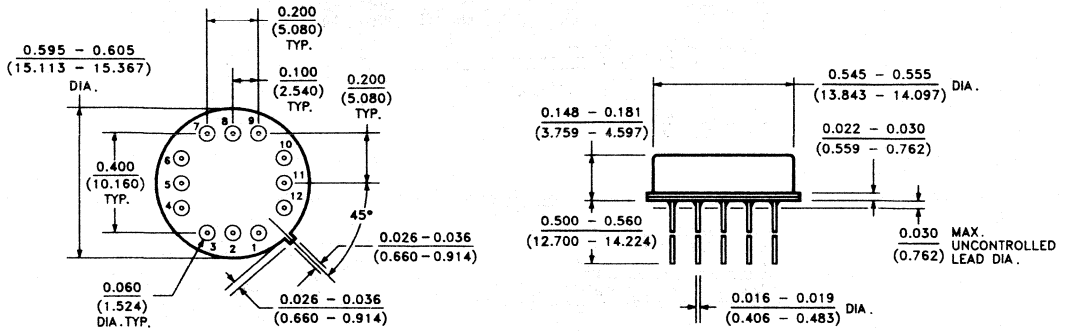
A



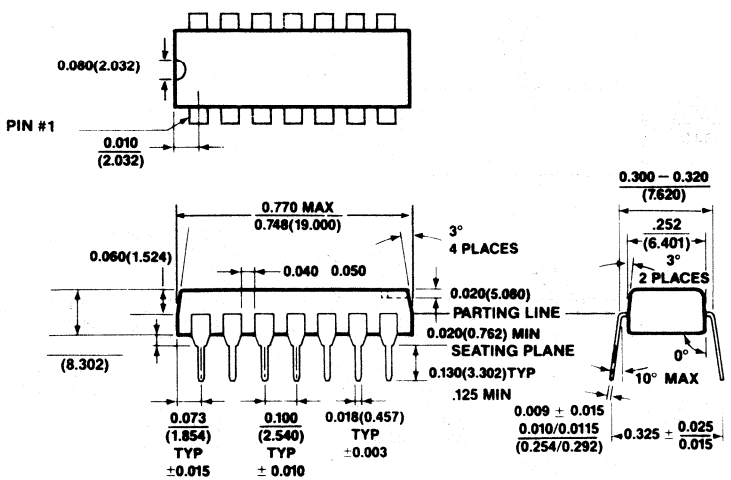
8 Lead TO-3 Can (K)
θ_{JA} = 25° C/W
θ_{JC} = 2° C/W



10 Lead TO-100 Can (TW)
θ_{JA} = 150° C/W
θ_{JC} = 45° C/W

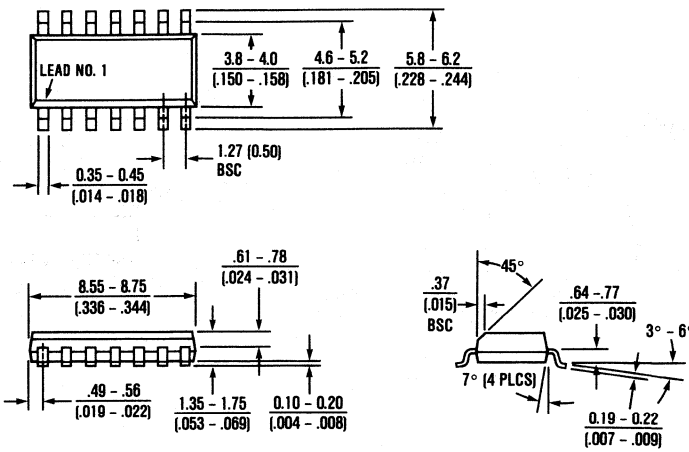


12 Lead TO-8 Can (G)
$\theta_{JA} = 100°$ C/W
$\theta_{JC} = 60°$ C/W



14 Lead Plastic Dip (PD)
$\theta_{JA} = 140°$ C/W
$\theta_{JC} = 70°$ C/W

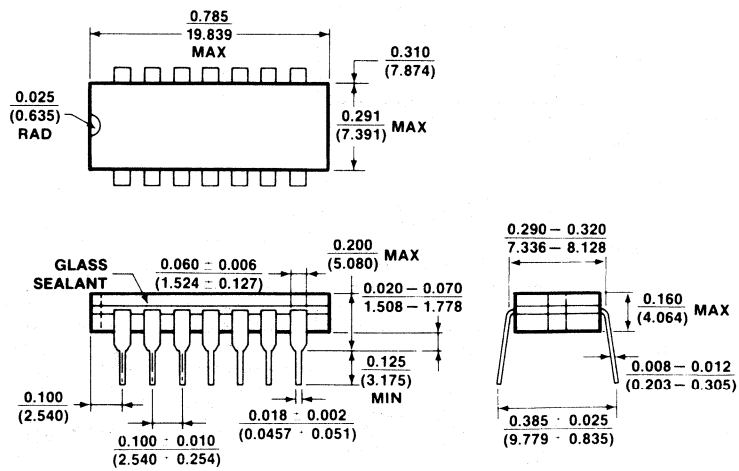
A



14 Lead Small Outline (SD)

$\theta_{JA} = 115°$ C/W

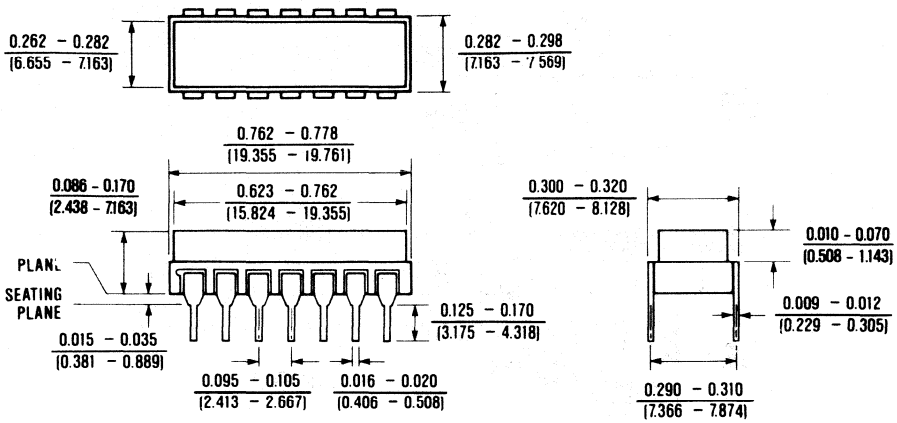
$\theta_{JC} = 60°$ C/W



14 Lead CERDIP (JD)

$\theta_{JA} = 105°$ C/W

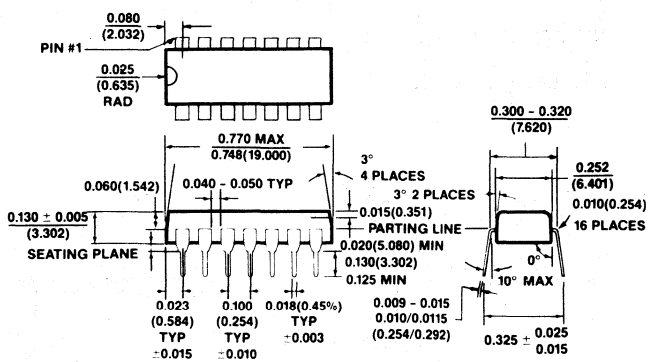
$\theta_{JC} = 50°$ C/W



14 Lead Hybrid

$\theta_{JA} = 100°$ C/W

$\theta_{JC} = 45°$ C/W

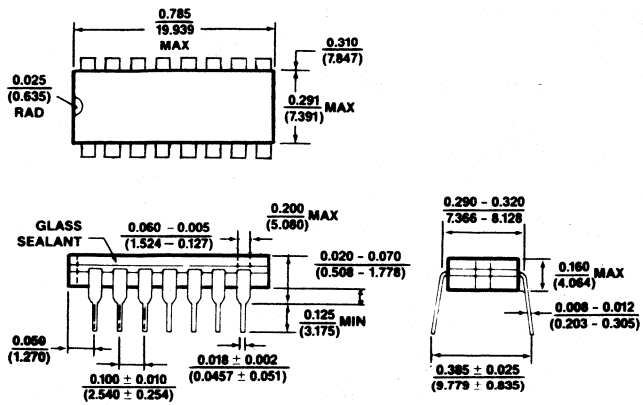


16 Lead Plastic Dip (PE)

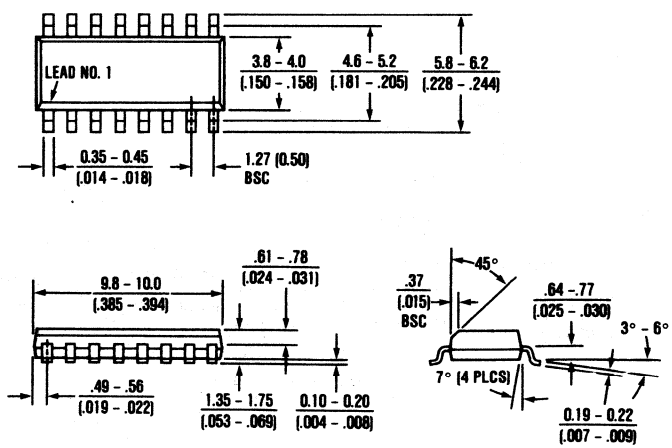
$\theta_{JA} = 135°$ C/W

$\theta_{JC} = 65°$ C/W

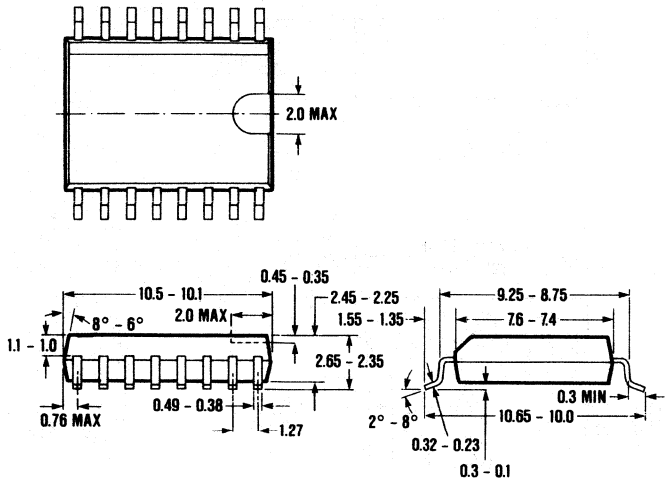
A



16 Lead CERDIP (JE)
$\theta_{JA} = 100°$ C/W
$\theta_{JC} = 50°$ C/W



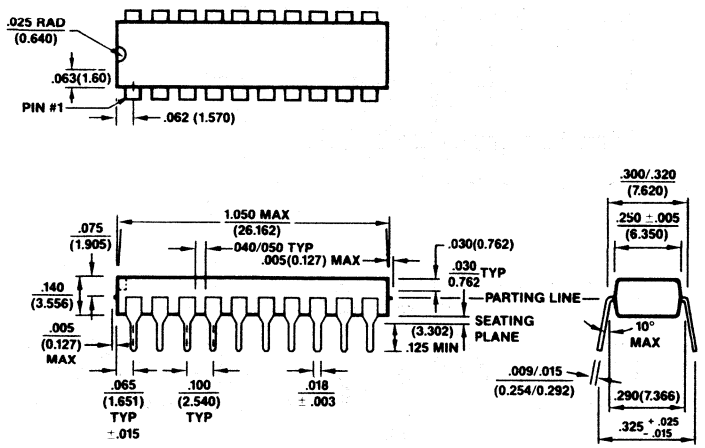
16 Lead Small Outline (SE)
$\theta_{JA} = 110°$ C/W
$\theta_{JC} = 60°$ C/W



16 Lead Small Outline, Wide (WE)

θ_{JA} = 90° C/W

θ_{JC} = 50° C/W

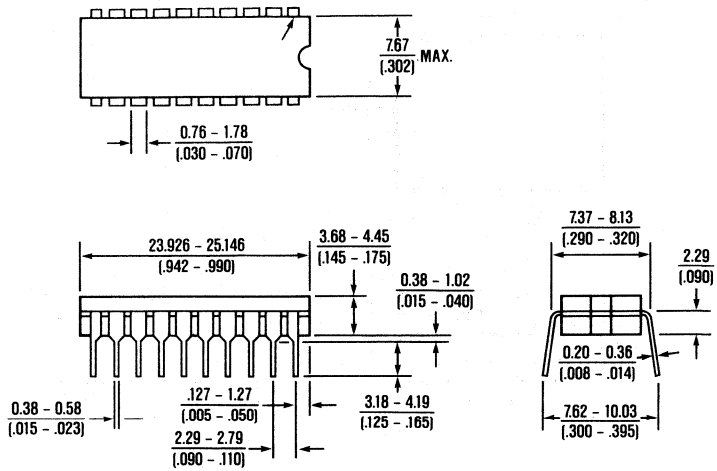


20 Lead Plastic Dip (PP)

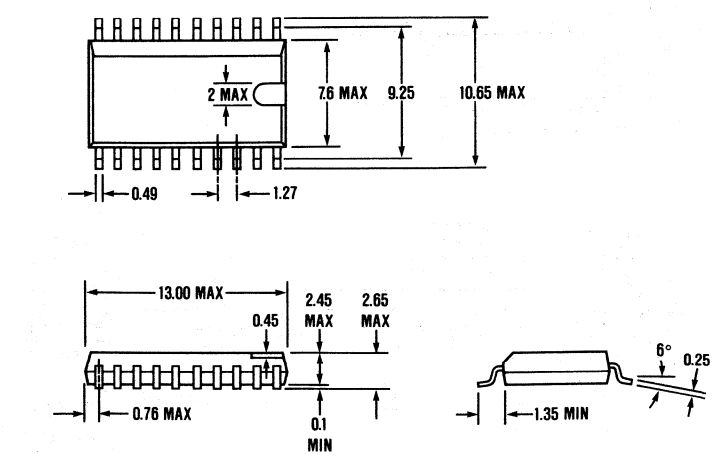
θ_{JA} = 125° C/W

θ_{JC} = 60° C/W

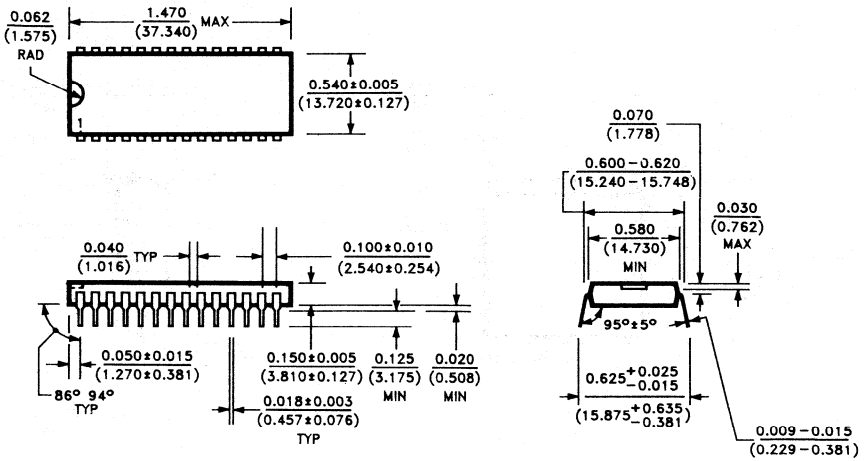
A



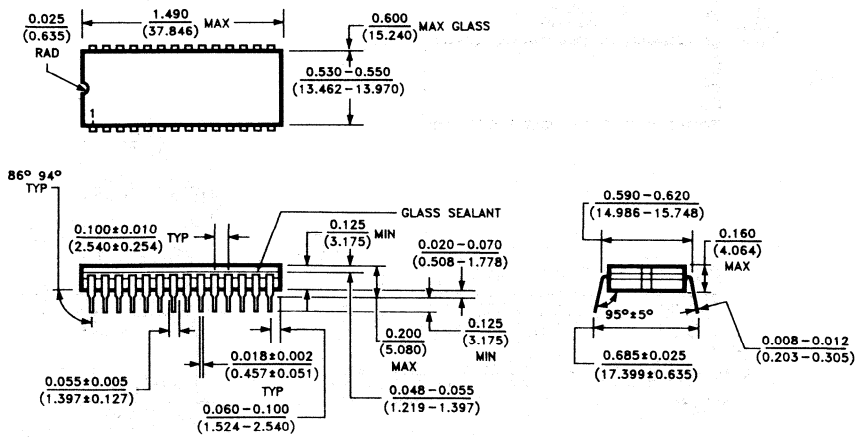
20 Lead CERDIP (JP)
$\theta_{JA} = 95°$ C/W
$\theta_{JC} = 45°$ C/W



20 Lead Small Outline, Wide (WP)
$\theta_{JA} = 90°$ C/W
$\theta_{JC} = 50°$ C/W



28 Lead Plastic Dip (PI)
$\theta_{JA} = 110°$ C/W
$\theta_{JC} = 50°$ C/W



28 Lead CERDIP (JI)
$\theta_{JA} = 55°$ C/W
$\theta_{JC} = 20°$ C/W

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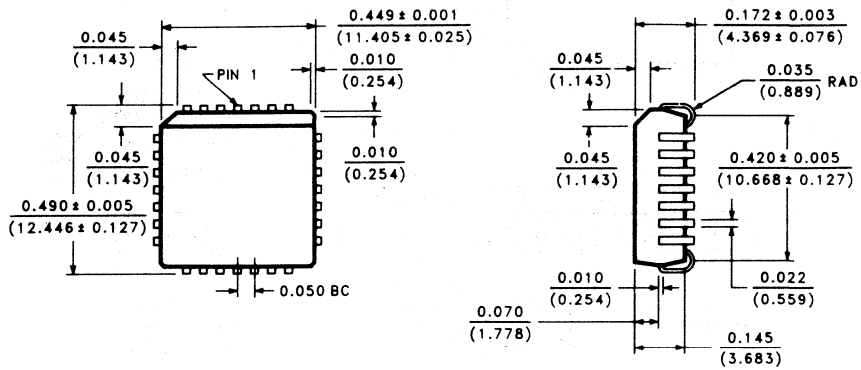
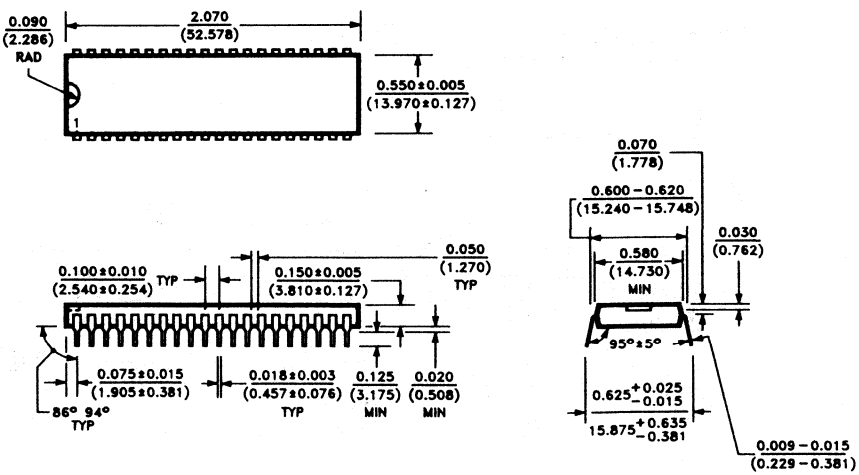
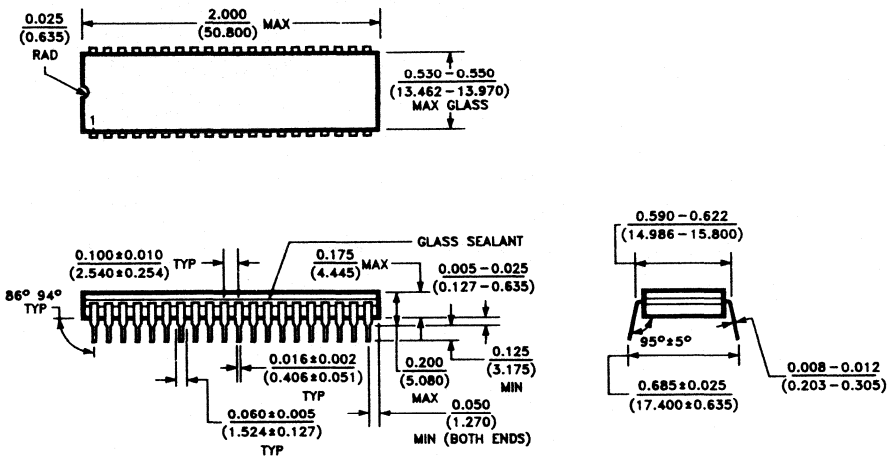


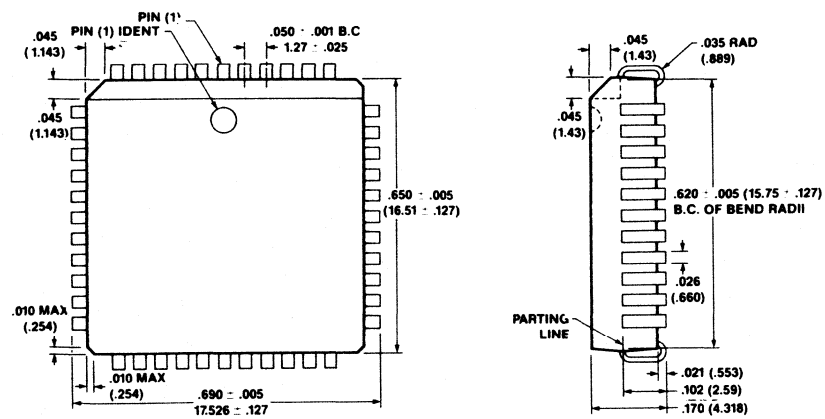
28 Lead Plastic Chip Carrier (Quad Pak) (Q)
θ_{JA} = 100° C/W
θ_{JC} = 45° C/W



40 Lead Plastic Dip (PL)
θ_{JA} = 100° C/W
θ_{JC} = 45° C/W



40 Lead CERDIP (JL)
$\theta_{JA} = 45°$ C/W
$\theta_{JC} = 20°$ C/W



44 Lead Plastic Chip Carrier (Quad Pak) (QH)
$\theta_{JA} = 80°$ C/W
$\theta_{JC} = 40°$ C/W

A

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A

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LINCWOOD-Tgrd

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See TAI Corp., New Jersey

Pennsylvania (West)
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